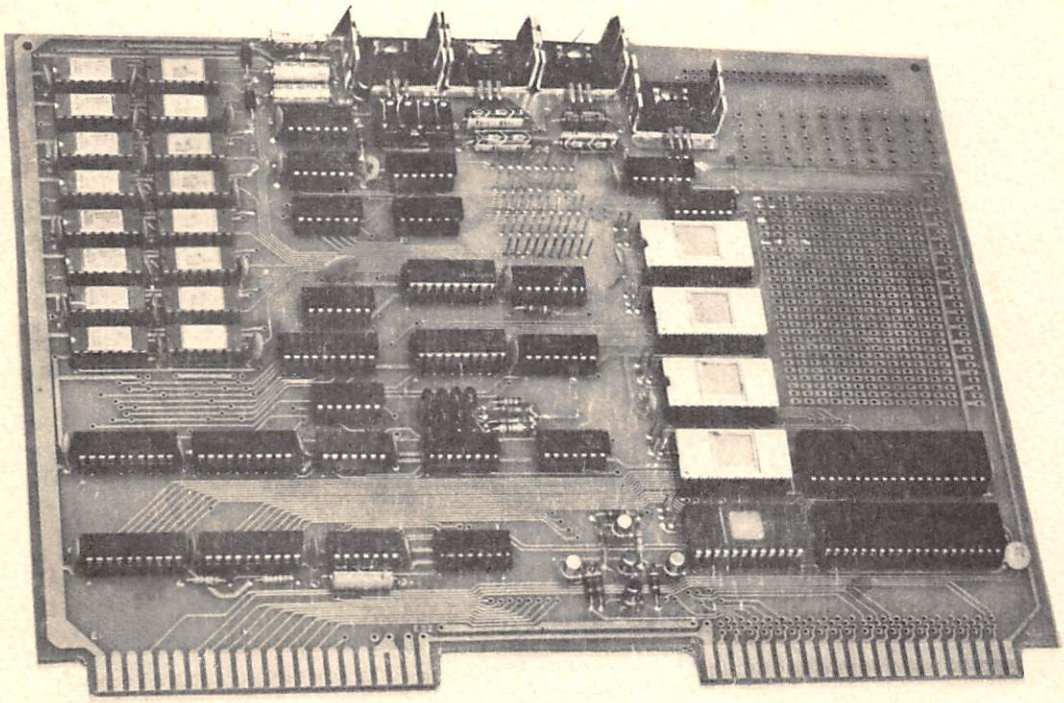
DRAM PLUS™



FOR THE

AIM • SYM • KIM

DRAM PLUS™

Multi-purpose Expansion Board

for the

AIM • SYM • KIM

16/32K RAM

8/16K EPROM

I/O Ports and Timers

EPROM Programmer

Prototyping Area

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DRAM PLUS

Table of Contents

Overview of DRAM PLUS Capabilities and Features

DRAM PLUS has been specifically designed to work with the AIM, SYM, and KIM microcomputers. With its combination of RAM, EPROM, EPROM Programmer and VIAs, it should be the only memory expansion board your system ever needs.

RAM Memory: 16K or 32K bytes of dynamic RAM. Transparent refresh. Addressable in 4K segments.

EPROM Memory: Sockets and address decoding for four EPROMS. These may be 2716/2516 2K type, 2732/2532 4K type, or 2332 4K ROMs. The various types may be used at the same time.

VIA 6522 I/O: Two Versatile Interface Adapter chips each provide two 8-bit programmable I/O ports with additional handshaking lines; two timer/counters; and a serial-to-parallel/parallel-to-serial shift register. This is the same I/O chip used on the AIM and SYM.

EPROM Programmer: A complete EPROM programming capability. Will handle the four types of EPROM, includes a voltage regulation/control circuit for the programming voltage, automatically verifies as it programs, and is very easy to use.

Simple Power: Only requires + 5 volts at about 1 amp and + 12 volts at about 150 milliamps. This may be provided directly as regulated power, or may be provided as slightly higher voltages which can be regulated on-board. The - 5 volts required by the dynamic RAMs is generated on-board. The programming voltage may be obtained by using three inexpensive transistor radio batteries.

Socketted ICs: All of the ICs are socketted so that a chip failure in the field may often be diagnosed and corrected without having to send the unit back for service.

MICRO Bus: The connections between the DRAM PLUS and the AIM/SYM/KIM follow the same conventions used by the KIM-4 mother board. DRAM PLUS may be interfaced via a simple cable or the MOTHER PLUS™.

Ready-to-go: The unit is fully assembled, burned-in and tested. It is a high quality unit, with solder masks on both sides and a silk screen.

Set Up and Check Out

Overview:

1. If you are using regulated power, + 5 and + 12 volts, then go to step 2. Otherwise, follow the instructions in the section on **Power.**

2. Attach the DRAM PLUS to your AIM, SYM or KIM via the Connector Cable you purchased, a cable you made [see **Building a Cable**], or a MOTHER PLUS board.

3. Attach + 12 volt regulated power to pin Z on the application connector.

4. Turn on your system. Using your system monitor, examine and modify a few locations in memory. The board is shipped with memory addresses **2000** to **5FFF** selected for RAM.

5. You have now successfully interfaced DRAM PLUS to your system. Read the various sections in this manual to find out how to make full use of this versatile expansion board.

Detailed Set Up and Start Up Instructions

1. Carefully unpack your DRAM PLUS board from its individual box, padding, and protective anti-static wrapping. While none of the components on this board are unusually susceptible to static, any chip can be damaged [i.e. destroyed] by a large static shock. So, take some care to avoid static build-up.

2. Examine the board for any visible damage which may have occurred in shipping. Push all ICs firmly into their sockets. Unbend any capacitors which have been bent. Check for any bent pins underneath the board which may be contacting adjacent runs. [A number of boards have been returned for repair which have required no more than the above 'service'].

3. Briefly read the entire DRAM PLUS manual. Pay particular attention to the main sections on **Power** and **Address Selection.**

4. Connect the DRAM PLUS to your MICRO. This may be done directly via the MOTHER PLUS, through the optional Connector Cable, or, if you are building your own cable assembly, proceed to the section on **Building a Cable.**

5. Set up your + 5 volt power connection in one of the following ways:

   a. If you have a single + 5 volt supply which is going to run both the DRAM PLUS and your microcomputer, then the normal Connector Cable or MOTHER PLUS will supply the proper connections to bring power from your system micro board to the DRAM PLUS. The Power Header should be placed in the + 5 volt position. In this position there is a wire jumper on the extreme left end of the Power Header. See the diagram below.

   b. If you have a separate + 5 volt regulated supply for DRAM PLUS, then there should be **no connection** between the + 5 of the microcomputer and the + 5 of the DRAM PLUS. If you are using the standard Connector Cable, you must remove the connections between DRAM E-21 & MICRO E-21 and between DRAM E-Y & MICRO E-21. If you are using the MOTHER PLUS board, then the traces to the expansion slot which contains the DRAM PLUS board should have the E-21 and E-Y traces cut from the rest of the bus. If you are making your own cable, do not make the + 5 volt power connections to the microcomputer.

      Attach your + 5 volt regulated power to the DRAM PLUS connector at E-21 and E-Y. Attach your power supply ground in common with the system ground. This may be done at E-1, E-22, E-A, E-Z and/or A-1. The Power Header should be positioned for regulated power as shown below.

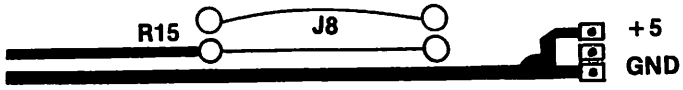
   c. If you have an unregulated + 8 to + 10 volt supply, then do **not** make any connections between the DRAM PLUS and the microcomputer + 5 volt supplies. Supply the unregulated power to DRAM E-19 and DRAM E-20. Connect the ground of your supply in common with the system ground. This may be done at the DRAM E-1, E-22, E-A, E-Z and/or A-1 connector points.

      The Power Header must be set to the unregulated position. In this position there is a jumper wire at the extreme right end of the Power Header. See the diagram below.

6. Set up the + 12 volt to the DRAM PLUS in one of the following ways:

a. If you are supplying regulated + 12, then simply connect it to the DRAM PLUS at the application connector A-Z and connect the ground from your supply to E-1, E-22, E-A, E-Z, and/or A-1. The board is shipped with jumper J8 in place. This connects A-Z to the + 12 distribution on the board directly. If your DRAM PLUS has ever been modified to work with the on-board regulators for + 12, as described in 6.b. below, then the resistor or jumper which was installed at R15 must be removed and a wire placed at jumper J8.

b. If you are going to use the on-board regulators and provide + 15 to + 24 volts to supply power for the + 12, then a modification will be required. First, remove jumper J8. This is located above the Prototyping Area. Then install a wire or resistor between the pair of holes directly below J8, marked on the left end as R15 and connected by a line to the right end. This new connection will connect the power you are providing to the input side of a 1 amp, + 12V regulator, Q4. The regulator is specified to handle up to 35 volts, but this will cause it to become quite hot. The use of a resistor to drop some of the voltage is recommended if the input voltage is above 15 volts. An 18 ohm 2 watt resistor works well for 24 volts.



7. The dynamic RAM chips used in DRAM PLUS require – 5 volts. To keep the power requirements for the board simple, this voltage is generated on-board, derived from the + 12 volt supply. Therefore, you do not have to do anything about this voltage. One word of warning, however. The capacity of the on-board circuit is designed to handle the 32K dynamic RAM only. It should **not** be used to drive any devices in the Prototyping Area. While there might be some additional capacity, it is recommended that it be left entirely alone.

8. When using the EPROM Programmer, a small amount of + 25 volt power is required. This may be simply provided by attaching + 27 to 30 volts at application pin A-22. This may be easily obtained by placing three 9V transistor radio type batteries in series, with the plus side to A-22 and the negative side to A-1. A 24 volt regulator, Q11, is part of a regulation circuit which will deliver the 30 milliamp + 25 volts required for programming. A safety circuit is built-in which protects the EPROM being damaged by only permitting the + 25 volts to reach the programming socket when the EPROM Programming Program is running. For this reason you will be unable to measure the 25 volts at the Programming socket under normal conditions. For more details on this valuable safety feature, read the section on **EPROM Programming.**

9. Now turn on your power. Using your monitor, examine some locations in the range 2000 to 5FFF. This is the 16K RAM area as the board is normally shipped. You should be able to read and write to any location within this area. If you can read and write into this RAM, then go on to step 10. If you are unable to read or write in this area, check the following potential problems:

A. Is the Power Header in the proper direction?
B. Are your power connections correct?
C. Does your power supply have enough power?
D. If you have other expansion boards in your system, is there any conflict in addressing?
E. Are the MSB1 jumpers connected to 2, 3, 4, and 5 on J1?
F. Are you cable connections all correct?
G. Have all ICs been pushed firmly into their sockets?

If none of the above problems are causing the difficulty, then go to the section on **Memory Testing and Field Repair.**

10. Now check the VIAs. The board is shipped with the VIAs addressed at 7000 (lower) and 7800 (upper). A quick test to indicate that the VIAs are working correctly may be made by examining a few addresses within each VIA. The values given in the table below should be found after a system RESET.

Address	Contents	Description
7000/7800	FF	Port B Data, set to FF by RESET
7001/7801	FF	Port A Data, set to FF by RESET
7002/7802	00	Port B Direction, set to 00 by RESET
7003/7803	00	Port A Direction, set to 00 by RESET
7004/7804	XX	Timer Low, constantly changing
7005/7805	XX	Timer High, constantly changing

Note that on the KIM, addresses 7004/7804 and 7005/7805 will look like 88 since the KIM monitor continually updates the LED display from the actual current contents of the address being examined. The AIM or SYM monitors only examine an address once, so their LED display will remain steady, but the value of data will change on each new request to examine the Timer addresses.

If the above values are found, then the VIAs are probably working correctly. Additional testing is left up to the imagination and requirements of the user. The VIAs were fully tested before shipping. If the above checks were positive, then go on to step 11. If the above values are not found, then check for the following problems:

A. Is there a jumper between pin 7 on J1 and pin V on J5?
B. Are the VIAs firmly in their sockets?
C. Are any devices attached to the Application Connector? If so, disconnect them and see if the problems disappear.

If none of the above problems are causing the difficulty, go to the section on **Memory Testing and Field Repair.**

11. Test the EPROM area by inserting an EPROM, preferably a programmed one whose contents you know, into the lowest EPROM socket - U38. This is the next to the bottom 24 pin socket. The lowest socket is for EPROM Programming. The DRAM PLUS is shipped with jumpers in place for a 2K EPROM to be addressed at 6000 to 67FF. The instructions presented in this section are only for a 2716 or 2516 type 2K EPROM. Section 12 discusses the test for use with a 2732, 2532, or 2332 type 4K device. Using your monitor, read the contents of the EPROM starting at 6000. If the values agree with what should be in the EPROM, all is probably well. Go on to step 13. If the values do not agree, make the following checks:

A. Is there a jumper wire between the pin labelled '6' on J1 and one of the two pins labelled 'E38' on J4?
B. Is there a jumper wire between the other pin labelled 'E38' on J4 and one of the pins labelled 'BA11' on J1, J2, J3, or J4?
C. Are there two jumpers in parallel on the jumper strip next to the EPROM socket U38?
D. Is the EPROM firmly in the socket and in the proper direction?

If the above checks do not solve the problem, go to **Memory Testing and Field Repair.**

12. To test the EPROM capability with a 4K device, the following jumper changes must first be made. Remove the jumper which connects pin 'BA11' on J1, J2, J3, or J4 to one of the pins marked 'E38' on J4. Use this jumper to connect the two pins marked 'E38' on J5 together. This will provide a 4K address space for the EPROM/ROM in U38. The jumper wires next to U38 must be changed for the type of device being used. See the wiring diagram on the DRAM PLUS board labelled 'J9 - J13' located near EPROM socket U39. For a 2732 or 2332, follow the diagram marked '2732'. Use the diagram marked '2532' for that type of device. Now read the contents of the device using your monitor. The addresses are in the 6000 to 6FFF range. If the results agree, then go on to step 13. If there is any problem, then carefully check all of the jumpers. If the problem is not found by inspection, then go to **Memory Testing and Field Repair.**

13. That's all. Your DRAM PLUS checks out. You may now want to reconfigure the RAM, EPROM, and VIAs to suit your particular system requirements. See **Address Selection** for details on how to do this. When you are ready for it, read the **EPROM Programming** section. You may want to run the Memory Test occasionally to make sure everything is still working well. You have now successfully installed a very flexible expansion board which should fulfill most of your RAM, EPROM and basic I/O requirements. With the addition of specialized circuits to the Prototype Area and the programming of various EPROMs as the needs arise, you should find this DRAM PLUS the mainstay of your system. We hope that it will give you years of uninterrupt service.

Power

Overview: The power requirements of DRAM PLUS are basically simple: +5 volts at about 1 amp and +12 volts at about 150 milliamps. That is all that the user must supply to run the board. While the dynamic RAM chips require a small amount of - 5 volts, this is generated on board from the +12 volts to keep the supply requirements simple. The only other voltage ever required is +27 volts when programming an EPROM.

+5 volts: The dynamic RAMS, the EPROMs, the VIAs, and all of the support chips require this voltage. A fully loaded board will draw about 1 amp. This voltage may be supplied as regulated +5 directly, or may be supplied as a regulated or unregulated voltage in the range +8 to +15 volts. On-board regulators will regulate this higher voltage down to the required +5. Three 5 volt regulators are provided in order to keep the power separate and clean. The dynamic RAMs and four of the 81LS95 ICs are served by one regulator [Q1: U1 - U20]; the majority of the support ICs are serviced by another regulator [Q2: U21 - U36]; the EPROMs, EPROM Programmer, VIAs and two support ICs by a third [Q3: U37 - U44].

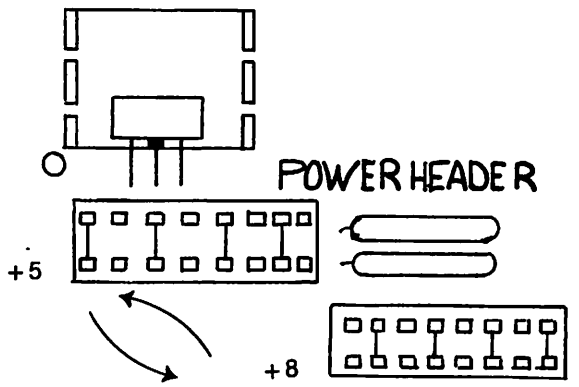
The Power Header [H1] determines whether or not the regulators will be used. When positioned so that there is no wire at the left end of the Header, the +8 to +15 volts will be directed through the regulators and the output of the regulators distributed throughout the board. When positioned such that there is a wire at the left end of the Header, the regulators are bypassed and the +5 volts from the external source is used to power the board.

+12 volts: This voltage may be provided as regulated +12 volts or regulated/unregulated +15 to 24 volts. In any case, the voltage is provided at pin Z of the DRAM PLUS application connector. If the regulated +12 is used, then a wire jumper is installed at J8, above the Prototype Area. This is the way the board is normally shipped. If the voltage is to be regulated on-board, then this jumper is removed and either a jumper or resistor is placed at R15. While the regulator is capable of handling up to 35 volts, it will get quite hot at the higher voltages. It is suggested that the higher voltages be lowered by using an 18 ohm 2 watt resistor in series with the regulator. Lower voltages can run the regulator direct.

+25 Programming Voltage: The 2716/2516/2732/2532 EPROMs all require +25 volts during programming. To make this voltage simple, and safe, a special circuit has been provided to take +27 to +35 volts and regulate it to the required +25. In addition to the regulation, there is a programmable switch, based on one of the VIAs, which prevents the programming voltage from reaching the programming socket unless the EPROM Programming Program is running. This can prevent the destruction of an EPROM in the event the user forgets to remove the programming power before removing the EPROM from the programming socket. If you attempt to measure the programming voltage at the programming socket when the program is not running, you will not get what you expect. The programming voltage can be tested at lower pin of the small voltage regulator, Q11.

A very easy way to provide the +27 volt input is to wire three 9 volt transistor batteries in series. The current drain while programming is very small, on the order of 30 milliamps, so a set of batteries will normally last about their normal shelf life. Connect the positive side of the battery pack to pin 22 on the application connector and the negative side to pin 1 on the aplication connector or any other convenient ground point.

- 5 volt power: This is generated on-board. Please do not attempt to 'borrow' any of this voltage for any other purpose. It is a reference voltage for the dynamic RAMS and should not be used for anything else.



Address Selection

The versatility of the address selection for the dynamic RAM, EPROM, and VIAs is a significant feature of this board. Each of the three types of device has it own set of addressing capabilities and will be covered separately.

RAM Address Selection

Overview: A wire jumper connected between J3 MSB1/MSB2 and one of the pins numbered 0 through F on J1/J2 determines the 4K segment starting address of a 4K segment.

The memory chips used to form the dynamic RAM portion of the board are configured as 16K locations with a single bit of information at each location. Eight chips in parallel form the 8 bit byte for the system. Circuitry is provided which allows the 16K locations to be selected as four semi-independent 4K segments. This means that the memory does not have to be used as a single 16K block. Each of the 4K segments may be separately selected. There are some restrictions on the set of addresses that may be used within any 16K segment. Address bits A12 and A13 may not be the same for any of the individual 4K segments within a 16K segment. This results in a type of "Chinese Menu" selection. One 4K segment may be selected from each column of the following table which lists the starting address of each of the 4K boundaries in hexidecimal:

0000	1000	2000	3000
4000	5000	6000	7000
8000	9000	A000	B000
C000	D000	E000	F000

An examination of the table will show that any four contiguous blocks will automatically come from different coulmns, and will therefore be valid. If blocks were selected at 1000, 2000, and 3000, then the fourth block would have to be 0000 (highly unlikely on an AIM/SYM/KIM), 4000, 8000, or C000, for that 16K segment of memory.

The actual selection of the RAM memory is provided by jumpers. The pins for the selection are contained in the five rows of pins toward the middle of the board about one inch below the regulators. The center row, J3, contains two sections marked 'MSB1' and 'MSB2'. MSB1 is the Memory Select Bank 1, and is connected to the dynamic RAM chips nearest the edge of the board. These are the chips normally installed on a 16K version. To select a 4K segment of this memory bank, a connection must be made between one of the four pins above the letters 'MSB1' and one of the 16 hex address lines in the two rows of jumpers directly below. J1 contains addresses 0K through 7K [0000, 1000, ... , 7000] as indicated by the markings 0 1 2 3 4 5 6 7. J2 contains addresses 8K through FK. To select a particular address for Memory Bank 1, simply connect any one of the MSB1 pins to the desired address pin.

The connection may be made via one of the jumper wires provided with the board; with a wire-wrap, or with a soldered wire in the case of a permanent installation. The advantage of the jumper wire is that it is quick, easy to change, and does not require any equipment. Its disadvantage is that it causes the wire to stick up above the board. This may be a problem in certain system configurations. The advantage of the wire-wrap is that it is quick, easy to change, and does not get in the way. It does require special equipment. The advantage of the soldered wire is that it will not be change by mistake, and can be kept out of the way. Choose whichever method suits your requirements and equipment.

Selection of RAM in the second Memory Bank follows the same rules. The only difference is that the connections are made between the address pins and the 'MSB2' pins.

VIA Addressing

Overview: The two VIAs share a 4K address segment. The lower VIA is in the lower half of the segment, the upper VIA is in the upper half.

The 4K segment which will contain both VIAs is selected by connecting the pin marked 'V' on J5 to one of the 4K address select pins on J1/J2. The lower VIA will have its addresses as the lowest 10 hex addresses of the 4K segment. For example, if the VIAs are placed in the 7000 segement, then the lower VIA will have its addresses as: 7000, 7001, 7002, ... , 700F. The upper VIA will have its addresses as the lowest 10 hex addresses of the next 2K segment: 7800, 7801, 7802, ... , 780F.

EPROM Address Selection

Overview: Jumpers between the pins marked as E38, E39, E40, and E41 on J4 and the address pins on J1/J2 determine the 4K starting address of each EPROM socket. A second jumper determines whether a socket is at a 4K boundary or at a 2K boundary.

EPROM address selection requires two sets of jumpers to be set. The first set of jumpers functions much like that discussed above for the RAM. The 4K addresses are selected by running jumpers from the appropriate pins on J1 and J2 to the particular EPROM pins on J4. There are four EPROM positions. They are marked between J4 and J5 as 'E38', 'E39', 'E40', and 'E41'. The 'E' stands for EPROM. The number refers to the socket number on the board. 'E38' is the EPROM in socket U38, the second socket up from the edge connector, adjacent to the upper VIA, directly above the EPROM Programming Socket. 'E39' is the next socket up, and so forth.

If 4K EPROMs are being used [INTEL 2732 type or TI 2532 type], then each socket needs to be addressed as an independent 4K segment. This is accomplished by connecting either one of the two pins on J4 for the particular EPROM to the desired 4K address on J1 or J2, and then connecting the two pins of J5 for the particular EPROM together. For example, to have the top EPROM socket, U41, be addressed at 6000, a wire would be run from the pin labelled '6' on J1 to one of the two pins labelled 'E41' on J4. The two pins labelled 'E41' on J5 would then be wired together.

If 2K EPROMs are being used [INTEL 2716 type or TI 2516 type], then each EPROM socket only requires a 2K address. It would be wasteful to use up 4K of addressing for each 2K EPROM. To avoid such waste, the address selection is designed to permit any EPROM socket to be selected on a 2K boundary. The first part of the selection is as above. A connection is made between the 4K address which contains the 2K boundary desired, that is 4000 for 4000 or 4800, 5000 for 5000 or 5800, and so forth, and the particular EPROM pins on J4. Then, instead of connecting the two EPROM pins on J5 together, an additional wire is brought to the unused EPROM pin on J4. This second wire is brought from either pin 1 ['$\overline{BA11}$'] or pin 2 ['BA11'] of jumpers J1 through J4. $\overline{BA11}$ will cause the EPROM to be selected in the upper half of the 4K space: 4800, 5800, etc. BA11 will cause the EPROM to be selected in the lower half of the 4K space: 4000, 5000, etc. By selecting the same 4K segment for two EPROM sockets and then setting one of them to the upper half [$\overline{BA11}$] and the other to the lower half [BA11], the two 2K EPROMs can share on 4K segment of memory. The second EPROM gets its 4K address by connecting a jumper from the 4K address pin of the first EPROM on J5. The ERPOM address pins are run in parallel from J4 to J5 to provide for this type of 'daisy chaining'.

Prototype Area Addressing

Overview: Provision is made for the Prototype Area to 'borrow' some of the address space of the VIA 4K segment.

Since each of the VIAs only uses the lowest 10 hex addresses in its 2K address space, it makes sense to use the extra address space for the Prototyping Area (PA) rather than using up additional address space. To make this easy, there is an etched jumper, J14, located between the upper VIA and the PA. This line carries the chip select for the upper VIA. The jumper may be cut and the left end connected to user supplied decode circuitry in the PA. Part of the new address decoding should include a chip select for the VIA at the lowest 10 hex addresses. When this is connected to the right end of the J14 pads, the VIA will function as normal. All of the remaining addresses in the 2K address space are now available for use by the user circuitry of the PA. Since the chip select for the 4K segment which contains the VIAs, and now the PA as well, also is used to control the bi-directional data bus buffers, interfacing additional circuitry is quite easy. For additional information on using the PA, see the section on the **Prototype Area**.

Building a Cable

If you are not connecting the DRAM PLUS to your AIM/SYM/KIM via the MOTHER PLUS or a purchased Connection Cable, then you must build your own cable. While this is a fairly straightforward task, it must be done carefully. The cable is comprised of two dual 22 pin connectors interconnected by wires which should be between about 5 and 8 inches in length. The following table gives the wiring list. Note that it is almost one-to-one except for a shift in the address lines.

Expansion Connector Cable

AIM/SYM/KIM	DRAM PLUS	Function of Signal
1	NC	[SYNC is not used]
[22]	1	Ground
2	NC	[RDY is not used]
3	NC	[Phase 1 is not used]
4	4	IRQ Interrupt Request. Interrupt LOW.
5	NC	[Not used]
6	NC	[NMI Non-Maskable Interrupt. Not used]
7	7	RES Reset. True when LOW.
8	8	Data Bit 7
9	9	Data Bit 6
10	10	Data Bit 5
11	11	Data Bit 4
12	12	Data Bit 3
13	13	Data Bit 2
14	14	Data Bit 1
15	15	Data Bit 0
NC	16	Decode Signal to KIM only. Application Connector A-K
17	NC	[Varies by microcomputer]
18	NC	[Varies by microcomputer]
NC	19	+8 volts optional power
NC	20	+8 volts optional power
21	21	+5 volts power. **Do NOT** connect to microcomputer pin 21 if separate + 5 V supplies are to be used for the microcomputer and DRAM PLUS!
22	22	Ground. Also connects to 1, A, and Z on DRAM PLUS
[22]	A	Ground
A	B	Address Bit 0
B	C	Address Bit 1
C	D	Address Bit 2
D	E	Address Bit 3
E	F	Address Bit 4
F	H	Address Bit 5
H	J	Address Bit 6
J	K	Address Bit 7
K	L	Address Bit 8
L	M	Address Bit 9
M	N	Address Bit 10
N	P	Address Bit 11
P	R	Address Bit 12
R	S	Address Bit 13
S	T	Address Bit 14
T	U	Address Bit 15
U	V	Phase 2
V	W	Read/Write bar
W	NC	[Read/Write. Not used]
X	NC	[Cassette Test. Not used]
Y	NC	[Phase 2 bar. Not used]
[+5]	Y	+5V external or from pin 21
Z	NC	[Ram R/W. Not used]
[22]	Z	Ground

Notes: There is one ground connection on the microcomputer expansion connector. This is normally tied to all four ground connections of the DRAM PLUS expansion connector. An additional ground may be run between pin 1 on the AIM/SYM/KIM application connector and pin 1 on the DRAM PLUS application connector. This is normally not required, but, in general, the more grounds the better. All five separate ground connections on the DRAM PLUS are tied together.

If the +5 volts is common between the microcomputer and the DRAM PLUS, then the connections should be made between pin 21 on the micro and pins 21 and Y on the DRAM PLUS. If the +5 volts is provided by separate supplies, then there should be no connection between these pins. Pins 21 and Y of the DRAM PLUS should go directly to the power supply.

The somewhat clumsy interconnection scheme presented above was defined by MOS Technology, inventors of the 6502 and KIM, for their original memory expansion boards and mother board. Even though these boards are no longer made, the definitions of the interconnections have been adopted by most manufacturers of expansion boards for the KIM. Since the AIM and SYM have the same microcomputer expansion pinouts, they will also work with this expansion bus scheme. This bus is sometimes called the 'KIM-4 Bus', referring to the MOS Technology Mother Board which defined the bus in hardware.

Loading the Cassette Tapes

The cassette tape supplied with the DRAM PLUS contains two useful programs. They are recorded in the standard KIM-1 format which is loadable on the AIM and SYM as well as the KIM.

MEMORY TEST [ID 10]: The Memory Test loads and runs entirely in page zero. Follow the instructions in **Memory Testing and Field Repair** to run the program. Load into your particular microcomputer as follows:

AIM: Set address **A408** to **5A** for KIM format tape. Use the **K** device for input. Filename is **10.**

SYM: Use **LD1** to load KIM format tape. Program ID is **10.**

KIM: Set **00F1** to **00.** Set **17F9** to ID **10.** Start tape loader at **1873.**

EPROM Programming Program [ID 20]: This program is used for programming EPROMs. It loads and runs in page zero. See **EPROM Programming** for details. Load into your particular microcomputer as follows:

AIM: Set address **A408** to **5A** for KIM format tape. Use the **K** device for input. Filename is **20.**

SYM: Use **LD1** to load KIM format tape. Program ID is **20.**

KIM: Set **00F1** to **00.** Set **17F9** to ID **20.** Start tape loader at **1873.**

Versatile Interface Adapter

Overview: The VIA 6522 is, as its name implies, a very versatile device. It consists of two independent 8-bit I/O ports with additional handshaking lines; two multi-mode timers; a serial-to-parallel/parallel-to-serial shift register; programmable interrupts; and so forth. It serves two distinct purposes on the DRAM PLUS board: general purpose I/O and the heart of the EPROM Programmer.

A Little Information: While the **Versatile Interface Adapter** data sheet in the Appendix provides a lot of detail about the use, operation, and organization of the device, a few words here may be helpful. The VIA addressing is discussed in detail in the section on **Address Selection.** Assuming that the two VIA's are in the 7000/7800 blocks of address space, the following table shows the basic purpose of each register address.

Address	Register	Function
7000/7800	ORB	Output Register B/Input Register B
7001/7801	ORA	Output Register A/Input Register A with Handshake
7002/7802	DDRB	Data Direction Register B
7003/7803	DDRA	Data Direction Register A
7004/7804	T1C-L	Timer/Counter 1 Low
7005/7805	T1C-H	Timer/Counter 1 High
7006/7806	T1L-L	Timer/Counter 1 Latch Low
7007/7807	T1L-H	Timer/Counter 1 Latch High
7008/7808	T2C-L	Timer/Counter 2 Low
7009/7809	T2C-H	Timer/Counter 2 High
700A/780A	SR	Shift Register
700B/780B	ACR	Auxiliary Control Register
700C/780C	PCR	Peripheral Control Register
700D/780D	IFR	Interrupt Flag Register
700E/780E	IER	Interrupt Enable Register
700F/780F	ORA2	Output Register A/Input Register A without Handshake

The Application Connector: The two VIAs have their signals brought out to the application connector. The **DRAM Schematic** in the Appendix shows the details of the connections. In summary, they are as follows:

The lower VIA in socket U43 and with the lower address has its connections on the alpha (bottom) side of the application connector.

VIA Signal	Application	Function/Name
CA1	B	Peripheral A Control Line 1
CA2	C	Peripheral A Control Line 2
PA0 - PA7	D - M	Peripheral A Port
PB0 - PB7	N - W	Peripheral B Port
CB1	X	Peripheral B Control Line 1
CB2	Y	Peripheral B Control Line 2

The upper VIA in socket U44 and with the higher address has its connections on the numeric (top) side of the application connector.

VIA Signal	Application	Function/Name
CA1	2	Peripheral A Control Line 1
CA2	3	Peripheral A Control Line 2
PA0 - PA7	4 - 11	Peripheral A Port
PB0 - PB7	12 - 19	Peripheral B Port
CB1	20	Peripheral B Control Line 1
CB2	21	Peripheral B Control Line 2

Note: The only other connections on the Application Connector are +5V at A, ground at 1, +27V for programming at 22, and +12V at Z.

Caution: Be sure to disconnect any devices from the Application Connector which might affect the VIAs before attempting to run the EPROM Programmer. You may wish to have two separate Application Connection connectors, one with the VIA I/O connections and one with just the +27 and ground for programming.

Prototype Area

Overview: One of the nice little extras that the DRAM PLUS board provides is the Prototype Area (PA). Although it is small, it can be invaluable when a small circuit is required.

How to use it: If you look on the bottom side of the board you will see that the individual pads of the PA are connected together in groups of two or three. The hole layout is designed to accommodate either .300 or .600 sockets and ICs, and may be used with wire-wrap or solder sockets. If wire-wrap sockets are used, then simply follow standard wire-wrapping procedures, treating each hole as independent from the rest. If solder type sockets are used, the socket is soldered into one set of holes and the pads connected to those holes are used to provide interconnection wiring points. Ground and +5 volts are available along the edge of the board near the PA. The pads connected along the edge to the trace on the bottom of the board are ground. The pads connected to the trace on the top of the board are +5 volts.

Input/Output Connections: Input and output for the PA that is off-board may use the special connector located near the top of the board. A number of manufacturers make connectors which will fit into the holes provided. The connectors are available in various sizes so that you do not need to buy a 50 pin connector if all you need are 20 pins. The matrix between the PA and the top connector provides a maping between the two. Alternatively, if some of the VIA application connector locations are not required by the system, provision has been made for them to be cut between the adjacent pads near the application connector, freeing up the connector pin for the PA connection. A pair of pads is provided so that the VIA can be reconnected if necessary at a later time.

Addressing Hints: As discussed briefly in the section on **Address Selection**, provision has been made for the PA to use some of the VIA addressing space. This is done by cutting the jumper, J14, between the PA and the upper VIA; building a decoding circuit in the PA; and returning the lowest 10 hex addresses to the VIA at the right end of the jumper. The additional address lines required for the decoder, and for other purposes within the PA, can be most easily be obtained by placing a 24 pin header in an unused EPROM socket (assuming there is an unused socket), and picking up the required address lines from there. Address lines BA0 to BA10 are available at the EPROM socket. Since lines BA11 through BA15 have already made their contribution to the address decoding, they should not normally be needed. Data lines BD0 to BD7 are also available at the EPROM socket.

One reasonable decoding circuit would provide eight additional selects using a single 74LS138, which we will refer to as DECODE, as follows:

Connect BA8 from EPROM socket pin 23 to pin 1 on DECODE
Connect BA9 from EPROM socket pin 22 to pin 2 on DECODE
Connect BA10 from EPROM socket pin 19 to pin 3 on DECODE
Cut jumper J14 and attach left pad to pins 4 and 5 on DECODE
Connect a 3.3K pull-up resistor between +5 and pin 6 on DECODE
Connect ground to pin 8 of DECODE
Connect right pad of jumper J14 to pin 15 of DECODE
Connect +5 volts to pin 16 of DECODE

With these connections, and the VIA select at 7000, the upper VIA will still be selected as 7800, and the remainder of the address space will be divided in 100 hex blocks. Pin 14 is 7900, pin 13 is 7A00, pin 12 is 7B00, pin 11 is 7C00, pin 10 is 7D00, pin 9 is 7E00 and pin 7 is 7F00. Pin 15 which was used to re-connect the VIA is 7800 - just as before the additional decoding was added. The user may now use this additional decoding for whatever purposes he choses.

Three Inverters: There are three free 74LS04 inverter gates available on the board. These are marked on the board. To use any of them, simply connect the signal to be inverted to the input pad and get the inverted signal from the output pad.

Applications for the PA: There are obviously a large number of possible applications for this area. We will issue, from time-to-time, application notes. A few suggestions to start with include: programmable write protection of some or all of the on-board RAM; programmable address switching of the EPROM sockets to permit two different sets of software which reside in the same address space to be selected one-at-a-time; provide buffers/drivers for VIA signals when necessary; and, of course, implement complete circuits which have nothing to do with the rest of the DRAM board.

If you design some circuitry which you feel would be of interest to other, please send us complete specifications and we will try to distribute the information.

EPROM Programming

Overview: An important key to the real usefulness of the DRAM PLUS board is the EPROM Programmer. Having an easy-to-use, always available programmer that is totally compatible with the rest of the system adds a new dimension to the use of EPROMs. No more dumping punched paper tapes in some terrible format; no more waiting for someone else to do the job. The entire programming process can be accomplished on the DRAM PLUS board in just a couple of minutes.

The Major Components: The EPROM Programming facility is comprised of a number of parts. This consist of the EPROM Programming Socket (EPS), the two VIAs, a voltage regulating/control circuit, an EPROM Programming Program (EPP), and some memory - RAM or EPROM - which contains the information to be stored in the EPROM. All of these parts, working together, making the programming possible.

EPROM Programming Socket (EPS): The EPS is U37 and is located near the application connector to the immediate left of the lower VIA. Immediately to the left of the EPS is a five pin jumper block, J13. This jumper block permits the socket to be configured for use with the 2716/2516 2K EPROMs, the 2732 and 2532 4K EPROMS. The diagram toward the center of the DRAM board shows how the pair of jumpers is to be placed for each of the three types of EPROM. The EPS is very special. It is **not** connected to any of the system address, data or control lines! It is, essentially, a "figment of the VIAs' imagination". This may be seen by referring to the DRAM PLUS Schematic in the Appendix.

The VIAs: The lower VIA, U43, provides eleven (11) pseudo address lines and two (2) programming control lines. The upper VIA, U44, provides eight (8) pseudo data lines and controls the +5 volt and +25 volt lines as well. Programming is accomplished by having the VIAs establish and latch the pseudo address and data lines, and then provide the programming control pulses.

The Voltage Regulation/Control Circuits: There are two separate circuits under control of the upper VIA, U44. The first circuit provides the +25 volt programming voltage. This is regulated by a 24 volt regulator/diode combination (Q11). It is controlled by a circuit consisting of three transistors (Q7, Q8, and Q9), three resistors (R8, R9, and R10), and an invertor (U21). The voltage is not permitted to get to the EPS unless the EPROM Programming Program is running. The second circuit controls the +5 volts, keeping is low unless the program is running. It consists of two transistors (Q6 and Q10), and two resistors (R7 and R11). These regulation/control circuits help prevent accidental damage to the EPROM, especially that caused by inserting/removing an EPROM into/from a "live" socket.

The EPROM Programming Program: The entire programming operation is orchestrated by a program. The EPP has been written to run on any AIM, SYM, or KIM without user modification. It is normally loaded from a cassette tape and resides in page zero. It takes as its operating parameters the address of where the code to be copied starts, where it ends, and an offset into the EPROM space.

The Memory to be Copied From: Since the EPROM Programming Socket resides in the VIAs' 'fantasy land', and therefore does not actually occupy any memory space, it does not matter where the program being copied resides. It may be on the DRAM PLUS board in RAM or EPROM or both, or it may be in any other memory accessible to the microcomputer. The material to be copied does not have to be in the location which it would normally run in.

Running the EPROM Programmer: There are just a few steps required to program EPROMS:

1. Load the data to be programmed into any memory.
2. Load the EPROM Programming Program into page zero from cassette.
3. Setup the EPROM Programming Socket jumpers for the type of EPROM to be programmed.
4. Insert the EPROM in the EPS.
5. Turn on the +27 volt supply.
6. Enter the starting address of the data to be copied into addresses 0000 and 0001 in the normal 6502 order: low address, high address.
7. Enter the offset into the EPROM into addresses 0002 and 0003: low offset, high offset. While an EPROM may be programmed from its lowest address, 0000, it does not have to be. There are many occasions in which the programming is to start at some other address within the EPROM. That address is provided by this offset value.
8. Enter the last address to be copied into addresses 0004 and 0005: low address, high address.
9. Start the EPP running at 0006. The program will run until it has programmed all of the data requested, or until some error condition is detected. A table in the EPROM Programmer Program Listing in the appendix shows the exits for the three microcomputers.
10. If the programming was successful, remove the EPROM, turn off the programming power, and the operation is complete.

Memory Testing and Field Repair

You should test the RAM, when you initially set up your system. You may also want to test it occasionally to make sure it is all working correctly. Finally, you will definitely want to test it whenever you have any reason to suspect that it is not working properly. The DRAM PLUS Memory Test was adapted from "Memory Test" by Jim Butterfield, **The First Book of KIM**, edited by Butterfield, Ockers and Rehnke, pages 122-123.

> "Testing RAM isn't just a question of storing a value and then checking it. It's important to test for interference between locations. Such tests often involve writing to one location and then checking all other locations to see they haven't been disturbed; this can be time consuming.
>
> This program checks memory thoroughly and runs exceptionally fast. It is adapted from an algorithm by Knaizuk and Hartmann published in "**IEEE Transactions on Computers**", April 1977.
>
> The program first puts value FF in every location under test. Then it puts 00 in every third location, after which it tests all locations for correctness. The test is repeated twice more with the positions of the 00's changed each time. Finally, the whole thing is repeated with the FF and 00 values interchanged.
>
> To Run: Set the addresses of the first and last memory pages you wish to test into location 0000 and 0001 respectively. Start the program at address 0002; it will halt with a memory address on the display. If no faults were found, the address will be one location past the last address tested. If a fault is found, its address will be displayed."

The DRAM PLUS version of the Memory Test will run on an AIM, SYM or KIM. It is provided on the DRAM PLUS Cassette Tape as the first program with program ID = 10. It is completely self-modifying. Set the starting page in 0000 [a 20 if the DRAM RAM to be tested starts at location 2000], the ending page in 0001 [a 5F if the DRAM RAM is selected from 2000 to 5FFF], and then start the program at 0002. The program should only take a few seconds, depending on the amount of memory to be tested. It should exit by printing a memory address on the display of your AIM, SYM, or KIM. If the address is the last address tested plus 1 [6000 if 5F was the last address specified in location 0001], then the test did not detect any errors and your memory is probably functioning correctly. If any other address is displayed, it indicates that an error was found at the address displayed. The contents of the displayed address provide a clue as to the problem. The contents of a correct address after the test will be an FF or a 00.

If the error address contains a value that has missing bits [FB for example] or added bits [20 for example], then a particular 4116 memory chip may be defective. Using the **Memory Map**, determine which chip is suspect and try exchanging it with another chip. Several things may happen:

If the chip is truly defective, the problem will move with the chip. For example the test which failed before at some location with 'FB' may now fail and show 'BF'. If this occurs, the 4116 probably needs to be replaced.

If the problem was due to improper seating of the 4116 in its socket, or due to oxidation or dirt in the socket, then the test may now pass since the problem may have been corrected by physically moving the chip.

If the problem is due to some cause other than a defective 4116, then the problem may continue to occur at the same address no matter what 4116 chip is put there. In this case, you can try to solve the problem by a little more sophisticated chip swapping. Try swapping the support chips. Exchange the two 74LS245 chips [U31 and U32]. U32 controls the RAM data lines; U31 controls the EPROM, VIA and Prototype Area data lines. If this cures the problem, you have a defective 74LS245. Examine the **DRAM PLUS Schematic**. You will see other chips such as the 81LS95s and 74LS32s which are used in multiple places on the board. Try interchanging identical chips to see if the problem moves and/or disappears. If you can isolate the problem by chip swapping, then it is a simple matter to replace the defective chip. This should be the only type of problem to occur on these boards. If none of these chip swaps work, then you may have to send the board back for service.

Memory Map

Memory Bank 1			Memory Bank 2		
U3	Data Bit 7	Hex Value 80	U13	Data Bit 7	Hex Value 80
U4	Data Bit 6	Hex Value 40	U14	Data Bit 6	Hex Value 40
U5	Data Bit 5	Hex Value 20	U15	Data Bit 5	Hex Value 20
U6	Data Bit 4	Hex Value 10	U16	Data Bit 4	Hex Value 10
U7	Data Bit 3	Hex Value 08	U17	Data Bit 3	Hex Value 08
U8	Data Bit 2	Hex Value 04	U18	Data Bit 2	Hex Value 04
U9	Data Bit 1	Hex Value 02	U19	Data Bit 1	Hex Value 02
U10	Data Bit 0	Hex Value 01	U20	Data Bit 0	Hex Value 01

Parts List

Item	Part Number	Qty.	Description
		Integrated Circuits	
1.	U3 - U10, [U13 - U20]	8/[16][1]	4116 Dynamic RAM, 16K x 1 bit
2.	U1, U2, U11, U12, U24	5	81LS95 Octal buffer
3.	U22	1	74LS00 Quad 2-input positive NAND gates
4.	U21, U23, U34B	3	74LS04 Hex inverters
5.	U28	1	74LS08 Quad 2-input positive AND gates
6.	U26, U27	2	74LS10 Triple 3-input positive NAND gates
7.	U45	1	74LS11 Triple 3-input positive AND gates
8.	U33	1	74LS20 Dual 4-input positive NAND gates
9.	U34A, U42	2	74LS32 Quad 2-input positive OR gates
10.	U35, U36	2	74LS138 3-to-8 decoders/multiplexers
11.	U29, U30	2	74LS221 Dual monostable multivibrators
12.	U31, U32	2	74LS245 Octal bus tranceivers
13.	U25	1	74393 Dual 4-bit binary counters
14.	U43, U44	2	6522 Versatile Interface Adapter
		Regulators and Transistors	
15.	Q1, Q2, Q3	3	7805 +5 volt regulator
16.	Q4	1	7812 +12 volt regulator
17.	Q5, Q7 - Q9	4	2N2222 General purpose transistors
18.	Q11	1	78L24 +24 volt regulator
		Resistors, Capacitors and Diodes	
19.	R3	1	1.2K ¼ watt
20.	R13	1	1.6K ¼ watt
21.	R1	1	1.6K ½ watt
22.	R12	1	2.2K ¼ watt
23.	R5	1	2.7K ¼ watt
24.	R2, R8, R9	3	4.7K ¼ watt
25.	R4	1	6.2K ¼ watt
26.	R6	1	7.5K ¼ watt
27.	R10	1	20K ¼ watt
28.	[R14][1]	[1]	[3.3K ¼ watt]
29.	[R15][2]	[1]	[18 ohm 2 watt]
30.	C1 - C7, C12	8	22 MFD at 50 volts
31.	C8 - C11	4	50 pFD Dip Mica
32.	C13	1	4.7 MFD at 35V
33.	C14, C15	2	.01 MFDmonolithic
34.	C16 - C54	39	.01 MFD
35.	D1, D2, D3, D6	4	1N914 or 1N4148 diode
36.	D4	1	1N750 or 1N751 diode
37.	D5	1	1N752 diode
		Miscellaneous	
38.	J1 - J5	5	10 pin AMP headers
39.	J9 - J13	5	6 pin AMP headers
40.		4	Heat sinks for regulators
41.		11	14 pin Augat dip sockets
42.		20	16 pin Augat dip sockets
43.		7	20 pin Augat dip sockets
44.		5	24 pin Augat dip sockets
45.		2	40 pin Augat dip sockets
46.	H1	1	16 pin Header
47.		11/[15][1]	Wire jumpers. Enough are supplied for the RAM, VIAs, Eprom Programmer and one EPROM. If you are going to use this type of jumper for the other EPROMs, write and we will send an additional 12 jumpers at no charge.

Notes:
1. An optional device which is not supplied.
2. This is provided, but not installed. The user should install it and remove jumper J8 when using +24 volts. See **POWER** for details.
3. The following parts are indicated on the silk screen but have been eliminated from the circuit: Q6, Q10, R7 and R11.

Notes, Errata, Suggestions, and Hints

Since this is the first version of DRAM PLUS, there are bound to be some changes, corrections, etcetera. Please read this section carefully and, if necessary, make any corrections in the referenced sections. In this manner we can keep the documentation updated, providing the user with the latest information.

1. **EPROM Programming Changes:** The Voltage Regulation/Control Circuits [page 13] have been changed. The +25 volt control circuit holds the voltage at +5 volts for low, not zero. This circuit is used to provide the two voltages required for programming and verifying the 2732/2532 EPROMs. The +5 volt control circuit has been eliminated. This voltage is always present at the EPROM Programming socket. Therefore, you should probably remove the +27 input voltage and the system +5 volts before inserting or removing an EPROM from the programming socket, to avoid any possible damage to the EPROM. My experience to date, with 2716 and 2532 types, is that no damage occurs, as long as the program is not running and the +25 volts is not therefore present at the socket. I have not yet tested the 2732 EPROM.

The changes to the EPROM Programming circuit resulted in the elimination of the following parts which are shown on the silk screen: **Q6, Q10, R7** and **R11**. These parts are intentionally left off of the board.

2. **EPROM Programming Program:** Use the instructions in Appendix B for running the EPROM Programming Program, not those on page 13.

3. **Prototype Area +5 and GND:** The pads along the right hand edge of the board near the Prototype Area contain +5 volt and ground connections. The pads connected on the top side of the board are **GROUND**. The pads connected on the bottom side of the board are **+5 volts.**

4. **Using +24 volts:** The resistor required to run the board with +24 volts in place of the regulated +12 is provided for the user to add if required. Unfortunately, the holes drilled in the board are too small for the 2 watt resistor. Two easy solutions are possible: drill out the holes to accommodate the resistor, or, tack the resistor directly to the board using small wires through the holes to insure a firm contact. Do not forget to remove Jumper 8.

5. **Jumper Wires:** Make sure the jumper wires do not touch each other and short.

Limited Warranty and Service

Should you experience difficulty with your **DRAM PLUS** board and be unable to diagnose or correct the problem, you may return the board to The COMPUTERIST, Inc. for repair. **DRAM PLUS** is warranted by The COMPUTERIST, Inc. against defects in workmanship and materials for a period of ninety [90] days from date of delivery. During the warranty period, The COMPUTERIST, Inc. will repair or, at its option, replace at no charge any components that prove to be defective provided that the board is returned, shipping prepaid, to:

The COMPUTERIST, Inc.
Service Department
34 Chelmsford Street
Chelmsford, MA 01824

This warranty does not apply if the board has been damaged by accident or misuse, or as a result of repairs or modifications made by other than authorized personnel at the above service facility. No other warranty is expressed or implied. The COMPUTERIST, Inc. is not liable for consequential damages.

Beyond the ninety [90] day warranty period, **DRAM PLUS** boards will be repaired for a reasonable service fee. All service work performed by The COMPUTERIST, Inc. beyond the warranty period is warranted for an additional ninety [90] day period after shipment of the repaired board.

It is the customer's responsibility to return the board with shipping charges prepaid to the above service facility. For in-warranty service, the board will be returned to the customer, shipping prepaid, by the fastest economical carrier. For out-of-warranty service, the customer will pay for shipping charges both ways. The repaired board will be returned to the customer COD unless the repairs and shipping charges have been prepaid by the customer.

If you have any minor problems, please call us at 617/256-3649 and ask for "Service".

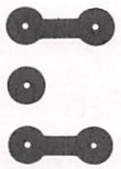
```
                        MEMORY TEST  9 FEBRUARY 1979

                        MEMORY ORG   $0000

                        ACCESS *     $8B86  SYM-1 ACCESS ENTRY
                        OUTBYT *     $82FA  SYM-1 OUTPUT BYTE
                        SCANDS *     $8906  SYM-1 SCAN DISPLAY

                        GOKIM  *     $1C4F  KIM-1 ENTRY POINT
                        LPOINT *     $00FA  KIM DISPLAY POINTERS
                        HPOINT *     $00FB


                        ASCOUT *     $EF7B  AIM 65 OUTPUT ASCII

0000 20                 BEGIN  =     $20    STARTING TEST PAGE
0001 3F                 END    =     $3F    ENDING TEST PAGE

0002 A9 00              START  LDAIM $00    ZERO POINTERS
0004 A8                        TAY          FOR LOW ORDER ADDRESSES
0005 48                        PHA          SET ALL STATUS BITS TO ZERO
0006 28                        PLP
0007 85 D1                     STAZ  POINTL

0009 85 D3              BIGLP  STAZ  FLAG   = 00 FIRST PASS, = FF SECOND PASS
000B A2 02                     LDXIM $02
000D 86 D5                     STXZ  PASS   SET 3 TESTS EACH PASS

000F A5 00              NPASS  LDAZ  BEGIN  SET POINTER TO
0011 85 D2                     STAZ  POINTH START OF TEST AREA
0013 A6 01                     LDXZ  END
0015 A5 D3                     LDAZ  FLAG
0017 49 FF                     EORIM $FF    REVERSE FLAG
0019 85 D4                     STAZ  FLIP   = FF FIRST PASS, = 00 SECOND PASS

001B 91 D1              CLEAR  STAIY POINTL WRITE FLIP VALUE
001D C8                        INY          INTO ALL LOCATIONS
001E D0 FB                     BNE   CLEAR
0020 E6 D2                     INCZ  POINTH
0022 E4 D2                     CPXZ  POINTH
0024 BC F5                     BCS   CLEAR

                        FLIP VALUE IN ALL LOCATIONS.  NOW CHANGE 1 IN 3

0026 A6 D5                     LDXZ  PASS
0028 A5 00                     LDAZ  BEGIN  SET POINTER
002A 85 D2                     STAZ  POINTH BACK TO START

002C A5 D3              FILL   LDAZ  FLAG   CHANGE VALUE
002E CA                 TOP    DEX
002F 10 04                     BPL   SKIP   SKIP 2 OUT OF 3
0031 A2 02                     LDXIM $02    RESTORE 3 COUNTER
0033 91 D1                     STAIY POINTL CHANGE 1 OUT OF 3
0035 C8                 SKIP   INY
0036 D0 F6                     BNE   TOP
0038 E6 D2                     INCZ  POINTH NEW PAGE
```

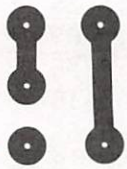
```
003A A5 01          LDAZ  END    HAVE WE PASSED
003C C5 D2          CMPZ  POINTH END OF TEST AREA?
003E B0 EC          BCS   FILL   NO. KEEP GOING

              MEMORY SET UP.  NOW TEST IT

0040 A5 00          LDAZ  BEGIN  SET POINTER
0042 85 D2          STAZ  POINTH BACK TO START
0044 A6 D5          LDXZ  PASS   SET UP 3 COUNTER

0046 A5 D4    POP   LDAZ  FLIP   TEST FOR FLIP VALUE
0048 CA             DEX          2 OUT OF 3 TIMES
0049 10 04          BPL   SLIP   OR
004B A2 02          LDXIM $02    1 OUT OF 3 TIMES
004D A5 D3          LDAZ  FLAG   TEST FOR FLAG VALUE

004F D1 D1    SLIP  CMPIY POINTL HER IS THE TEST
0051 D0 15          BNE   OUT    BRANCH IF FAILED
0053 C8             INY          BUMP POINTER
0054 D0 F0          BNE   POP    IF NOT DONE, KEEP BOING
0056 E6 D2          INCZ  POINTH
0058 A5 01          LDAZ  END    TEST END
005A C5 D2          CMPZ  POINTH
005C B0 E8          BCS   POP

              ABOVE TEST OKAY.  CHANGE AND REPEAT

005E C6 D5          DECZ  PASS   CHANGE 1 IN 3 POSITION
0060 10 AD          BPL   NPASS  AND DO NEXT PASS
0062 A5 D3          LDAZ  FLAG   INVERT FLAG
0064 49 FF          EORIM $FF    FOR PASS TWO
0066 30 A1          BMI   BIGLP  AND REPEAT BIG LOOP

0068 84 D1    OUT   STYZ  POINTL PUT LOW ORDER ADDRESS FOR DISPLAY
006A AD FD FF       LDA   $FFFD  TEST HIGH BYTE OF INTERRUPT VECTOR
006D C9 8B          CMPIM $8B    = SYM-1
006F F0 46          BEQ   SYM
0071 C9 E0          CMPIM $E0    = AIM 65
0073 F0 0B          BEQ   AIM

0075 A5 D1    KIM   LDAZ  POINTL MOVE POINTERS FOR KIM
0077 85 FA          STAZ  LPOINT
0079 A5 D2          LDAZ  POINTH
007B 85 FB          STAZ  HPOINT
007D 4C 4F 1C       JMP   GOKIM  RETURN TO KIM MONITOR

0080 A5 D2    AIM   LDAZ  POINTH MOVE DATA FOR AIM DISPLAY
0082 85 D6          STAZ  AHIGH
0084 A5 D1          LDAZ  POINTL
0086 85 D7          STAZ  ALOW
0088 A2 00          LDXIM $00    GET DATA AT ADDRESS
008A A1 D1          LDAIX POINTL
008C 85 D8          STAZ  ADATA
008E A2 13          LDXIM $13    START AT POSITION 19.

0090 8A       ALOOP TXA          SAVE X VALUE
```

```
0091 48              PHA          ON STACK
0092 A0 04           LDYIM $04    SHIFT 4 POSITIONS PER CHARACTER
0094 A5 D8           LDAZ  ADATA  GET DATA
0096 29 0F           ANDIM $0F    MASK TO NIBBLE
0098 C9 0A           CMPIM $0A    TEST DECIMAL
009A 30 03           BMI   AOKAY  DECIMAL
009C 18              CLC          A - F.  MUST CONVERT TO
009D 69 07           ADCIM $07    ASCII
009F 18       AOKAY  CLC          FINISH CONVERSION
00A0 69 B0           ADCIM $B0    ASCII + AIM FLAG
00A2 20 7B EF        JSR   ASCOUT OUTPUT TO DISPLAY
00A5 46 D6    AMOVE  LSRZ  AHIGH  MOVE TO NEXT NIBBLE
00A7 66 D7           RORZ  ALOW
00A9 66 D8           RORZ  ADATA
00AB 88              DEY
00AC D0 F7           BNE   AMOVE

00AE 68              PLA          RESTORE X
00AF AA              TAX
00B0 CA              DEX
00B1 E0 0E           CPXIM $0E    DONE?
00B3 B0 DB           BCS   ALOOP  NO
00B5 90 C9           BCC   AIM    YES. REPEAT

00B7 20 86 8B SYM    JSR   ACCESS ENABLE SYM MOEMORY
00BA A5 D2           LDAZ  POINTH.
00BC 20 FA 82        JSR   OUTBYT OUTPUT
00BF A5 D1           LDAZ  POINTL
00C1 20 FA 82        JSR   OUTBYT
00C4 A0 00           LDYIM $00
00C6 B1 D1           LDAIY POINTL GET DATA
00C8 20 FA 82        JSR   OUTBYT

00CB 20 06 89 DISPLY JSR   SCANDS SCAN DISPLAY
00CE 4C CB 00        JMP   DISPLY CONTINUE

00D1 00       POINTL =     $00
00D2 00       POINTH =     $00
00D3 00       FLAG   =     $00
00D4 00       FLIP   =     $00
00D5 00       PASS   =     $00
00D6 00       AHIGH  =     $00
00D7 00       ALOW   =     $00
00D8 00       ADATA  =     $00
```

EPROM Programming Program

1. Set up the jumpers for the type of EPROM to be programmed according to the following table:





2. Place the EPROM into the EPROM Programming Socket. The notch on the top of the EPROM should be toward the center of the DRAM PLUS board.

3. Load the data to be copied into any memory. This may be RAM on the DRAM PLUS, EPROM on the DRAM PLUS, or any other memory in your system.

4. Load the EPROM Programming Program into your microcomputer from the cassette tape provided. See Page 10 for tape loading instructions.

5. The program assumes that the VIAs on the DRAM PLUS are set for 7000 and 7800. If you have the VIAs addressed somewhere else, then change the addresses in **VTABLE**, at locations 031B to 031E, to point to the VIAs as addressed in your configuration. Refer to the listing for the address information.

6. Remove any devices that you have connected to the VIAs.

7. Set up the programming parameters as follows:

0000	Start Address of data to be copied, Low
0001	Start Address of data to be copied, High
0002	Start Address of EPROM area to be copied to, Low
0003	Start Address of EPROM area to be copied to, High
0004	End Address of data to be copied, +1, Low
0005	End Address of data to be copied, +1, High

For example, to copy memory from 2000 through and including 2345, into the EPROM starting at relative address 0100, the parameters would be set:

0000	00	20**00**	Data Start at 2000
0001	20	**20**00	
0002	00	01**00**	EPROM Start at 0100
0003	01	**01**00	
0004	46	23**46**	Data End at 2345 [2345 + 1 = 2346]
0005	23	**23**46	

6. Turn on the +27 volts.

7. Start the EPROM Programming Program at **0200** for a **2516, 2716** or **2732.**
Start the EPROM Programming Program at **0208** for a **2532.**

8. EPROM Programmer Exits:

Programming Successful: Address **02Fx** , where x varies between the AIM, SYM, and KIM, indicates that the program ran successfully to completion.

Verify Error: Address **02Dx** , where x varies between AIM, SYM, and KIM, indicates that the EPROM did not program correctly. The address that contains the failure is shown by the contents of 0002/0003 which points to the current EPROM address. If the failure is on the first location to be programmed, then check that your EPROM was properly erased to all ones to start; that your programming voltage +27 or above is properly connected; that the EPROM is firmly and properly in the socket; that the select jumpers are in the proper position for the type of EPROM; that the VIAs are selected at 7000 and 7800; and that there are no external connections to the VIAs.

Start Address Error: Address **02Ex** indicates that the Start Address wrapped around from FFFF to 0000. This indicates either a bad starting address or an ending address which is lower than the starting address. Check your parameters in locations 0000 to 0005.

EPROM Address Error: Address **030x** indicates that the EPROM Address wrapped around from FFFF to 0000. This indicates either a bad EPROM Address or a bad ending address. Check your parameters.

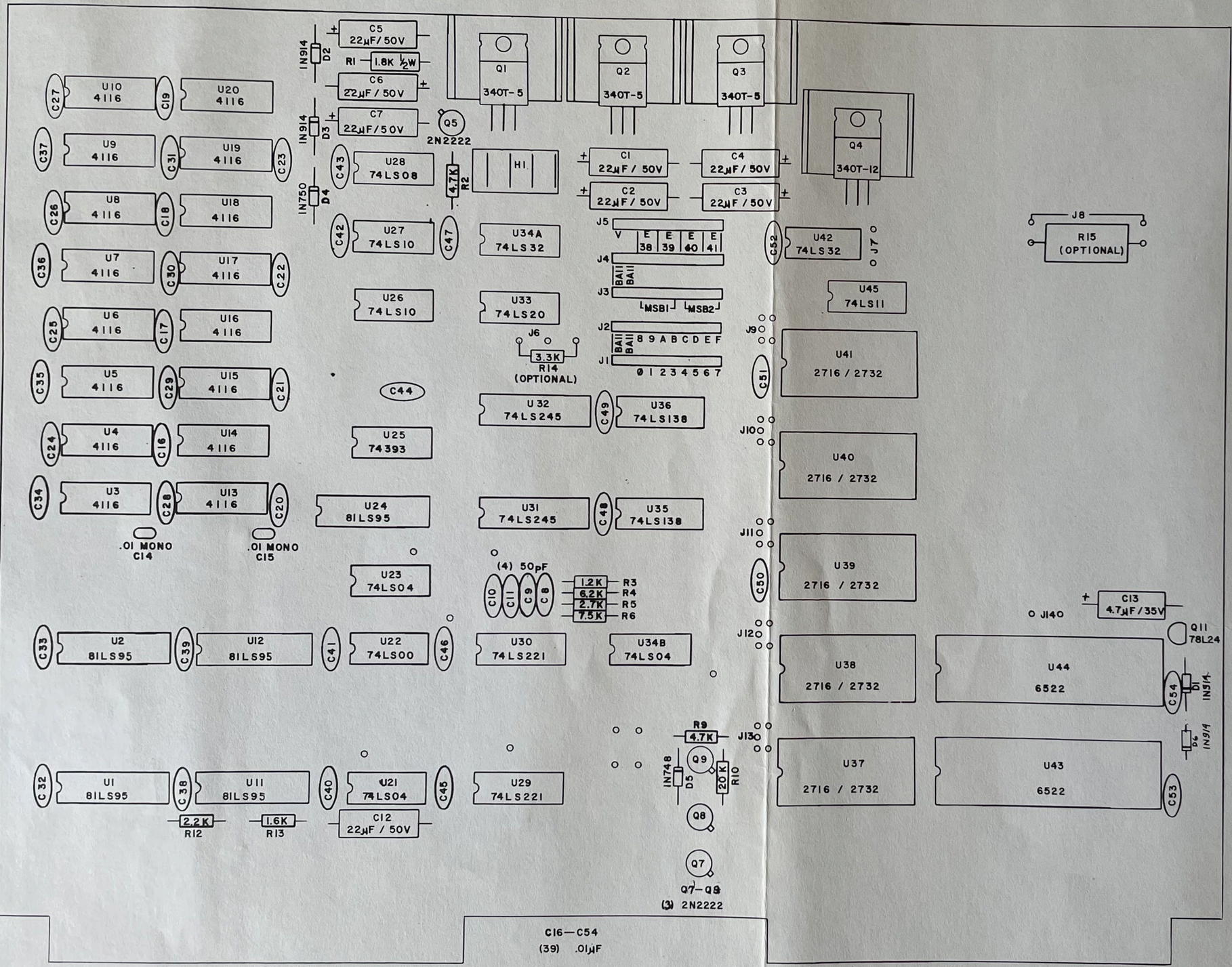
9. Remove the EPROM from the Programming Socket. First remove the +27 volt supply. Then remove the EPROM. The EPROM is now programmed and verified. It may be placed into one of the EPROM sockets and run. That's all there is to it.

```
0010:                   DRAM PLUS (TM) EPROM PROGRAMMER
0020:                     13 APRIL 1980
0030:                   COPYRIGHT (C) BY:
0040:                     THE COMPUTERIST, INC.
0050:                     34 CHELMSFORD STREET
0060:                     CHELMSFORD, MA 01824
0070:                      617/256-3649
0080:
0090:                   WRITTEN BY: ROBERT M. TRIPP
0100:
0110:                   WILL RUN ON AIM, SYM, OR KIM
0120:                   PROGRAMS 2516, 2716, 2532 AND 2732 EPROMS
0130:
0140:                   VIA REGISTER OFFSETS
0150:
0160: 032C              ORB     *       $0000   OUTPUT REGISTER B
0170: 032C              ORA     *       $0001   OUTPUT REGISTER A
0180: 032C              DDRB    *       $0002   DATA DIRECTION REGISTER B
0190: 032C              DDRA    *       $0003   DATA DIRECTION REGISTER A
0200: 032C              TTWOL   *       $0008   TIMER TWO LOW
0210: 032C              TTWOH   *       $0009   TIMER TWO HIGH
0220: 032C              PCR     *       $000C   PERIPHERAL CONTROL REGISTER
0230: 032C              IFR     *       $000D   INTERRUPT FLAG REGISTER
0240: 032C              IER     *       $000E   INTERRUPT ENABLE REGISTER
0250:
0260: 032C              ACCESS  *       $8B86   SYM 1 ACCESS ENTRY
0270:
0280: 032C              SAL     *       $0000   STARTING ADDRESS LOW
0290: 032C              SAH     *       $0001   STARTING ADDRESS HIGH
0300: 032C              PRMLOW  *       $0002   EPROM ADDRESS LOW
0310: 032C              PRMHGH  *       $0003   EPROM ADDRESS HIGH
0320: 032C              EAL     *       $0004   END ADDRESS LOW
0330: 032C              EAH     *       $0005   END ADDRESS HIGH
0340: 032C              VIA     *       $0006   POINTER TO VIA A
0350: 032C              VIB     *       $0008   POINTER TO VIA B
0360: 032C              MONTOR  *       $000A   SYSTEM MONITOR
0370: 032C              INTVEC  *       $000C   SYSTEM INTERRUPT VECTOR
0380: 032C              TMP     *       $000E   TEMPORARY POINTERS
0390: 032C              PGM     *       $0010   PROGRAM BIT PATTERN
0400: 032C              ELEVEN  *       $0011   ADDRESS 11 BIT PATTERN
0410: 032C              TYPE    *       $0012   2716 OR 2732 = CC, 2532 = EC
0420:
0430: 0200                      ORG     $0200   PROGRAM
0440:
0450:                   ENTRY POINT FOR INTEL 2716 OR 2732. ALSO TI 2516.
0460:
0470: 0200 A0 20        INTEL   LDYIM $20       CB2 WILL CONTROL A 11
0480: 0202 A2 02                LDXIM $02       CA2 WILL CONTROL PROGRAMMING
0490: 0204 A9 CC                LDAIM $CC       SET TYPE = CC FOR 27XX
0500: 0206 D0 06                BNE   SETUP     ALWAYS
0510:
0520:                   ENTRY POINT FOR TI 2532 TYPE EPROMS
0530:
0540: 0208 A0 02        TI      LDYIM $02       CA2 WILL CONTROL A 11
0550: 020A A2 20                LDXIM $20       CB2 WILL CONTROL PROGRAMMING
0560: 020C A9 EC                LDAIM $EC       SET TYPE EC FOR 2532
```

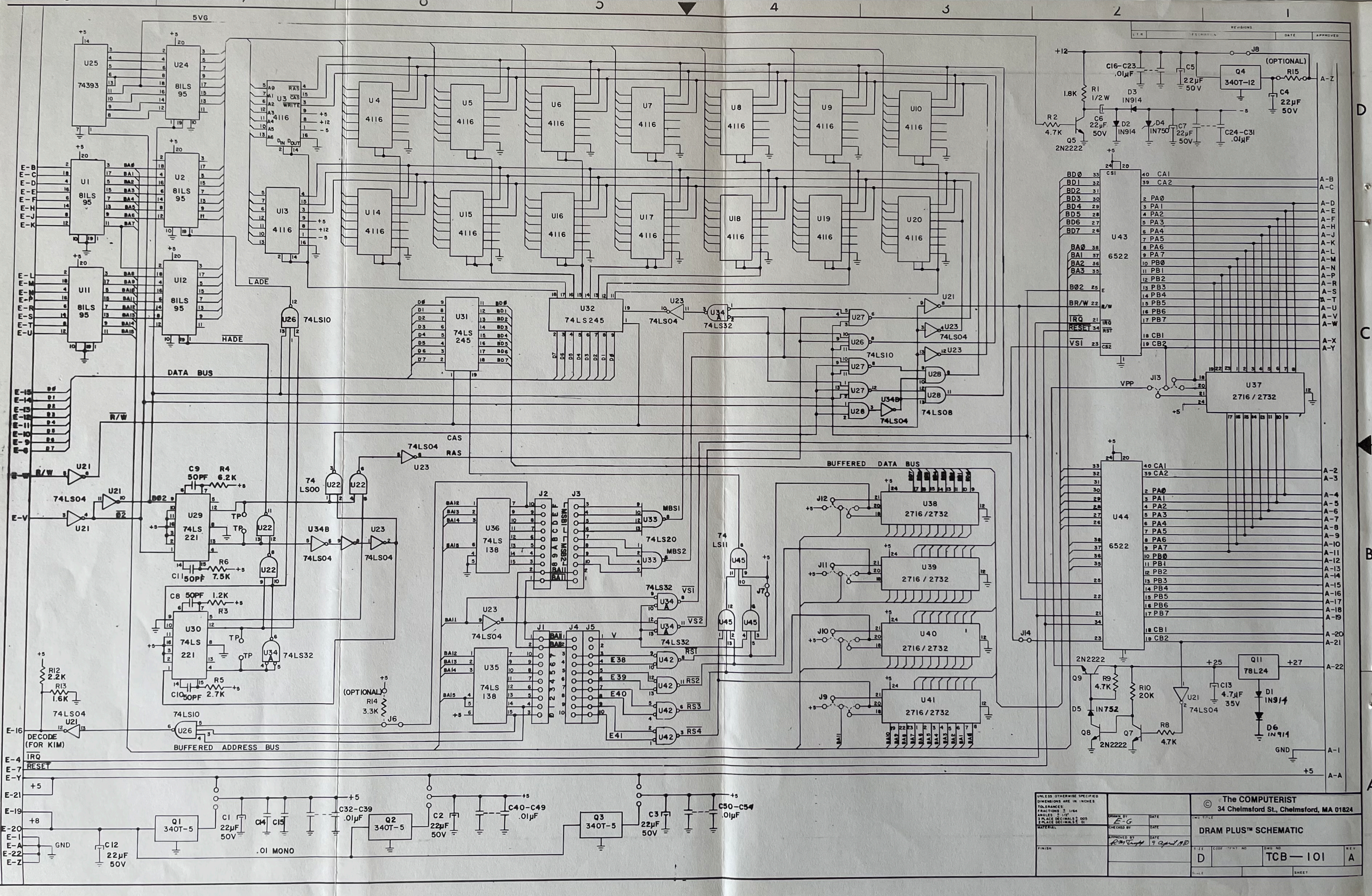
```
0570:
0580: 020E 84 11      SETUP  STY   ELEVEN SAVE A11 PATTERN
0590: 0210 86 10             STX   PGM    SAVE PROGRAMMING PATTERN
0600: 0212 85 12             STA   TYPE   SAVE TYPE INFORMATION
0610: 0214 A0 03             LDYIM $03    MOVE VIA POINTERS
0620: 0216 B9 1B 03  VLOOP   LDAY  VTABLE
0630: 0219 99 06 00          STAY  VIA
0640: 021C 88                DEY
0650: 021D 10 F7             BPL   VLOOP
0660:
0670: 021F A9 00      SPECAL LDAIM $00    CLEAR ALL STATUS FLAGS
0680: 0221 48                PHA          PUTTING 00 ON STACK AND THEN
0690: 0222 28                PLP          PULLING BACK AS STATUS
0700: 0223 A2 13             LDXIM STABLE ASSUME SYM
0710: 0225 AD FD FF          LDA   $FFFD  TEST HIGH BYTE OF INTERRUPT VECTOR
0720: 0228 C9 8B             CMPIM $8B    TO TEST AIM, SYM, OR KIM
0730: 022A F0 0A             BEQ   SYM    8B = SYM
0740: 022C A2 0F             LDXIM ATABLE ASSUME AIM
0750: 022E C9 E0             CMPIM $E0
0760: 0230 F0 07             BEQ   MOVE   E0 = AIM
0770: 0232 A2 17             LDXIM KTABLE ASSUME KIM
0780: 0234 D0 03             BNE   MOVE   ALWAYS
0790: 0236 20 86 8B  SYM     JSR   ACCESS SYM REQUIRES ACCESS CALL
0800:
0810: 0239 86 0E      MOVE   STX   TMP    POINTER
0820: 023B A9 03             LDAIM ATABLE / PAGE
0830: 023D 85 0F             STA   TMP    +01
0840: 023F A0 03             LDYIM $03    POINTER/COUNTER
0850: 0241 B1 0E      MOVEX  LDAIY TMP    GET TABLE VALUE
0860: 0243 99 0A 00          STAY  MONTOR PUT TO WORKING AREA
0870: 0246 88                DEY
0880: 0247 10 F8             BPL   MOVEX  UNTIL Y = FF
0890: 0249 A0 00             LDYIM $00    ENTRY IF TABLE PRESET
0900: 024B A9 1F             LDAIM INTRPT GET INTERRUPT POINTER
0910: 024D 91 0C             STAIY INTVEC SETUP VIA TABLE
0920: 024F A9 03             LDAIM INTRPT / GET PAGE
0930: 0251 C8                INY          BUMP POINTER
0940: 0252 91 0C             STAIY INTVEC
0950: 0254 A0 0E             LDYIM IER    DISABLE ALL INTERRUPTS
0960: 0256 A9 7F             LDAIM $7F    ON BOTH VIAS
0970: 0258 91 06             STAIY VIA
0980: 025A 91 08             STAIY VIB
0990: 025C A0 0D             LDYIM IFR
1000: 025E A9 FF             LDAIM $FF    CLEAR ANY PENDING INTERRUPTS
1010: 0260 91 06             STAIY VIA
1020: 0262 91 08             STAIY VIB
1030: 0264 A0 0E             LDYIM IER
1040: 0266 A9 A0             LDAIM $A0    ENABLE TIMER TWO
1050: 0268 91 06             STAIY VIA
1060:
1070: 026A A2 00      NEXT   LDXIM $00    INIT X REGISTER
1080: 026C A0 0C             LDYIM PCR    TURN POWER ON
1090: 026E A5 12             LDA   TYPE   SET NOT CS, NOT PROGRAM
1100: 0270 91 06             STAIY VIA
1110: 0272 A9 CC             LDAIM $CC    TURN ON +25VOLTS
1120: 0274 91 08             STAIY VIB    CONTROLLED BY VIB
```

```
1130: 0276 A9 FF            LDAIM $FF    SET DATA FOR OUTPUT
1140: 0278 A0 02            LDYIM DDRB
1150: 027A 91 06            STAIY VIA    HIGH ADDRESS: VIA PORT B
1160: 027C A0 03            LDYIM DDRA
1170: 027E 91 06            STAIY VIA    LOW ADDRESS: VIA PORT A
1180: 0280 91 08            STAIY VIB    DATA: VIB PORT A
1190: 0282 A0 01            LDYIM ORA
1200: 0284 A5 02            LDA   PRMLOW OUTPUT NEXT ADDRESS
1210: 0286 91 06            STAIY VIA    LOW 8 BITS
1220: 0288 A0 00            LDYIM ORB
1230: 028A A5 03            LDA   PRMHGH
1240: 028C 91 06            STAIY VIA    HIGH 3 OR 4 BITS
1250: 028E A1 00            LDAIX SAL    GET DATA BYTE
1260: 0290 A0 01            LDYIM ORA
1270: 0292 91 08            STAIY VIB    OUTPUT DATA: VIB PORT A
1280:
1290: 0294 A9 50     TIMER  LDAIM $50    SETUP 50 MILLISECOND TIMER
1300: 0296 A0 08            LDYIM TTWOL
1310: 0298 91 06            STAIY VIA    OUTPUT TO TIMER TWO LOW
1320: 029A A9 C3            LDAIM $C3    OUTPUT HIGH BYTE OF TIME
1330: 029C A0 09            LDYIM TTWOH  TO TIMER TWO HIGH
1340: 029E 91 06            STAIY VIA
1350: 02A0 A5 12            LDA   TYPE   ASSUME A11 IS OFF
1360: 02A2 A4 03            LDY   PRMHGH TEST TO SEE IF REALLY OFF
1370: 02A4 C0 08            CPYIM $08
1380: 02A6 30 02            BMI   TIMEX  YES IT IS OFF.
1390: 02A8 05 11            ORA   ELEVEN A11 ON. TURN ON BIT
1400:
1410: 02AA A0 0C     TIMEX  LDYIM PCR    TURN ON A11 IF REQUIRED
1420: 02AC 91 06            STAIY VIA
1430: 02AE 45 10            EOR   PGM    TOGGLE TO TURN ON PROGRAM PULSE
1440: 02B0 91 06            STAIY VIA
1450:
1460: 02B2 C0 0C     WAIT   CPYIM PCR    TEST FOR INTERRUPT SERVICED
1470: 02B4 F0 FC            BEQ   WAIT   WAIT FOR Y TO CHANGE
1480:
1490: 02B6 A0 0C     VERIFY LDYIM PCR    TURN OFF +25 VOLT POWER
1500: 02B8 A9 EC            LDAIM $EC    LEAVE +5 VOLTS ON
1510: 02BA 91 08            STAIY VIB
1520: 02BC A0 64            LDYIM $64    DELAY TO PERMIT THE +25V
1530: 02BE 88        DELAY  DEY          TO SETTLE DOWN TO +5 FOR
1540: 02BF D0 FD            BNE   DELAY  THE VERIFY TESTS
1550: 02C1 A0 0C            LDYIM PCR    TEST FOR 2532 AND IF YES,
1560: 02C3 A5 10            LDA   PGM    TURN PROGRAMMING PULSE OFF FOR
1570: 02C5 C9 20            CMPIM $20    VERIFYING
1580: 02C7 D0 04            BNE   VTEST  2716/2732/2516 ARE OKAY
1590: 02C9 51 06            EORIY VIA    2532 GETS TURNED OFF HERE
1600: 02CB 91 06            STAIY VIA    FOR VERIFY MODE
1610:
1620: 02CD A9 00     VTEST  LDAIM $00    VERIFY PROGRAMMING
1630: 02CF A0 03            LDYIM DDRA   SET ORA FOR INPUT
1640: 02D1 91 08            STAIY VIB    VIB PORT A
1650: 02D3 A0 01            LDYIM ORA    SETUP POINTER
1660: 02D5 B1 08            LDAIY VIB
1670: 02D7 C1 00            CMPIX SAL    COMPARE ORIGINAL DATA
1680: 02D9 F0 03            BEQ   OKAY   GOOD IF MATCH
```

```
1690: 02DB 20 06 03          JSR   JMPMON EXIT ON ERROR
1700:
1710: 02DE E6 00     OKAY    INC   SAL    BUMP DATA POINTER
1720: 02E0 D0 07             BNE   TEST   BRANCH IF NOT ZERO
1730: 02E2 E6 01             INC   SAH    BUMP HIGH DATA POINTER
1740: 02E4 D0 03             BNE   TEST   BRANCH IF NOT ZERO
1750: 02E6 20 06 03          JSR   JMPMON EXIT ON MEMORY WRAP-AROUND
1760:
1770: 02E9 A5 05     TEST    LDA   EAH    TEST END OF PROGRAMMING
1780: 02EB C5 01             CMP   SAH    BY COMPARING POINTERS
1790: 02ED D0 09             BNE   MORE
1800: 02EF A5 04             LDA   EAL
1810: 02F1 C5 00             CMP   SAL
1820: 02F3 D0 03             BNE   MORE
1830: 02F5 20 06 03          JSR   JMPMON DONE
1840:
1850: 02F8 E6 02     MORE    INC   PRMLOW BUMP PROM POINTERS
1860: 02FA D0 07             BNE   LOOP   READY IF NOT ZERO
1870: 02FC E6 03             INC   PRMHGH BUMP HIGH POINTER
1880: 02FE D0 03             BNE   LOOP   OKAY IF NOT ZERO
1890: 0300 20 06 03          JSR   JMPMON EXIT ON MEMORY WRAP-AROUND
1900:
1910: 0303 4C 6A 02  LOOP    JMP   NEXT
1920:
1930: 0306 A0 0C     JMPMON  LDYIM PCR    TURN OFF POWER
1940: 0308 A9 EE             LDAIM $EE
1950: 030A 91 08             STAIY VIB    BOTH +25 AND +5 VOLTS
1960: 030C 6C 0A 00          JMI   MONTOR RETURN TO MONITOR
1970:
1980: 030F 6D        ATABLE  =     $6D    AIM 65 MONITOR ENTRY
1990: 0310 E1                =     $E1
2000: 0311 00                =     $00    IRQ INTERRUPT VECTOR
2010: 0312 A4                =     $A4
2020:
2030: 0313 35        STABLE  =     $35    SYM MONITOR ENTRY
2040: 0314 80                =     $80
2050: 0315 7E                =     $7E    IRQ INTERRUPT VECTOR
2060: 0316 A6                =     $A6
2070:
2080: 0317 05        KTABLE  =     $05    KIM MONITOR ENTRY
2090: 0318 1C                =     $1C
2100: 0319 FE                =     $FE    IRQ INTERRUPT VECTOR
2110: 031A 17                =     $17
2120:
2130: 031B 00        VTABLE  =     $00    POINTER TO VIA
2140: 031C 70                =     $70
2150: 031D 00                =     $00    POINTER TO VIB
2160: 031E 78                =     $78
2170:
2180: 031F B1 06     INTRPT  LDAIY VIA    GET PCR
2190: 0321 45 10             EOR   PGM    TURN OFF PROGRAM PULSE
2200: 0323 91 06             STAIY VIA
2210: 0325 A0 0D             LDYIM IFR    SETUP TO CLEAR INTERRUPT
2220: 0327 B1 06             LDAIY VIA    READ AND WRITE TO CLEAR
2230: 0329 91 06             STAIY VIA    USING A SNEAKY TRICK
2240: 032B 40                RTI          RETURN FROM INTERRUPT
```



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: FRACTIONS ± 1/64 ANGLES ± 1/2° 3 PLACE DECIMALS ± .005 2 PLACE DECIMALS ± .01 MATERIAL FINISH		© The COMPUTERIST 34 Chelmsford St., Chelmsford, MA 018
	DRAWN BY E-G DATE	DWG TITLE DRAM PLUS™ ASSEMBLY
	CHECKED BY DATE	
	APPROVED BY R.M. Wright DATE 9 April 1980	SIZE D CODE IDENT NO DWG NO TCB-101
		SCALE SHEET



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2 PLACE DECIMALS ± .005
3 PLACE DECIMALS ± .01
MATERIAL
FINISH

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APPROVED BY DATE

DWG TITLE
DRAM PLUS™ SCHEMATIC

SIZE D | CODE IDENT NO | DWG NO TCB—101 | REV A

SCALE | SHEET