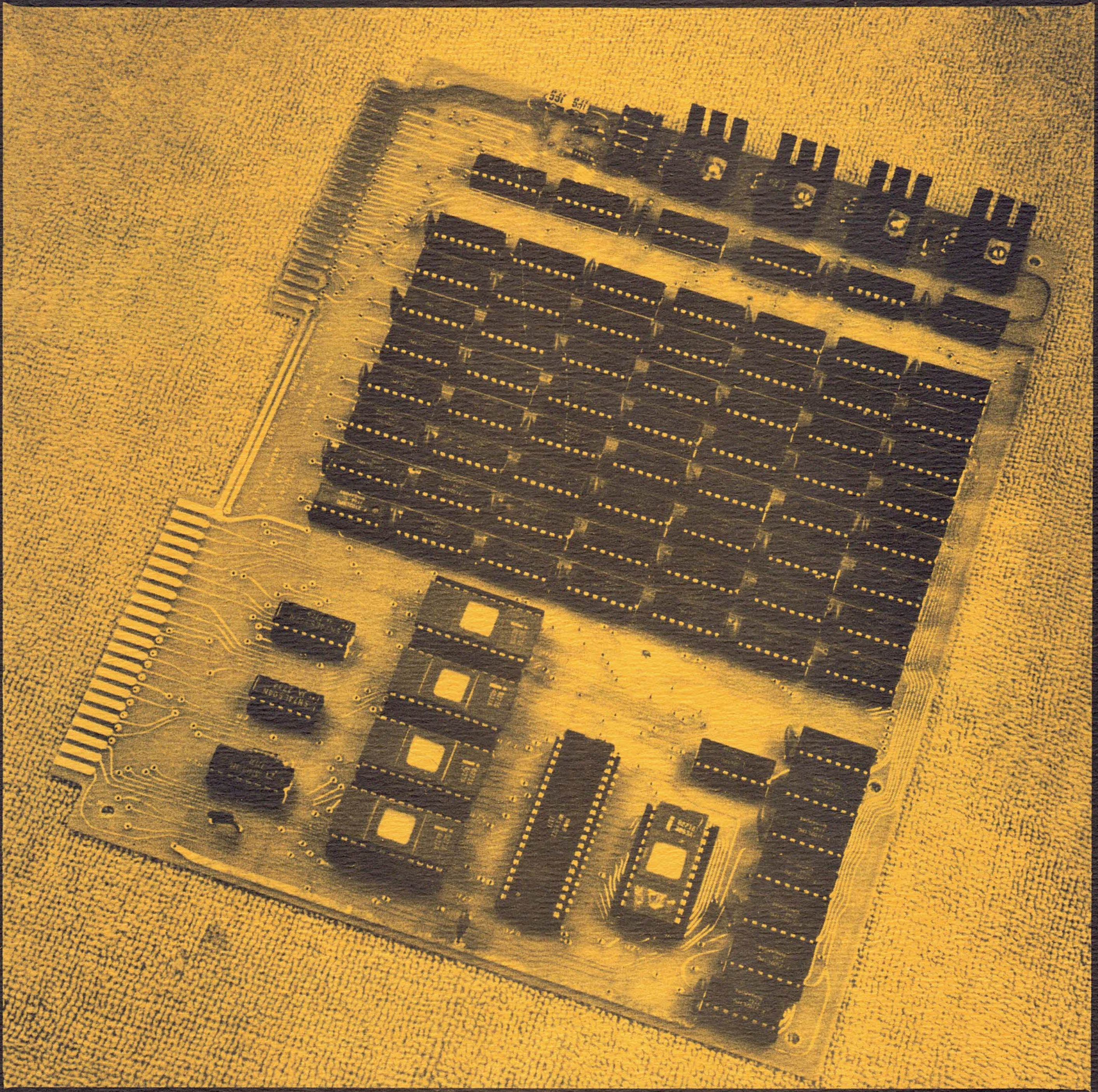
MEMORY PLUS™



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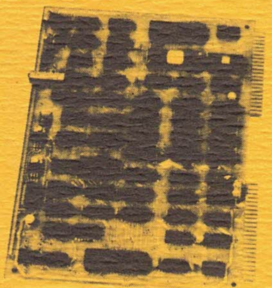

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128 Additional User Programmable Characters: GRAPHICS-SYMBOLS-FOREIGN CHARACTERS
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KEYBOARD and LIGHT PEN Interfaces
Up to 4K DISPLAY RAM
Provision for 2K EPROM
Provision to add 6502 for STAND-ALONE SYSTEM

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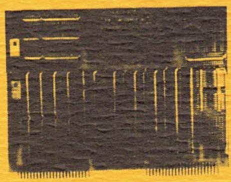
Provisions for 40 14/16 pin sockets
4 24/40 pin sockets
3 voltage regulators



PROTO PLUS: $\$40^{00}$

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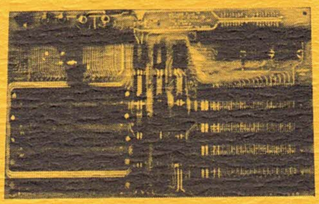


MOTHER PLUS: $\$80^{00}$ FULLY ASSEMBLED AND TESTED

The COMPUTERIST specializes in expansion needs for your **AIM/SYM/KIM**. We offer a wide variety of support in expansion boards, power supplies, and software. Since we are continuously developing new 6502 based products, please contact us for the latest product and pricing information.

Prices subject to change without notice.

The COMPUTERIST, Inc.
P. O. Box 3
So. Chelmsford, MA 01824
617/256-3649

[October 1979]

Table of Contents

Warranty and Service

Should you experience difficulty with your MEMORY PLUS board and be unable to diagnose or correct the problem, you may return the board to The COMPUTERIST for repair. MEMORY PLUS is warranted by The COMPUTERIST against defects in workmanship and materials for a period of ninety (90) days from date of delivery. During the warranty period, The COMPUTERIST will repair or, at its option, replace at no charge components that prove to be defective provided that the board is returned, shipping prepaid, to:

The COMPUTERIST, Inc.
Service Department
34 Chelmsford Street
Chelmsford, MA 01824

This warranty does not apply if the board has been damaged by accident or misuse, or as a result of repairs or modification made by other than authorized personnel at the above service facility. No other warranty is expressed or implied. The COMPUTERIST is not liable for consequential damages.

Beyond the ninety (90) day warranty period, MEMORY PLUS boards will be repaired for a reasonable service fee. All service work performed by The COMPUTERIST beyond the warranty period is warranted for an additional ninety (90) day period after shipment of the repaired board.

It is the customer's responsibility to return the board with shipping charges prepaid to the above service facility. For in-warranty service, the board will be returned to the customer, shipping prepaid, by the fastest economical carrier. For out-of-warranty service, the customer will pay for shipping charges both ways. The repaired board will be returned to the customer C.O.D. unless the repairs and shipping charges are prepaid by the customer.

INTRODUCTION

MEMORY PLUS^{tm} has been designed specifically to work with the KIM-1, SYM-1, AIM 65 microcomputers. It greatly extends the power of the basic MICRO by providing four major facilities:

RAM Memory: 8K bytes of low power 2102 type static RAM.

ROM Memory: Sockets and decoding for up to 8K bytes of 2716 type erasable programmable read-only memory - EPROM

Versatile Interface Adapter: Two 8-bit programmable I/O ports with additional handshaking lines. Two sophisticated timers. A serial-to-parallel and parallel-to-serial shift register.

EPROM Programmer: All components required to programming the INTEL type 2716 EPROM. This includes a programming socket, all hardware, a +25 volt regulator circuit, and an EPROM Programming program on cassette tape.

Other features of MEMORY PLUS include:

On board +5 volt regulators: User need only supply +8 to +10 unregulated power for running everything on MEMORY PLUS except the EPROM Programmer.

Provision for Battery Backup: External batteries may be connected to MEMORY PLUS to maintain power to the RAMs during any power outage, thereby automatically preserving the contents of the RAM.

All ICs are socketted: This means that in the event of a chip failure in the field the user may often be able to correct the problem immediately and locally, and not be required to ship the board back to the factory for service.

May be mounted directly underneath the KIM-1 or SYM-1. Mounting holes are provided so that the board may be attached to the existing holes on the KIM-1 or SYM-1.

Compatible with the KIM-4 Bus: The basic connections between the MICRO and MEMORY PLUS are identical to those between the KIM-1 and KIM-2/KIM-3. Therefore, users who have already designed and/or built systems based on these KIM boards may easily adapt to the MEMORY PLUS board.

Provision for Off-the-board EPROM Programming Socket: All of the lines necessary to add an external EPROM Programming Socket are available at the MEMORY PLUS application connector.

Fully Assembled, Burned-in, and Tested: Ready to go.

Switch Selectable Addressing: Starting address for RAM and ROM are set by rotary switches on the board. They may each start at any 8K boundary (2K hex).

Set Up and Check Out

The quickest way to get your new MEMORY PLUS board "up and running" with your MICRO is to take your time and follow all of the steps outlined below.

1. Carefully unpack your MEMORY PLUS board from its individual box, padding, and protective anti-static wrapping. While none of the components on this board are unusually susceptible to static, any chip can be damaged (destroyed) by a large static shock. So, take some care about avoiding static buildup.

2. Examine the board for any visible damage which may have occurred in shipping. Push all IC's firmly into their sockets. Unbend any capacitors which have been bent.

3. Read briefly the entire MEMORY PLUS manual. Pay particular attention to the main sections on "POWER", "RAM Memory", "EPROM Memory", and "VERSATILE INTERFACE ADAPTER", but do not try to memorize everything.

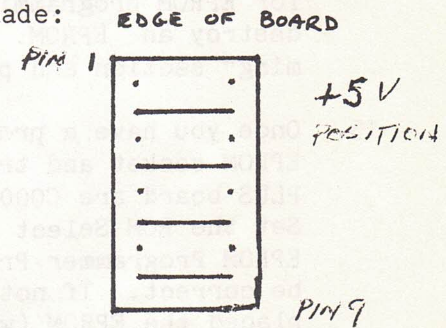
4. Build the required connector cables following the wiring list labelled "MEMORY PLUS to MICRO Connections".

4A <u>KIM-1 ONLY</u>; If you are only planning to use the RAM memory to start, then only the expansion connector cable is required. A wire running from pin E-16 of MP to A-K of KIM for the DECODE. Remember to remove the wire you currently have between pin A-K of KIM and pin A-1 of KIM which grounds the DECODE signal for an unexpanded system.

5. Carefully check the cable you built for any errors or bad connections.

6. Set up your power for MEMORY PLUS in one of the following ways:

   a. If you have a single +5V supply which is going to run both the MICRO and MEMORY PLUS (it must be capable of about 3.5 amps), then the following connections should be made:



      MP E-21 to MICRO E-21
      MP E-Y to MICRO E-21
      MP A-A to MICRO A-A

   The Header should be positioned with no wire near the edge of the board.

   b. If you have a separate +5 regulated supply for MEMORY PLUS, the above connections must not be made. The header should be positioned with no wire near the edge of the board. Attach supply to MP E-21/E-Y.

   c. If you have a +8 to +10 unregulated supply, then the above connections must not be made. The header should be positioned with a wire near the edge of the board. Attach supply to MP E-19/E-20.

7. Connect the MICRO and MEMORY PLUS together via the cables you have made.

8. Set the RAM Select Switch to the 2000 position.

9. Turn on the power supply. Using the MICRO monitor, examine and modify a few RAM locations to verify that they basically work. With the RAM switch set to 2000, locations 2000 through 3FFF are accessible. If you are unable to examine and modify these locations, then check steps 2 to 8 for any errors. If you can not find anything you did wrong, then go to the section on "MEMORY PLUS Testing and Field Repair" on page 16.

10. If the above preliminary examination of RAM memory is successful, then you are ready to run a more rigorous memory test. Follow the instructions in the section on "RAM Memory Test". If these tests work, and all you plan to use on MEMORY PLUS is the RAM, then you are done with the initial set up and check out.

11. If you plan to use the EPROM Programmer, you must build the cable that goes between the MICRO and MEMORY PLUS application connectors if you have not already done so. Follow the wiring list labelled "MEMORY PLUS to MICRO Connections". Carefully check the cable you built and review the power connections as discussed in step 6 above.

12. Connect the MICRO and MEMORY PLUS together with the application cable.

13. No specific tests are provided for testing the VIA. If you wish to test this chip, read the section on "VERSATILE INTERFACE ADAPTER" and the "MCS6522 VERSATILE INTERFACE ADAPTER - Data Sheet" contained in your MICRO Manual. You may then devise your own tests dependent on how you intend to use the VIA chip.

14. The only simple way to test the EPROM Programmer is to program an EPROM. The EPROM Programmer requires a +25 volts at 30 milliamps. The best way to provide this is by using the on board regulator circuit. A +27 to +30V unregulated supply can be connected to pin E-3 of the MEMORY PLUS expansion connector. See the section on "EPROM Programming" for details. This will provide about +24.7V for EPROM programming and will prevent over voltages which can destroy an EPROM. Follow the instructions in the "EPROM Programming" section and program an EPROM.

15. Once you have a programmed EPROM, you can place it into the correct EPROM socket and try to use it. The "standard" addresses for the MEMORY PLUS board are C000 - C7FF, C800 - CFFF, D000 - D7FF, and D800 - DFFF. Set the ROM Select Switch to the desired 8K starting address. Since the EPROM Programmer Program verified as it programmed, the contents should be correct. If not, then there is probably a problem in where you have placed the EPROM (wrong socket) or which direction you have inserted the EPROM (pin 1 goes upper right corner). If the contents of the EPROM look okay, then execute the code to determine if it runs correctly. If the code looks correct, then it should run properly.

16. Congratulations. You now have an expanded MICRO system with a lot of new capabilities. You should now make yourself more familiar with the MEMORY PLUS facilities by re-reading the documentation, particularly the VIA Data Sheet.

4

MEMORY PLUS to MICRO Connections

Expansion Connector

Function	MEMORY PLUS Pin#	MICRO Pin#	Function	MEMORY PLUS Pin#	MICRO Pin#
Ground	E-1	E-22	Ground	E-A	E-22
* +5V Battery	E-2		AB0	E-B	E-A
* +27 Unreg.	E-3	groen/wit	AB1	E-C	E-B
$\overline{IRQ}$	E-4	E-4	AB2	E-D	E-C
	E-5		AB3	E-E	E-D
	E-6		AB4	E-F	E-E
$\overline{RST}$	E-7	E-7	AB5	E-H	E-F
DB7	E-8	E-8	AB6	E-J	E-H
DB6	E-9	E-9	AB7	E-K	E-J
DB5	E-10	E-10	AB8	E-L	E-K
DB4	E-11	E-11	AB9	E-M	E-L
DB3	E-12	E-12	AB10	E-N	E-M
DB2	E-13	E-13	AB11	E-P	E-N
DB1	E-14	E-14	AB12	E-R	E-P
DB0	E-15	E-15	AB13	E-S	E-R
DECODE	E-16	A-K *	AB14	E-T	E-S
	E-17		AB15	E-U	E-T
	E-18		Phase 2	E-V	E-U
+8V Unreg.	E-19	Blauw	Read/Write	E-W	E-V
+8V Unreg.	E-20		$\overline{\text{Phase 2}}$	E-X	E-Y
+5V Regulated	E-21	E-21 Rood	+5V Regulated	E-Y	E-21
Ground	E-22	E-22 Zwart	Ground	E-Z	E-22

Application Connector

Function	MEMORY PLUS Pin#	MICRO Pin#	Function	MEMORY PLUS Pin#	MICRO Pin#
Ground	A-1	A-1	+5V Regulated	A-A	A-A
MPA1	A-2		MPB6	A-B	
MPA2	A-3			A-C	
MPA3	A-4			A-D	
MPA4	A-5		MCA2	A-E	
MPA5	A-6		MCA1	A-F	
MPA6	A-7		MCB1	A-H	
MPA7	A-8		MCB2	A-J	*
MPB0	A-9		DECODE	A-K	A-K
MPB1	A-10			A-L	
MPB2	A-11			A-M	
MPB3	A-12			A-N	
MPB4	A-13			A-P	
MPA0	A-14			A-R	
MPB7	A-15			A-S	
MPB5	A-16			A-T	
MCB2	A-17			A-U	
	A-18			A-V	
PRA8	A-19	A-9		A-W	
PRA9	A-20	A-10		A-X	
PRA10	A-21	A-11		A-Y	
+25V Regulated	A-22			A-Z	

* SEE IMPORTANT WARNING NOTE ON PAGE 18 ABOUT E-2/E-3 CONNECTIONS.

* One of the two DECODE lines must be connected to the KIM-1. This is *not* required on the SYM-1 or AIM 65.

POWER

The power requirements for MEMORY PLUS are simple and on-board regulators are provided to make powering the board even easier. Essentially the board requires only +5 volts at about 2.0 amps. While the actual current requirements will vary slightly with the particular components on any board, the table below shows the individual and collective power requirements.

Component	#	Typical	Maximum	Measured	Max Total	Meas. Total
74LS00	1		8	3	8	3
74LS04	1		8	4	8	4
74LS32	1	5	10	2	10	2
74LS138	3	7	10	6	30	18
74LS367	3	14	24	17	72	51
2716	4	57	105	45	420	180
6522	1	50	[A] 60	52	60	52
2102L [B]	32	14	22	14	704	448
2102L	32	14	22	14	704	448
Total System					2016	1206 [C]

Notes: All current values in milliamps.

[A] Value as estimated by an engineer at MOS Technology.

[B] 2102Ls are split into two sections of 4K RAM each in the table for purposes of discussion below.

[C] Measurements were taken with an inexpensive meter and should be only used as a guide to the system current requirements.

[D] The above values were obtained with Fairchild 21L02s. The values may vary with other 21L02s produced by other manufacturers and supplied with your MEMORY PLUS board.

Regulated +5 Volt Supply. If the MEMORY PLUS is to be powered by regulated +5 volts, then the supply should be connected to pins E-21 and E-Y on the MEMORY PLUS expansion connector. The supply should be capable of supplying at least 2.0 amps in addition to any other board it is driving such as the KIM-1. The Header at the top of the board should be positioned so that the bus wires are away from the top of the board and the Header notched corner is positioned at pin 9.

Unregulated +8 to +10 Volt Supply. If the MEMORY PLUS is to be powered by unregulated +8 to +10 volts, then the supply should be connected to pins E-19 and E-20 on the MEMORY PLUS expansion connector. The supply should be capable of supplying at least 2.5 amps. This supply is distributed to three +5 volt regulators which each handle a separate section of the board.

Regulator Q4 supplies the high 4K of 2102L RAM with 448 to 704 milliamps.
Regulator Q5 supplies all support chips, the 2716s and the 6522 with 310 to 608 milliamps.
Regulator Q6 supplies the low 4K of 2102L RAM with 448 to 704 milliamps.

The Header at the top of the board should be positioned so that the bus wires are near the top of the board and the Header notched corner is positioned at pin 1.

The only other power requirement for the MEMORY PLUS board is +25 volts at 30 milliamps during programming of an EPROM. This voltage may be provided as either regulated +25 volt or unregulated +28 to +30 volts.

Regulated +25 Volt Supply. Programming of the INTEL 2716 EPROM requires +25V. This may be attached to pin A-22 of the MEMORY PLUS application connector. Care must be taken to assure that the voltage is within the limits of +24 to +26 volts. A higher voltage will destroy the EPROM as both the INTEL documentation and my own personal experience can attest.

* Unregulated +27 to +30 Volt Supply. MEMORY PLUS provides a circuit with a +24 volt regulator and a diode to produce a regulated +24.7 volts from an unregulated +27 to +30 volt supply. The unregulated supply, which may be three +9 volt transistor radio type batteries, is attached to pin E-3 of the MEMORY PLUS expansion connector. Since the programming voltage is so critical and since an over voltage can destroy an EPROM, use of this on board regulator is recommended. The three battery clips provided in the Accessory Bag are for the purpose of hooking up three +9 volt batteries.

* Battery Backup. Since it is often desirable to be able to protect the contents of the RAM memory during a transient power interruption, or for longer periods of time, a provision has been made for battery backup to be connected to the MEMORY PLUS board. The batteries must be capable of providing between about 3.5 and 4.5 volts. They are connected to pin E-2 of the MEMORY PLUS expansion connector. There are diodes in the circuit which prevent current from being drawn from the batteries during normal system functioning. When the power drops, however, the batteries will automatically start supplying the required current. The amount of current will depend on the basic system configuration. If the MEMORY PLUS board is being run from +5 volts, then the batteries must supply the entire board. If the board is being run from the +8 to +10 volt regulators, then the battery backup will only run the RAM memory chips. This will result in a lower current drain on the batteries. The length of time that the system will retain its RAM contents on battery power will be a function of the configuration and the capacity of the batteries.

* SEE IMPORTANT WARNING NOTE ON PAGE 18.

Cassette Loading Instructions

The cassette tape is recorded in standard KIM format at the normal rate. The programs have been written so that they will run on a KIM-1, SYM-1 or AIM 65 with no modification.

The MEMORY TEST is the first program on the tape. It has program ID = 10. It loads into locations 0000 through 00D8. It is set up to test memory from 2000 to 3FFF. The starting address of the program is 0002. See pages 21 to 23 of this manual for the MEMORY TEST Source Listing and page 20 for instructions on using the program.

The PROM PROGRAMMER is the second program on the tape. It has Program ID = 20. It loads into locations 0000 through 00E7. The programming parameters must be set up in locations 0000 through 0005 as outlined in the section on EPROM Programming, pages 11 to 13. The starting address of the program is 0011. Complete Source Listings are located on pages 14 through 16 of this manual.

RAM Memory

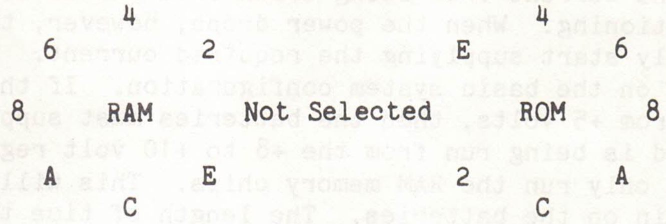
The Random Access Memory (RAM) used with MEMORY PLUS is 2102-type static RAM. Each 2102 chip contains 1024 bits of memory. Any single bit is directly addressable. By addressing eight chips in parallel, an eight bit word is accessed. It takes eight 2102 chips to provide 1024 8-bit bytes. The MEMORY PLUS provides 8K bytes of 8-bit RAM (actually 8192 bytes). This requires 64 2102 chips: eight chips per 1K times eight K.

The 2102 chips used with MEMORY PLUS are Synertek 21L02B or equivalent. This version of 2102 has the following basic parameters:

SPEED: 450 nanosecond access time
POWER: 30 milliamp worst case (these are "low power" chips)
single +5 voltage required

The MEMORY PLUS RAM is organized into a single contiguous 8K block of memory. The location of the RAM in the MICRO addressing space is defined by a switch which may be set to start at any 8K boundary (2K hex boundary). Looking at the board with the regulators at the top, the RAM select switch is the left switch of the pair of rotary switches. Using the flat side of the switch as the position indicator, the addresses are set as follows:

On-board Address Select
Switches for RAM and ROM



The address associated with each position is:

2K	2000 to 3FFF	Assumed as the RAM address in this manual.
4K	4000 to 5FFF	
6K	6000 to 7FFF	
8K	8000 to 9FFF	
AK	A000 to BFFF	
CK	C000 to DFFF	Assumed as the ROM address in this manual.
EK	E000 to FFFF	Not normally used for RAM since interrupt vectors must be defined in FFFA to FFFF if this memory is addressed. See note in EPROM Memory about using this space for EPROM.

The exact layout of the individual RAM chips may be found in a diagram in the section on "MEMORY PLUS Testing and Field Repair".

EPROM Memory

The Erasable Programmable Read-Only Memory (EPROM) used with MEMORY PLUS is an ultraviolet erasable and electrically programmable 2716 type ROM. This is a fairly new memory chip. The version used in MEMORY PLUS is made by INTEL. It is not compatible with the 2716 made by some other manufacturers such as Texas Instruments. It may be second sourced by other manufacturers, but be certain that any EPROM you purchase is at least INTEL 2716 compatible. Each 2716 chip contains 16,384 bits of memory. The addressing of the chip is such that data is accessed eight bits at a time. The organization is 2048 bytes of eight bits each. A single 2716 provides 2K bytes of memory. The MEMORY PLUS board has provision for up to four 2716 chips providing for a maximum of 8K bytes of EPROM.

The 2716 chips required for MEMORY PLUS are INTEL 2716 or equivalent (Texas Instrument 2516 but NOT T. I. 2716). This chip has the following basic parameters:

SPEED:	450 nanosecond access time
POWER:	105 milliamp worst case current, and single +5 volt required

The MEMORY PLUS EPROM is organized into a single contiguous 8K block of memory. The location of the EPROM in the MICRO addressing space is defined by a switch which may be set to start at any 8K boundary (2K hex boundary). See the chart of switch positions on the preceding page. The position is determined by the flat section of the switch.

(KIM 1 ONLY): If, and only if, the "EK" address is used, then the jumper "J1" (located on the top side of component U4) must be changed. The existing jumper etched on the board must be cut and a wire run from the hole nearest the "J" to the hole nearest the "1". This will cause interrupts to be serviced by the FFFx vectors instead of the 1FFx KIM-1 vectors.

The EPROM sockets are addressed such that the socket nearest the edge of the board has the lowest address. The exact layout of the individual EPROM chips may be found in a diagram in the section on "MEMORY PLUS Testing and Field Repair".

VIA Address Selection

There are several ways to address the MEMORY PLUS VIA chip. There is circuitry on the board which will normally address the VIA starting at 6200. This is accomplished by combining the 6000 signal generated by the 74LS138 at U4, pin 12, with address lines A8 and A9 in the 74LS32 at U6. If this address is in conflict with something in your system, it may be changed in several ways. The easiest change is to use any other available (unused) decode signal from the 74LS138 at U4. Simply unsolder the existing wire from pin 12 and attach it to the new pin. In this way you can have the VIA addressed as 2200, 4200, 6200 (which is the way the MEMORY PLUS board is shipped), 8200, A200, or C200. If these other addresses do not solve your problem, then you can provide from an external source a signal at pin L of the Application Connector in place of the signal from U4 discussed above. The U4 wire must be disconnected. The VIA address will be the value of the external signal to pin L, plus 0200. For example, using the K5 signal (1400) from the KIM-1 or SYM-1 will cause the VIA addresses to start at 1600 (1400 + 0200 = 1600). IMPORTANT NOTE: If you do change the VIA address, then locations 0006 and 0007 in the EPROM Programming Program must be changed before using it.

VERSATILE INTERFACE ADAPTER

The 6522 Versatile Interface Adapter is one of the important pluses of MEMORY PLUS. This sophisticated chip has the following basic features:

I/O: Two 8-bit parallel I/O ports with additional handshaking control lines. This more than doubles the basic KIM-1 I/O capabilities.

TIMERS: Two powerful interval timers which have a number of operating modes permitting them to be used as counters, "free-running" timers, "one-shot" timers, and more.

SHIFT REGISTER: Perform serial I/O under control of a timer, the system clock or an external signal. Serial-to-parallel and parallel-to-serial conversions take place within the 6522 without involving the MICRO on a bit-by-bit basis.

INTERRUPTS: The many different devices on the 6522 can cause interrupts to signal the completion of activity. These interrupts can be individually enabled, disabled and tested.

The 6255 chip has two functions on MEMORY PLUS. The first is to provide all of the 6522 capabilities to the user as an extension of the MICRO. The second is to control the EPROM Programmer. The 6522 is the heart of the EPROM Programmer. When the system is being used to program EPROMs, then the 6522, as well as several I/O lines from the basic MICRO, is dedicated to this task. See the section on "EPROM Programming" for details.

The addressing of the 6522 is determined by a +5 signal generated by the MEMORY PLUS board and the AB8 and AB9 address signals. The sixteen internal registers of the 6522 normally have the following addresses and functions:

6200	ORB	Output Register B/Input Register B
6201	ORA	Output Register A/Input Register A With Handshake
6202	DDRB	Data Direction Register B
6203	DDRA	Data Direction Register A
6204	T1C-L	Timer/Counter 1 Low
6205	T1C-H	Timer/Counter 1 High
6206	T1L-L	Timer/Counter 1 Low
6207	T1L-H	Timer/Counter 1 High
6208	T2C-L	Timer/Counter 2 Low
6209	T2C-H	Timer/Counter 2 High
620A	SR	Shift Register
620B	ACR	Auxiliary Control Register
620C	PCR	Peripheral Control Register
620D	IFR	Interrupt Flag Register
620E	IER	Interrupt Enable Register
620F	ORA2	Output Register A/Input Register A Without Handshake

EPROM Programming

The usefulness of the EPROMs on the MEMORY PLUS board is enhanced by the inclusion of on board EPROM programming facilities. The INTEL 2716 EPROM is electrically programmable and ultraviolet light erasable. The user can buy or build an ultraviolet light eraser. MEMORY PLUS provides the parts required for the programming of the EPROMs. These parts consist of the following items:

EPROM Programming Socket: Socket 79 is a 24 pin socket located toward the lower right hand corner of the board. The EPROM to be programmed is placed in this socket.

+25 Volt Regulator: +25 volts is required for programming the 2716. This may be provided directly by the user at pin A-22 of the MEMORY PLUS application connector. Since this voltage is so critical, and since an over voltage can destroy an EPROM, an on board regulator circuit is provided. This will provide about 24.7 volts when supplied with +27 to +30 volts at pin E-3 of the MEMORY PLUS expansion connector. *SEE NOTE ON PAGE 18.

Control Lines: The EPROM requires eleven (11) address lines, eight (8) data lines, and two (2) control lines. All but three of these lines are provided by the MEMORY PLUS VIA 6522. The remaining three lines come from the MICRO port B: PB0, PB1, and PB2.

Timing: EPROM programming requires a 50 millisecond pulse be applied to the EPROM. The VIA 6522 includes a timer which is used for timing this interval.

EPROM Programming Program: The control of the programming is handled by a program run on the MICRO. This program is provided in the form of a source listing in this manual and as a cassette tape included in the MEMORY PLUS package.

The 2716 EPROM may be programmed one location (byte) at a time, or the entire EPROM may be programmed. The steps required to program the EPROM are:

1. With the power off, insert the EPROM to be programmed into the Programming Socket.

2. Turn on the power and load the data to be copied into the EPROM into any portion of memory. This may be RAM memory loaded from cassette (or by hand) or may be another EPROM which is going to be copied.

3. Load the EPROM Programming Program from cassette (or by hand) into memory (locations 0000 to 00D8)

4. Make sure the following application connector connections are in place:
   MICRO A-9 TO MP A-19; MICRO A-10 TO MP A-20; MICRO A-11 TO MP A-21

5. Set up the following parameters for the EPROM Programming Program:

0000 and 0001	Starting address of memory to be copied from.
0002 and 0003	First address in EPROM to be copied to.
0004 and 0005	Last address +1 of memory to be copied from.

For example, to copy from RAM locations 2000 through 217A into the EPROM starting at location 0300, the following values would be set:

0000	00	Low byte of Starting address 2000
0001	20	High byte of Starting address 2000
0002	00	Low byte of First address in EPROM 0300
0003	03	High byte of First address in EPROM 0300
0004	7B	Low byte of Last address +1 217A = 7B
0005	21	High byte of Last address +1 217A

6. Turn on +25 volt supply connected to MP A-22 or unregulated +27 to +30 volt supply connected to MP E-3. SEE NOTE ON PAGE 18.

7. After double checking that all prior steps have been done correctly, start the program at 0011.

8. It will take about 50 milliseconds per location for programming. This means about 100 seconds to program an entire 2K EPROM. When the program is done it will return to the MICRO Monitor with an address which will indicate successful completion of the requested programming. The address value is given in the table in 10. below.

9. Turn off the +25 volt (or +27 to +30 volt) supply and the rest of the power to the system. Then remove the EPROM from the programming socket. The EPROM may now be placed in its operational socket and used.

10. The EPROM Programming Program performs several tests and may exit to the Monitor to indicate an error or successful completion. The address which will be displayed depends on which Monitor/MICRO you are using.

AIM 00B8 KIM 00B9 SYM 00BA	Program ran successfully to completion.
AIM 009E KIM 009F SYM 00A0	A Verify error. The correct data has not been programmed into the EPROM. This may be caused by: An EPROM which was not "clean" (all 1's) to start. A defective EPROM. One or more address lines from the MICRO not properly hooked up or not properly functioning.
AIM 00A9 KIM 00AA SYM 00AB	A Starting address error. The memory address pointer has tried to go beyond location FFFF. This may be caused by: Providing an incorrect Starting address in locations 0000 and 0001. Providing an incorrect Last address in locations 0004 and 0005.
AIM 00C3 KIM 00C4 SYM 00C5	An EPROM address error. The EPROM address pointer has tried to go beyond location FFFF. This may be caused by: Providing an incorrect First address in locations 0002 and 0003. Providing an incorrect Last address in locations 0004 and 0005.

The following connections must be made between the MICRO and the MEMORY PLUS board before any EPROM Programming can take place:

MICRO A-9 to MP A-19	Port B Bit 0 (PB0)	Address Bit 8 for EPROM
MICRO A-10 to MP A-20	Port B Bit 1 (PB1)	Address Bit 9 for EPROM
MICRO A-11 to MP A-21	Port B Bit 2 (PB2)	Address Bit 10 for EPROM

If the MEMORY PLUS board is mounted in its normal position, directly below the MICRO, it may be difficult or impossible to get access to the EPROM socket for programming. There are two ways around this problem.

1. Use a 24 pin header to bring wires directly from the EPROM Programming Socket out to a more accessible location.
2. Attach wires for an additional EPROM Programming Socket directly to the MP application connector. All of the lines necessary for attaching an external EPROM Programming Socket are available:

EPROM Socket	MP Application Connector	Function
1	A-15	Address bit 7 from VIA PB7
2	A-B	Address bit 6 from VIA PB6
3	A-16	Address bit 5 from VIA PB5
4	A-13	Address bit 4 from VIA PB4
5	A-12	Address bit 3 from VIA PB3
6	A-11	Address bit 2 from VIA PB2
7	A-10	Address bit 1 from VIA PB1
8	A-9	Address bit 0 from VIA PB0
9	A-14	Data bit 0 from VIA PA0
10	A-2	Data bit 1 from VIA PA1
11	A-3	Data bit 2 from VIA PA2
12	A-1	Ground
13	A-4	Data bit 3 from VIA PA3
14	A-5	Data bit 4 from VIA PA4
15	A-6	Data bit 5 from VIA PA5
16	A-7	Data bit 6 from VIA PA6
17	A-8	Data bit 7 from VIA PA7
18	A-18	Program Pulse Inverted from VIA CB2
19 (MICRO A-11)	A-21	Address bit 10 from MICRO PB2
20	A-F	Chip Select from VIA CA2
21	A-22	+25V direct or from +27 to +30 regulator
22 (MICRO A-10)	A-20	Address bit 9 from MICRO PB1
23 (MICRO A-9)	A-19	Address bit 8 from MICRO PB0
24 (MICRO A-A)	A-A	+5V regulated

The addressing for the EPROM Socket only consists of eleven (11) bits. This means that addressing for programming purposes runs from 0000 to 07FF, regardless of the actual address that the EPROM will eventually reside at. The high order five (5) bits of EPROM address are totally defined by which socket the EPROM is placed in and where the set of EPROMs are switched to: 2000, 4000,..., E000.

```
                PROM PROGRAMMER  10 FEBRUARY 1979

                PROM    ORG     $0000

                ACCESS *        $8B86  SYM-1 ACCESS ENTRY
                VIA REGISTER OFFSETS

                ORB     *       $0000  OUTPUT REGISTER B
                ORA     *       $0001  OUTPUT REGISTER A
                DDRB    *       $0002  DATA DIRECTION REGISTER B
                DDRA    *       $0003  DATA DIRECTION REGISTER A
                TTWOL   *       $0008  TIMER TWO LOW
                TTWOH   *       $0009  TIMER TWO HIGH
                PCR     *       $000C  PERIPHERAL CONTROL REGISTER
                IFR     *       $000D  INTERRUPT FLAG REGISTER
                IER     *       $000E  INTERRUPT ENABLE REGISTER
0000 00         SAL     =       $00    STARTING ADDRESS LOW
0001 00         SAH     =       $00    STARTING ADDRESS HIGH
0002 00         PRMLOW  =       $00    EPROM LOW ADDRESS
0003 00         PRMHGH  =       $00    EPROM HIGH ADDRESS
0004 00         EAL     =       $00    END ADDRESS LOW
0005 00         EAH     =       $00    END ADDRESS HIGH
0006 00         VIA     =       $00    POINTER TO VIA
0007 62                 =       $62    NORMALLY AT 6200
0008 4C         JMPMON  =       $4C    JUMP TO MONITOR
0009 00         MONTOR  =       $00    POINTER TO SYSTEM MONITOR
000A 00                 =       $00    FOR RETURN FROM PROGRAMMER
000B 00         INTVEC  =       $00    POINTER TO INTERRUPT VECTOR
000C 00                 =       $00
000D 00         PBDD    =       $00    PORT B DATA DIRECTION
000E 00                 =       $00
000F 00         PBD     =       $00    PORT B DATA
0010 00                 =       $00

0011 A9 00      BEGIN   LDAIM   $00    CLEAR ALL STATUS FLAGS
0013 48                 PHA
0014 28                 PLP
0015 A2 E0              LDXIM   STABLE ASSUME SYM
0017 AD FD FF           LDA     $FFFD  TEST HIGH BYTE OF INTERRUPT VECTOR
001A C9 8B              CMPIM   $8B    = 8B FOR SYM-1
001C F0 0A              BEQ     SYM
001E A2 D0              LDXIM   ATABLE ASSUME AIM 65
0020 C9 E0              CMPIM   $E0    = E0 FOR AIM 65
0022 F0 07              BEQ     MOVE   IT IS THE AIM
0024 A2 D8      KIM     LDXIM   KTABLE ASSUME KIM
0026 D0 03              BNE     MOVE
0028 20 86 8B   SYM     JSR     ACCESS SYM REQUIRES ACCESS

002B 86 30      MOVE    STXZ    TABLE  +01 SETUP POINTER
002D A2 07              LDXIM   $07    MOVE 8 BYTES
002F B5 00      TABLE   LDAX    $00    REPLACED BY TABLE
0031 95 09              STAX    MONTOR MOVE TO MONTOR TABLE
0033 CA                 DEX
0034 10 F9              BPL     TABLE  MOVE UNTIL X = FF
```

```
0036 A9 00      ENTER   LDAIM $00     CLEAR ALL STATUS FLAGS
0038 48                 PHA
0039 28                 PLP
003A A0 00              LDYIM $00     ENTRY IF TABLE PRESET
003C A9 C5              LDAIM INTRPT  GET INTERRUPT POINTER
003E 91 0B              STAIY INTVEC  SETUP IN TABLE
0040 A9 00              LDAIM INTRPT  /
0042 C8                 INY           BUMP POINTER
0043 91 0B              STAIY INTVEC
0045 A9 EC              LDAIM $EC     SETUP VIA VALUES
0047 A0 0C              LDYIM PCR
0049 91 06              STAIY VIA
004B A0 0E              LDYIM IER     DISABLE ALL INTERRUPTS
004D A9 7F              LDAIM $7F
004F 91 06              STAIY VIA
0051 A0 0D              LDYIM IFR
0053 A9 FF              LDAIM $FF     CLEAR INTERRUPT PENDING
0055 91 06              STAIY VIA
0057 A0 0E              LDYIM IER
0059 A9 A0              LDAIM $A0     ENABLE TIMER TWO
005B 91 06              STAIY VIA

005D A2 00      NEXT    LDXIM $00     INIT X REGISTER
005F A9 FF              LDAIM $FF     SET DATA DIRECTION
0061 A0 02              LDYIM DDRB
0063 91 06              STAIY VIA
0065 A0 03              LDYIM DDRA
0067 91 06              STAIY VIA
0069 81 0D              STAIX PBDD
006B A5 02              LDA   PRMLOW  OUTPUT NEXT ADDRESS
006D 81 06              STAIX VIA     LOW 8 BITS
006F A5 03              LDA   PRMHGH
0071 81 0F              STAIX PBD     BITS 8, 9, 10
0073 A1 00              LDAIX SAL     GET DATA BYTE
0075 A0 01              LDYIM ORA
0077 91 06              STAIY VIA     OUTPUT VIA ORA

0079 A9 50      TIMER   LDAIM $50     SETUP 50 MILLISECOND TIMER
007B A0 08              LDYIM TTWOL
007D 91 06              STAIY VIA     OUTPUT TO TIMER TWO LOW
007F A9 C3              LDAIM $C3     HIGH BYTE OF TIMER
0081 A0 09              LDYIM TTWOH
0083 91 06              STAIY VIA     OUTPUT TO TIMER TWO HIGH
0085 A9 CE              LDAIM $CE     PROGRAM HIGH, PROGRAM MODE
0087 A0 0C              LDYIM PCR
0089 91 06              STAIY VIA

008B C0 0C      WAIT    CPYIM PCR     TEST FOR INTERRUPT SERVICED
008D F0 FC              BEQ   WAIT    ELSE, WAIT FOR IT

008F A9 00      VERIFY  LDAIM $00     VERIFY PROGRAMMING
0091 A0 03              LDYIM DDRA    SET ORA FOR INPUT
0093 91 06              STAIY VIA
0095 A0 01              LDYIM ORA     SETUP POINTER
0097 B1 06              LDAIY VIA
```

```
0099 C1 00                CMPIX SAL    COMPARE ORIGINAL DATA
009B F0 03                BEQ   OKAY   GOOD IF MATCH
009D 20 08 00             JSR   JMPMON EXIT ON ERROR

00A0 E6 00       OKAY     INC   SAL    BUMP DATA POINTER
00A2 D0 07                BNE   TEST   BRANCH IF NOT ZERO
00A4 E6 01                INC   SAH    BUMP HIGH DATA POINTER
00A6 D0 03                BNE   TEST   BRANCH IF NOT ZERO
00A8 20 08 00             JSR   JMPMON EXIT ON ERROR

00AB A5 05       TEST     LDA   EAH    TEST ALL DONE
00AD C5 01                CMP   SAH    BY COMPARING POINTERS
00AF D0 09                BNE   MORE
00B1 A5 04                LDA   EAL
00B3 C5 00                CMP   SAL
00B5 D0 03                BNE   MORE
00B7 20 08 00             JSR   JMPMON DONE.

00BA E6 02       MORE     INC   PRMLOW BUMP PROM POINTERS
00BC D0 9F                BNE   NEXT   READY IF NOT ZERO
00BE E6 03                INC   PRMHGH BUMP HIGH POINTER
00C0 D0 9B                BNE   NEXT   OKAY IF NOT ZERO
00C2 20 08 00             JSR   JMPMON EXIT ON ERROR

00C5 A9 EC       INTRPT   LDAIM $EC    RESET PROGRAM LOW, VERIFY MODE
00C7 91 06                STAIY VIA
00C9 A0 0D                LDYIM IFR    SETUP TO CLEAR INTERRUPT
00CB B1 06                LDAIY VIA    READ AND WRITE TO CLEAR
00CD 91 06                STAIY VIA    INTERRUPT VIA SNEAKY TRICK
00CF 40                   RTI          RETURN FROM INTERRUPT

00D0 6D          ATABLE   =     $6D    AIM 65 MONITOR ENTRY
00D1 E1                   =     $E1    TO DISPLAY PC COUNTER
00D2 0C                   =     $00    IRQ INTERRUPT VECTOR
00D3 A4                   =     $A4
00D4 02                   =     $02    PBDD
00D5 A0                   =     $A0
00D6 00                   =     $00    PBD
00D7 A0                   =     $A0

00D8 05          KTABLE   =     $05    KIM MONITOR ENTRY
00D9 1C                   =     $1C
00DA FE                   =     $FE    IRQ INTERRUPT POINTER
00DB 17                   =     $17
00DC 03                   =     $03    PBDD
00DD 17                   =     $17
00DE 02                   =     $02    PBD
00DF 17                   =     $17

00E0 35          STABLE   =     $35    SYM ENTRY POINT
00E1 80                   =     $80
00E2 7E                   =     $7E    IRQ INTERRUPT POINTER
00E3 A6                   =     $A6
00E4 02                   =     $02    PBDD
00E5 A0                   =     $A0
00E6 00                   =     $00    PBD
00E7 A0                   =     $A0
```

MEMORY PLUS Testing and Field Repair

Your MEMORY PLUS board has been burned in and tested before shipment. If, after following the steps outlined in the "Setting Up MEMORY PLUS" section, the board does not seem to work properly, or if it ever seems to stop functioning correctly, then the following steps should be taken.

1. Check that the board is receiving adequate power.

   Place the ground lead of a voltmeter or 'scope on any convenient ground on the board (the left lead of the large capacitor at the upper left hand corner of the board is handy) or on the connector (A-1, E-1, E-22, E-A, or E-Z).

   Measure the +5 volts at each of the four jumpers on the Header located near the voltage regulators. If you are providing unregulated +8 to +10 volts, then the top jumper should have this value. If you are using regulated +5 volts, then the top jumper should show +5V. The bottom three jumpers should show +5V in any case. If not, check your supply. If one of the three shows a voltage other than +5, it indicates a problem with the associated voltage regulator which might require replacement. The bottom jumper comes from Q6, the next jumper from Q5, and the next to top jumper from Q4. (See diagram on page 25).

   Measure the +25 volts at pin A-22 of the MEMORY PLUS application connector. If you are providing unregulated +27 to +30 volts, the output of the +25 volt regulator circuit should show about +24.7V. If you are providing regulated +25 volts at this pin, it will show the output of your power supply. If the value for the unregulated situation is not +24.7, then check your unregulated voltage at pin E-2 of the MEMORY PLUS expansion connector. It must be +27 to +30V.

2. Check that all IC chips are firmly in their sockets. It is possible for chips to come loose during handling and shipping. Push each chip firmly into its socket.

3. Check that the Header is in the proper position for the method of providing +5 volts. If you are providing +5 at pins E-21 and E-Y, then the Header should have its notched corner at pin 9 and the jumper wires should go from pins 2 - 15, 4 - 13, 6 - 11, and 8 - 9. If you are providing unregulated +8 to +10 volts at pins E-19 and E-20, then the Header should have its notched corner at pin 1 and the jumper wires should go from pins 1 - 16, 3 - 14, 5 - 12, and 7 - 10.

4. Check all of the connections between the MICRO, MEMORY PLUS, and the power supplies.

5. Follow the instructions in the "RAM Memory Test" section if the RAM Memory appears to be having problems.

6. Check the MICRO or try MEMORY PLUS with a different MICRO. For EPROM Programming it is absolutely essential that bits 0, 1, and 2 of the MICRO Port B are functioning properly (PB0, PB1, and PB2). A quick test of Port B may be made by putting FF in location PBDD and then trying to write 07 in location PBD. If this does not work, then you have a problem and should <u>not</u> attempt to program any EPROMs until you have the MICRO serviced.

Remember that you are exercising your MICRO in ways you may have never tried before. This will, in some cases, uncover faults that have existed undetected in a MICRO. For example, my own "reliable" Kim-1 which I had been using extensively for well over a year, turned out to have a defective Port B. Bits 0 and 1 which I had been using for cassette control worked fine, but bit 2 did not. I zapped a few EPROMs, not fatally thank goodness, before discovering this. Another KIM-1 I used had flakey memory in Page Zero such that the RAM Memory Test would not work. So, it really can happen.

7. Check all MEMORY PLUS switches and jumpers. In addition to the Header which was discussed in 1. and 3. above, there are two switches and a jumper to be concerned with:

   The RAM Address Select Switch (see page 8) must be set to "2K" for the Memory Test to work as documented. Actually, the memory test will work with any addresses, as long as the correct parameters are set in page zero location 0000 - start page number = first page to test and location 0001 - end page number = last page to test. The RAM switch must be selecting the bank of memory you are attempting to test, and it may not be selecting the same chunk of memory as the ROM select switch.

   The ROM Address Select Switch (see page 8) must not be set to the same starting address as the RAM switch. If the ROM switch is set to "EK", then there will be conflict with the MICRO Monitor interrupt vectors unless the jumper changes discussed on page 9 have been made, since the board comes with the jumper set so that interrupts will be decoded by the MICRO Monitor locations 1FFA through 1FFF. If you put ROM in E000 to FFFF, then this jumper must be changed. Otherwise any address in this range will be decoded twice: as E000 to FFFF <u>and</u> 0000 to 1FFF.

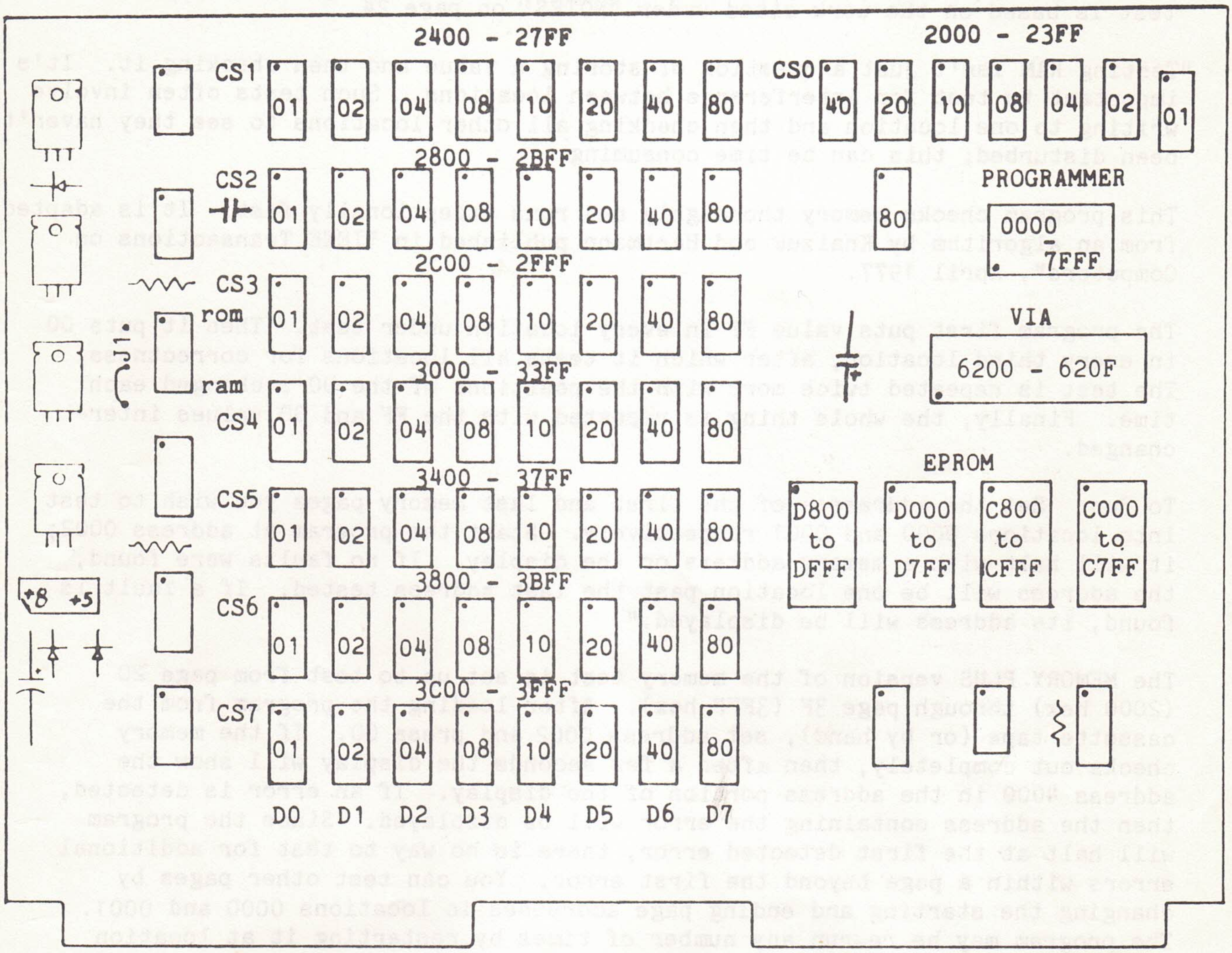
8. Check that all EPROMs are inserted in the proper direction. Pin 1 in the EPROM Programming Socket is in the upper left corner. Pin 1 in the EPROM normal sockets is in the upper right corner.

MEMORY PLUS was designed for easy field repair. It is, of course, hoped that no repair will ever be required on your unit. If some repair is required, then it is hoped that it can be done by the user or some local source. The unit should only have to be sent back for factory servicing in rare circumstances. This means that your MEMORY PLUS board should never be down very long.

WARNING:

Do <u>NOT</u> connect +5V Battery to E-2 or +27 Unreg. to E-3 if these lines are connected to your microcomputer via a cable of MOTHER board as these voltages could damage your computer. If these two voltages are to be used (for battery backup and EPROM programming) make sure they are isolated from the rest of your system.

Memory Organization with RAM selected at "2K" and ROM selected at "CK".



The dot in one corner of each IC chip and Header indicates the proper location of pin 1. The Header has two corners marked, one labelled +5 and one labelled +8. These indicate the proper orientation of the Header when the power supply is providing a regulated +5 volts or an unregulated +8 to +10 volts.

ROM and RAM show the location of the switches used to select the base address for the ROM and RAM memories.

J1 marks the location of the jumper which must be changed if ROM is placed to start at E000. The line shown is the etched jumper which causes interrupt addresses (FFFA to FFFF) to select the KIM-1 Monitor interrupt vectors (1FFA to 1FFF). This jumper must be removed and replaced by a jumper from the dot near the J to the dot near the 1 if interrupts are to be decoded by the high addresses.

RAM Memory Test

You should test the MEMORY PLUS RAM when you initially set up your system. You may also want to test it from time-to-time to make sure it is all still working properly. And, of course, you will want to test it whenever you have any reason to suspect that it may not be working right. The following memory test is based on the work cited under "NOTES" on page 24.

"Testing RAM isn't just a question of storing a value and then checking it. It's important to test for interference between locations. Such tests often involve writing to one location and then checking all other locations to see they haven't been disturbed; this can be time consuming.

This program checks memory thoroughly and runs exceptionally fast. It is adapted from an algorithm by Knaizuk and Hartmann published in "IEEE Transactions on Computers", April 1977.

The program first puts value FF in every location under test. Then it puts 00 in every third location, after which it tests all locations for correctness. The test is repeated twice more with the positions of the 00's changed each time. Finally, the whole thing is repeated with the FF and 00 values interchanged.

To Run: Set the addresses of the first and last memory pages you wish to test into locations 0000 and 0001 respectively. Start the program at address 0002; it will halt with a memory address on the display. If no faults were found, the address will be one location past the last address tested. If a fault is found, its address will be displayed."

The MEMORY PLUS version of the memory test is set up to test from page 20 (2000 hex) through page 3F (3FFF hex). After loading the program from the cassette tape (or by hand), set address 0002 and press GO. If the memory checks out completely, then after a few seconds the display will show the address 4000 in the address portion of the display. If an error is detected, then the address containing the error will be displayed. Since the program will halt at the first detected error, there is no way to test for additional errors within a page beyond the first error. You can test other pages by changing the starting and ending page addresses in locations 0000 and 0001. The program may be re-run any number of times by restarting it at location 0002.

Once a bad location has been detected, you can examine the location via the MICRO Monitor and perhaps determine the problem. For example, if the location has a data value of 7F, it would indicate that the most significant bit was not working. Refering to the Memory Organization drawing you could determine which 2102 chip was responsible for this bit. Since the RAM chips are all socketted, it is a simple matter to remove the suspect chip and replace it with another chip. Even if you do not have any spare 2102 chips handy, you can swap the suspect chip with another chip and see if the problem moves with the chip or stays in the same location. <u>IMPORTANT NOTE:</u> Turn the power off when removing any chips, otherwise you may destroy the memory chips. If the problem moves with the chip, then the solution is to get a replacement chip. If the problem does not move with the chip, then you must look elsewhere for the solution.

The next test would be to swap the 74LS367 chips and see if the problem shifted. Then the 74LS138 chips could be swapped. Finally you could replace the 74LS00, 74LS32, or 74LS04 chips. Note that the replacements do not have to be "LS" type. One of the above chip replacements should solve 99% of the problems which occur in the field.

```
                    MEMORY TEST  9 FEBRUARY 1979

                    MEMORY ORG   $0000

                    ACCESS  *    $8B86  SYM-1 ACCESS ENTRY
                    OUTBYT  *    $82FA  SYM-1 OUTPUT BYTE
                    SCANDS  *    $8906  SYM-1 SCAN DISPLAY

                    GOKIM   *    $1C4F  KIM-1 ENTRY POINT
                    LPOINT  *    $00FA  KIM DISPLAY POINTERS
                    HPOINT  *    $00FB

                    ASCOUT  *    $EF7B  AIM 65 OUTPUT ASCII

0000 20             BEGIN   =    $20    STARTING TEST PAGE
0001 3F             END     =    $3F    ENDING TEST PAGE

0002 A9 00          START   LDAIM $00    ZERO POINTERS
0004 A8                     TAY          FOR LOW ORDER ADDRESSES
0005 48                     PHA          SET ALL STATUS BITS TO ZERO
0006 28                     PLP
0007 85 D1                  STAZ  POINTL

0009 85 D3          BIGLP   STAZ  FLAG   = 00 FIRST PASS, = FF SECOND PASS
000B A2 02                  LDXIM $02
000D 86 D5                  STXZ  PASS   SET 3 TESTS EACH PASS

000F A5 00          NPASS   LDAZ  BEGIN  SET POINTER TO
0011 85 D2                  STAZ  POINTH START OF TEST AREA
0013 A6 01                  LDXZ  END
0015 A5 D3                  LDAZ  FLAG
0017 49 FF                  EORIM $FF    REVERSE FLAG
0019 85 D4                  STAZ  FLIP   = FF FIRST PASS, = 00 SECOND PASS

001B 91 D1          CLEAR   STAIY POINTL WRITE FLIP VALUE
001D C8                     INY          INTO ALL LOCATIONS
001E D0 FB                  BNE   CLEAR
0020 E6 D2                  INCZ  POINTH
0022 E4 D2                  CPXZ  POINTH
0024 B0 F5                  BCS   CLEAR

                  FLIP VALUE IN ALL LOCATIONS.  NOW CHANGE 1 IN 3

0026 A6 D5                  LDXZ  PASS
0028 A5 00                  LDAZ  BEGIN  SET POINTER
002A 85 D2                  STAZ  POINTH BACK TO START

002C A5 D3          FILL    LDAZ  FLAG   CHANGE VALUE
002E CA             TOP     DEX
002F 10 04                  BPL   SKIP   SKIP 2 OUT OF 3
0031 A2 02                  LDXIM $02    RESTORE 3 COUNTER
0033 91 D1                  STAIY POINTL CHANGE 1 OUT OF 3
0035 C8             SKIP    INY
0036 D0 F6                  BNE   TOP
0038 E6 D2                  INCZ  POINTH NEW PAGE
```

```
003A A5 01             LDAZ  END    HAVE WE PASSED
003C C5 D2             CMPZ  POINTH END OF TEST AREA?
003E B0 EC             BCS   FILL   NO. KEEP GOING

                MEMORY SET UP.  NOW TEST IT

0040 A5 00             LDAZ  BEGIN  SET POINTER
0042 85 D2             STAZ  POINTH BACK TO START
0044 A6 D5             LDXZ  PASS   SET UP 3 COUNTER

0046 A5 D4      POP    LDAZ  FLIP   TEST FOR FLIP VALUE
0048 CA                DEX          2 OUT OF 3 TIMES
0049 10 04             BPL   SLIP   OR
004B A2 02             LDXIM $02    1 OUT OF 3 TIMES
004D A5 D3             LDAZ  FLAG   TEST FOR FLAG VALUE

004F D1 D1      SLIP   CMPIY POINTL HER IS THE TEST
0051 D0 15             BNE   OUT    BRANCH IF FAILED
0053 C8                INY          BUMP POINTER
0054 D0 F0             BNE   POP    IF NOT DONE, KEEP BOING
0056 E6 D2             INCZ  POINTH
0058 A5 01             LDAZ  END    TEST END
005A C5 D2             CMPZ  POINTH
005C B0 E8             BCS   POP

                ABOVE TEST OKAY.  CHANGE AND REPEAT

005E C6 D5             DECZ  PASS   CHANGE 1 IN 3 POSITION
0060 10 AD             BPL   NPASS  AND DO NEXT PASS
0062 A5 D3             LDAZ  FLAG   INVERT FLAG
0064 49 FF             EORIM $FF    FOR PASS TWO
0066 30 A1             BMI   BIGLP  AND REPEAT BIG LOOP

0068 84 D1      OUT    STYZ  POINTL PUT LOW ORDER ADDRESS FOR DISPLAY
006A AD FD FF          LDA   $FFFD  TEST HIGH BYTE OF INTERRUPT VECTOR
006D C9 8B             CMPIM $8B    = SYM-1
006F F0 46             BEQ   SYM
0071 C9 E0             CMPIM $E0    = AIM 65
0073 F0 0B             BEQ   AIM

0075 A5 D1      KIM    LDAZ  POINTL MOVE POINTERS FOR KIM
0077 85 FA             STAZ  LPOINT
0079 A5 D2             LDAZ  POINTH
007B 85 FB             STAZ  HPOINT
007D 4C 4F 1C          JMP   GOKIM  RETURN TO KIM MONITOR

0080 A5 D2      AIM    LDAZ  POINTH MOVE DATA FOR AIM DISPLAY
0082 85 D6             STAZ  AHIGH
0084 A5 D1             LDAZ  POINTL
0086 85 D7             STAZ  ALOW
0088 A2 00             LDXIM $00    GET DATA AT ADDRESS
008A A1 D1             LDAIX POINTL
008C 85 D8             STAZ  ADATA
008E A2 13             LDXIM $13    START AT POSITION 19.

0090 8A         ALOOP  TXA          SAVE X VALUE
```

```
0091 48                    PHA           ON STACK
0092 A0 04                 LDYIM $04     SHIFT 4 POSITIONS PER CHARACTER
0094 A5 D8                 LDAZ  ADATA   GET DATA
0096 29 0F                 ANDIM $0F     MASK TO NIBBLE
0098 C9 0A                 CMPIM $0A     TEST DECIMAL
009A 30 03                 BMI   AOKAY   DECIMAL
009C 18                    CLC           A - F.  MUST CONVERT TO
009D 69 07                 ADCIM $07     ASCII
009F 18           AOKAY    CLC           FINISH CONVERSION
00A0 69 B0                 ADCIM $B0     ASCII + AIM FLAG
00A2 20 7B EF              JSR   ASCOUT  OUTPUT TO DISPLAY
00A5 46 D6        AMOVE    LSRZ  AHIGH   MOVE TO NEXT NIBBLE
00A7 66 D7                 RORZ  ALOW
00A9 66 D8                 RORZ  ADATA
00AB 88                    DEY
00AC D0 F7                 BNE   AMOVE

00AE 68                    PLA           RESTORE X
00AF AA                    TAX
00B0 CA                    DEX
00B1 E0 0E                 CPXIM $0E     DONE?
00B3 B0 DB                 BCS   ALOOP   NO
00B5 90 C9                 BCC   AIM     YES. REPEAT

00B7 20 86 8B     SYM      JSR   ACCESS ENABLE SYM MOEMORY
00BA A5 D2                 LDAZ  POINTH
00BC 20 FA 82              JSR   OUTBYT OUTPUT
00BF A5 D1                 LDAZ  POINTL
00C1 20 FA 82              JSR   OUTBYT
00C4 A0 00                 LDYIM $00
00C6 B1 D1                 LDAIY POINTL GET DATA
00C8 20 FA 82              JSR   OUTBYT

00CB 20 06 89     DISPLY   JSR   SCANDS SCAN DISPLAY
00CE 4C CB 00              JMP   DISPLY CONTINUE

00D1 00           POINTL   =     $00
00D2 00           POINTH   =     $00
00D3 00           FLAG     =     $00
00D4 00           FLIP     =     $00
00D5 00           PASS     =     $00
00D6 00           AHIGH    =     $00
00D7 00           ALOW     =     $00
00D8 00           ADATA    =     $00
```

MEMORY PLUS Parts List

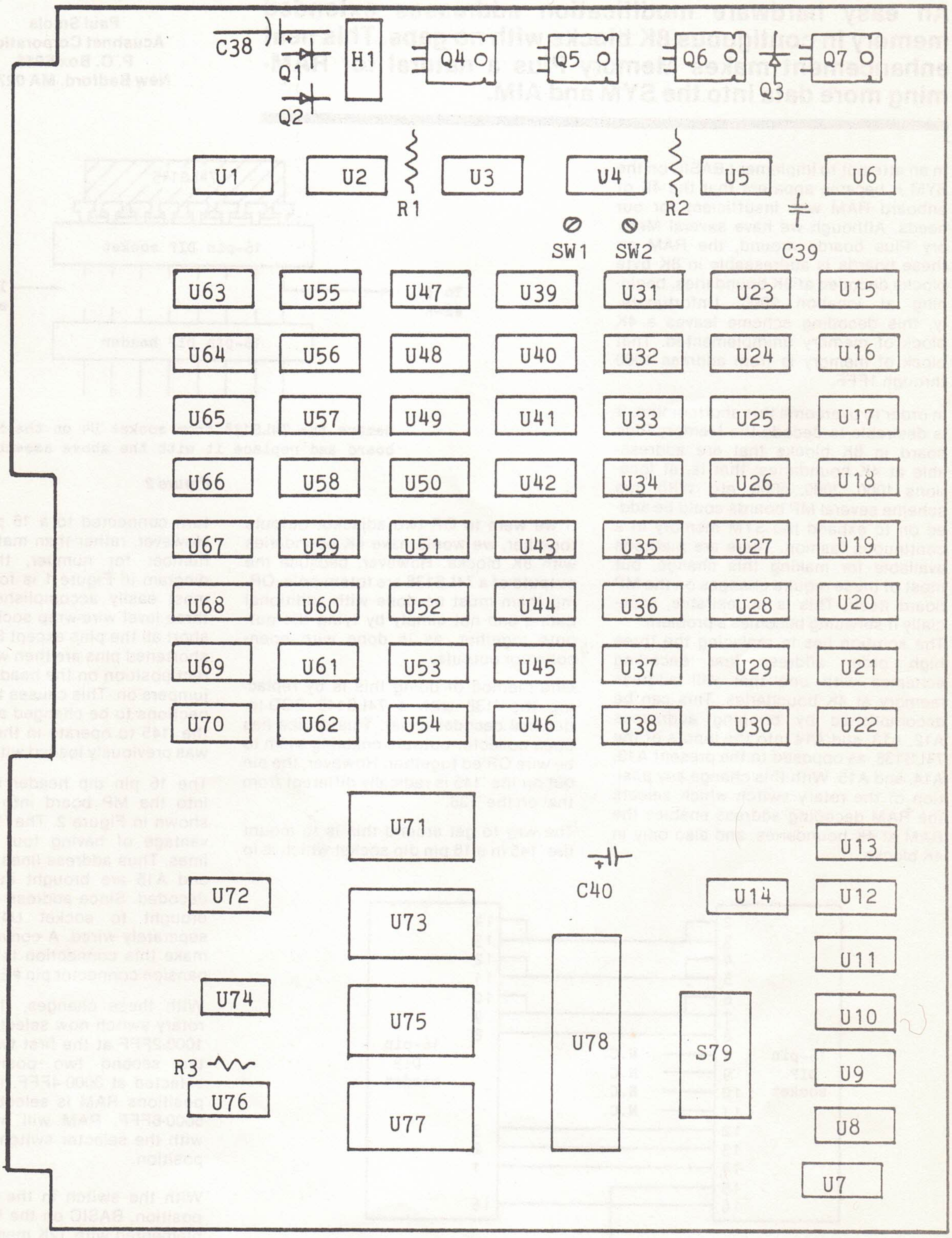
ITEM	PART	Qty.	DESCRIPTION
1.	U1, U2, U72	3	IC 74LS367 Hex Bus Driver with 3-state outputs
2.	U3, U4, U76	3	IC 74LS138 3-to-8 Line Decoder
3.	U5	1	IC 74LS00 Quad 2-Input Positive NAND Gates
4.	U6	1	IC 74LS32 Quad 2-Input Positive OR Gates
5.	U74	1	IC 74LS04 Hex Inverter
6.	U7 - U70	64	Memory Element 2102 450 nanosec, low power
7.	SW1, SW2	2	1-of-7 Rotary Switch
8.	R1 - R3	3	Resistor 3.3K, 1/4 watt
9.	C1 - C37	37	Capacitor .01 MFD, 50WV DC
10.	C38	1	Electrolytic Capacitor 22 - 25 MFD, 25V
11.	C39	1	Capacitor .001 MFD
12.	C40	1	Electrolytic Capacitor 3 - 5 MFD, 35V
13.	Q1, Q2, Q3	3	Diodes 1N4001 Rectifier 50V
14.	Q4, Q5, Q6	3	Voltage Regulator LM340T-5, +5V, 1.0A
15.	Q7	1	Voltage Regulator LM340T-24, +24V, 1.0A
16.	HS1 - HS3	3	T220 Heat Sink (Large)
17.	HS4	1	T220 Heat Sink (Small) (may be omitted)
18.	S1 - S4, S7 - S70, S72, S76, S80	71	IC Socket 16 pin
19.	S5, S6, S74	3	IC Socket 14 pin
20.	S71, S73, S75, S77, S79	5	IC Socket 24 pin
21.	S78	1	IC Socket 40 pin
22.	H1	1	IC Socket Header 16 pin
23.	U78	1	VIA 6522 Versatile Interface Adapter
	Accessories Package		
		3	Battery Clip 9V transistor battery type

NOTES:

1. The Memory Test is adapted from "Memory Test" by Jim Butterfield which appears on pages 122 and 123 of THE FIRST BOOK OF KIM, edited by Butterfield, Ockers and Rehnke, published by Hayden Book Company. The book sells for $9.00 and is a must for any 6502 user.

2. The program listings in this manual were produced by the Micro-ADE Assembler on a KIM-1 with a MEMORY PLUS board. The COMPUTERIST version of Micro-ADE includes a cassette tape with two versions of Micro-ADE. One has the program in 2000 to 2FFF and uses 3000 to 3FFF for the Source and Symbol working areas. The other has the program in C000 to CFFF and uses 2000 to 3FFF for the Source and Symbol working areas. This second version is ready to be placed into EPROM and left resident in your MEMORY PLUS board. Micro-ADE costs $25.00 for the Operators Manual and Cassette Tape. This Manual includes most of the Input/Output Source Listings so that the user can customize the package to his type of terminal. Complete Source Listings are available for an additional $25.00.

MEMORY PLUS Component Layout



SYM and AIM Memory Expansion

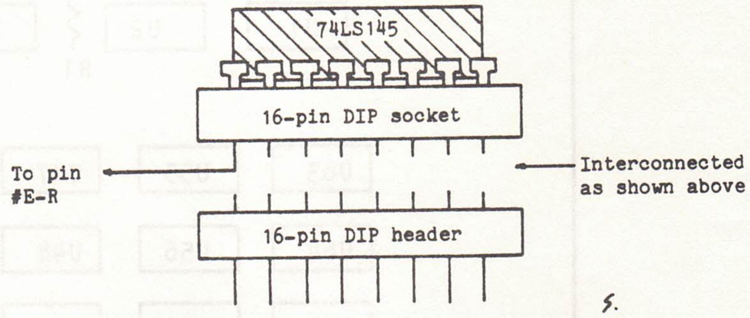
An easy hardware modification addresses extended memory in contiguous 8K blocks with no gaps. This neat enhancement makes Memory Plus a natural for RAMming more data into the SYM and AIM.

Paul Smola
Acushnet Corporation
P. O. Box E916
New Bedford, MA 02742

In an attempt to implement BASIC on the SYM it became apparent that the 4K of onboard RAM was insufficient for our needs. Although we have several Memory Plus boards around, the RAM on these boards is addressable in 8K byte blocks decoded at 8K boundaries, beginning at location 2000. Unfortunately, this decoding scheme leaves a 4K block of memory unimplemented. That block of memory is from address 1000 through 1FFF.

In order to overcome this shortcoming, it is desirable to decode the Memory Plus board in 8K blocks that are addressable at 4K boundaries; that is, at locations 1000, 3000, 5000, etc. With this scheme several MP boards could be added on to expand the SYM memory in a continuous fashion. There are methods available for making this change, but most of these require changes on the MP board itself. This is undesirable, especially if servicing becomes a problem.

The solution lies in replacing the three high order address line decoding schemes with one that will address memory at 4K boundaries. This can be accomplished by bringing addresses A12, A13, and A14 into the inputs of the 74LS138, as opposed to the present A13, A14, and A15. With this change any position of the rotary switch which selects the RAM decoding address enables the RAM at 4K boundaries, and also only in 4K blocks.



Remove the 74LS138 from socket U4 on the MP board and replace it with the above assembly

Figure 2

If we were to OR two adjacent outputs together, we would have 4K boundaries with 8K blocks. However, because the outputs of a 74LS138 are totem-pole, ORing them must be done with additional gating and not simply by tying the outputs together, as is done with open-collector outputs.

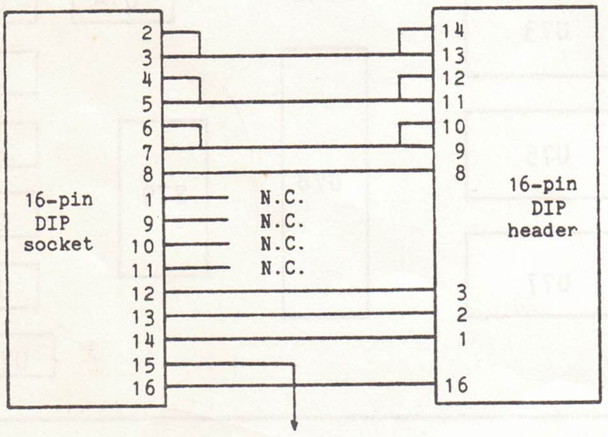
One method of doing this is by replacing the '138 with a 74LS145 BCD-to-decimal decoder driver. This device has open collector outputs enabling them to be wire OR'ed together. However, the pin out on the '145 is radically different from that on the '138.

The way to get around this is to mount the '145 in a 16 pin dip socket which is in turn connected to a 16 pin dip header. However, rather than matching the pins number for number, the connection diagram in Figure 1 is followed. This is most easily accomplished by using a three level wire-wrap socket and cutting short all the pins except 8 and 16. These shortened pins are then wired to the correct position on the header by soldering jumpers on. This causes the pin out connections to be changed and thus allows the '145 to operate in the socket which was previously loaded with the '138.

The 16 pin dip header is then loaded into the MP board into socket U4 as shown in Figure 2. The '145 has the advantage of having four address input lines. Thus address lines A12, A13, A14, and A15 are brought into it and fully decoded. Since address line A12 is not brought to socket U4, it must be separately wired. A convenient place to make this connection is on the MP expansion connector pin #E-R.

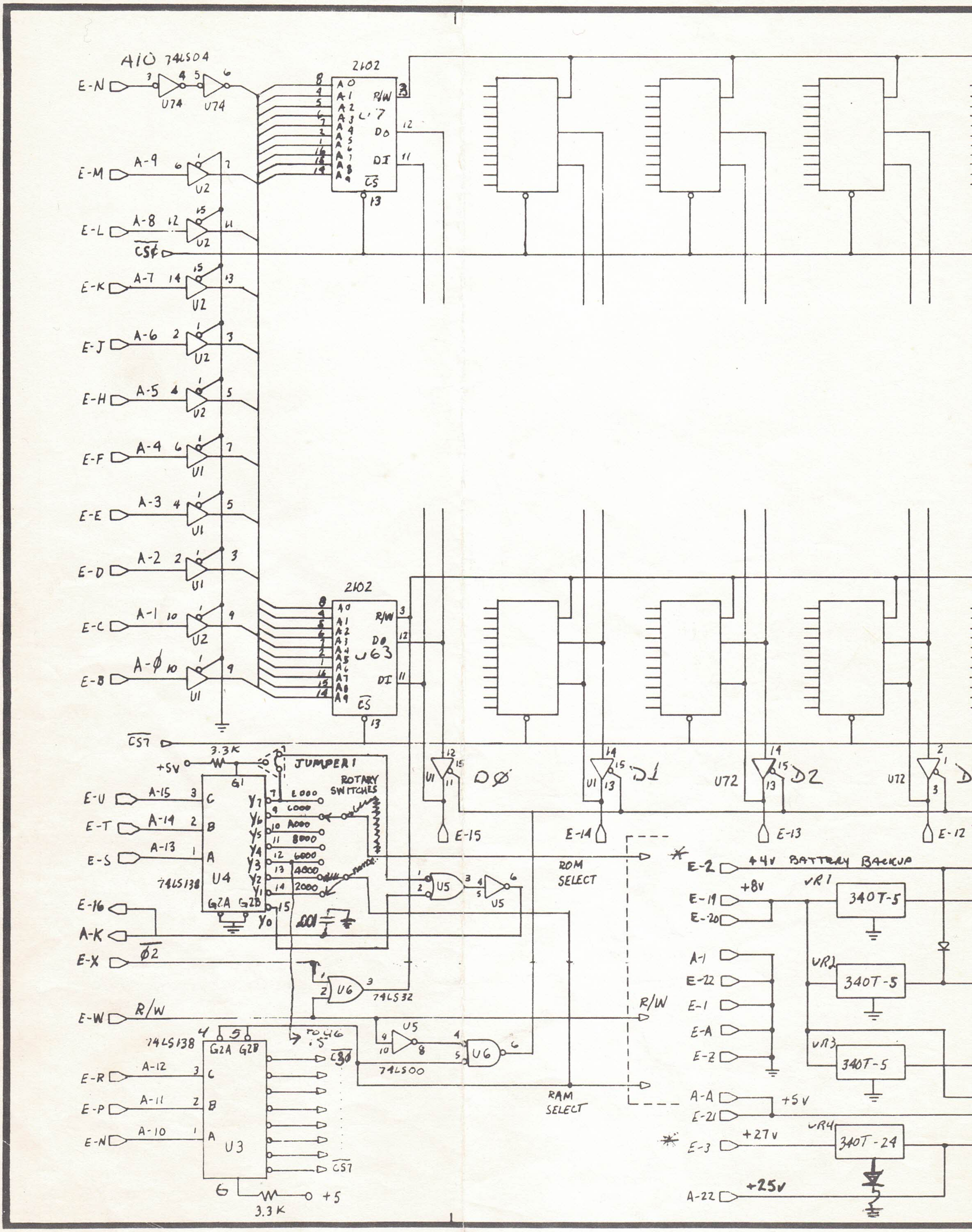
With these changes, the RAM select rotary switch now selects hex locations 1000-2FFF at the first two positions. At the second two positions RAM is selected at 3000-4FFF. In the third two positions RAM is selected at locations 5000-6FFF. RAM will not be selected with the selector switch in the seventh position.

With the switch in the first or second position, BASIC on the SYM can be implemented with 12K memory; the 4K onboard, plus the 8K from the MP. The addition of another MP board set up the same way with the RAM selection switch in either position 3 or 4 would yield a system with 20K of continuous memory.

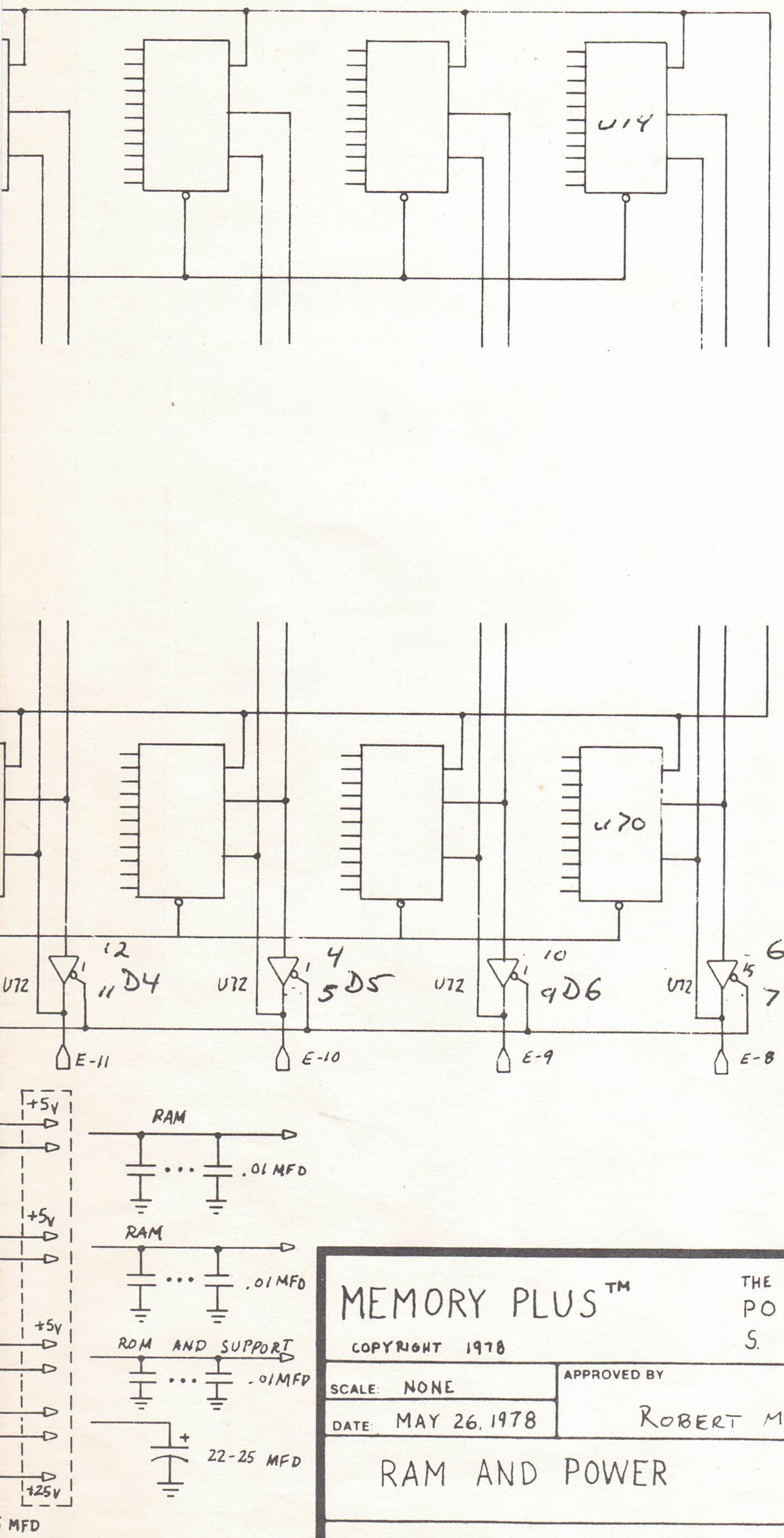


Solder to pin #E-R on the Memory Plus Expansion Connector

Figure 1



A10 74LS04
U74
E-N
E-M
A-9
E-L
A-8
CSφ
E-K
A-7
E-J
A-6
E-H
A-5
E-F
A-4
E-E
A-3
E-D
A-2
E-C
A-1
E-B
A-φ
U1
U2
2102
U7
2102
U63
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9
R/W
DO
DI
CS
CS7
+5V
3.3K
JUMPER 1
ROTARY SWITCHES
G1
Y7 Y6 Y5 Y4 Y3 Y2 Y1 Y0
E000
C000
A000
8000
6000
4000
2000
E-U
A-15
E-T
A-14
E-S
A-13
74LS138
U4
G2A G2B
E-16
A-K
E-X
φ2
.001
U5
U6
74LS32
74LS00
E-W
R/W
74LS138
G2A G2B
E-R
A-12
E-P
A-11
E-N
A-10
U3
CS7
+5
3.3K
TO U6 5
DØ
D1
D2
U72
E-15
E-14
E-13
E-12
ROM SELECT
RAM SELECT
R/W
E-2
+4V BATTERY BACKUP
+8V
E-19
E-20
VR1
340T-5
A-1
E-22
E-1
E-A
E-Z
VR2
340T-5
VR3
340T-5
A-A
E-21
+5V
E-3
+27V
VR4
340T-24
A-22
+25V



* See Warning Note on Page 18 before connecting power to E-2 (Battery Backup) or E-3 (Programming +27)

MEMORY PLUS™
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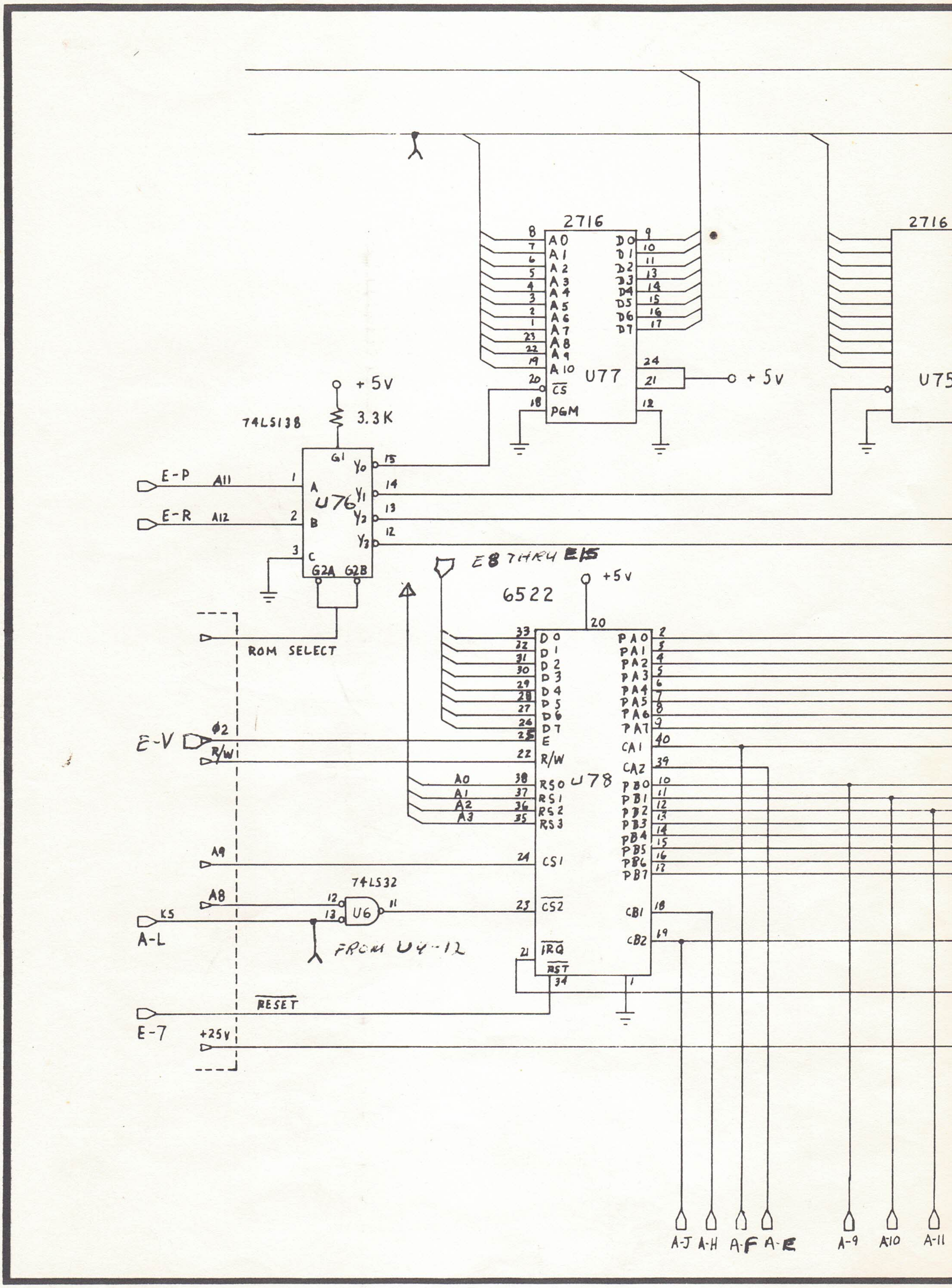
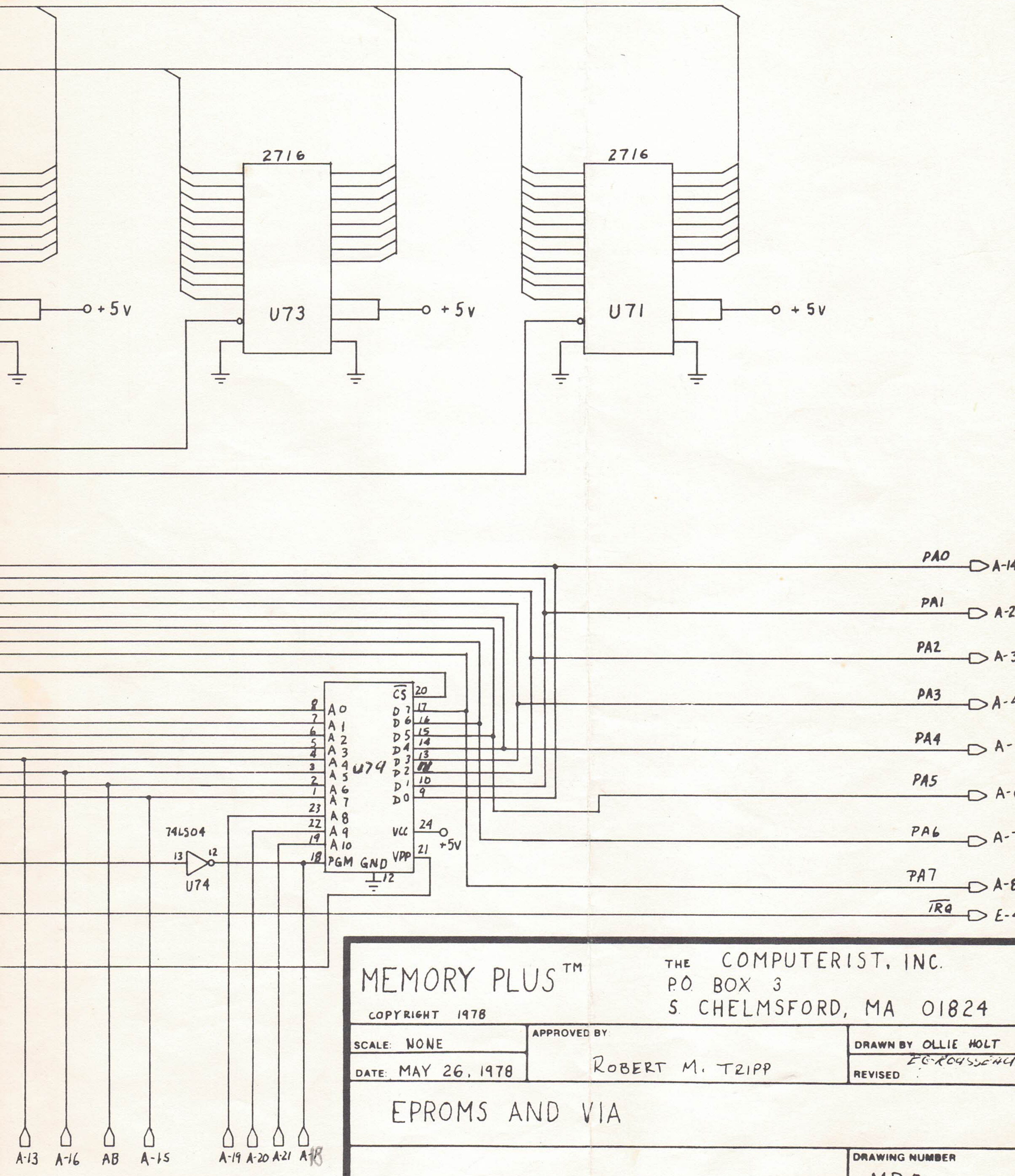
THE COMPUTERIST, INC.
PO BOX 3
S. CHELMSFORD MA 01824

SCALE: NONE	APPROVED BY	DRAWN BY OLLIE HOLT
DATE: MAY 26, 1978	ROBERT M. TRIPP	REVISED E G ROUSSEA

RAM AND POWER

DRAWING NUMBER
MP 1


2716
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10
D0 D1 D2 D3 D4 D5 D6 D7
U77
CS
PGM
+5V
74LS138
3.3K
G1
U76
Y0 Y1 Y2 Y3
A B C
G2A G2B
E-P A11
E-R A12
ROM SELECT
2716
U75
E8 THRU E15
6522
+5V
D0 D1 D2 D3 D4 D5 D6 D7
E
R/W
RS0 RS1 RS2 RS3
A0 A1 A2 A3
U78
PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7
CA1 CA2
PB0 PB1 PB2 PB3 PB4 PB5 PB6 PB7
CB1 CB2
CS1
CS2
IRQ
RST
E-V
φ2
R/W
A9
A8
74LS32
U6
KS
A-L
FROM U4-12
RESET
E-7
+25V
A-J A-H A-F A-E
A-9 A-10 A-11



MEMORY PLUS™

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THE COMPUTERIST, INC.
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SCALE: NONE

DATE: MAY 26, 1978

APPROVED BY: ROBERT M. TRIPP

DRAWN BY OLLIE HOLT

REVISED E.G. Rousseau

EPROMS AND VIA

DRAWING NUMBER MP 2

intel®

W

2716*

16K (2K × 8) UV ERASABLE PROM

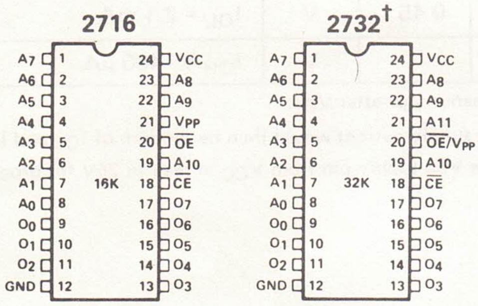
- **Fast Access Time**
  - **— 350 ns Max. 2716-1**
  - **— 390 ns Max. 2716-2**
  - **— 450 ns Max. 2716**
- **Single +5V Power Supply**
- **Low Power Dissipation**
  - **— 525 mW Max. Active Power**
  - **— 132 mW Max. Standby Power**
- **Pin Compatible to Intel® 5V ROMs (2316E, 2332, and 2364) and 2732 EPROM**
- **Simple Programming Requirements**
  - **Single Location Programming**
  - **Programs with One 50 ms Pulse**
- **Inputs and Outputs TTL Compatible during Read and Program**
- **Completely Static**

The Intel® 2716 is a 16,384-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2716 operates from a single 5-volt power supply, has a static standby mode, and features fast single address location programming. It makes designing with EPROMs faster, easier and more economical. For production quantities, the 2716 user can convert rapidly to Intel's pin-for-pin compatible 16K ROM (the 2316E) or the new 32K and 64K ROMs (the 2332 and 2364 respectively).

The 2716, with its single 5-volt supply and with an access time up to 350 ns, is ideal for use with the newer high performance +5V microprocessors such as Intel's 8085 and 8086. The 2716 is also the first EPROM with a static standby mode which reduces the power dissipation without increasing access time. The maximum active power dissipation is 525 mW while the maximum standby power dissipation is only 132 mW, a 75% savings.

The 2716 has the simplest and fastest method yet devised for programming EPROMs – single pulse TTL level programming. No need for high voltage pulsing because all programming controls are handled by TTL signals. Now, it is possible to program on-board, in the system, in the field. Program any location at any time – either individually, sequentially or at random, with the 2716's single address location programming. Total programming time for all 16,384 bits is only 100 seconds.

PIN CONFIGURATION*



†Refer to 2732 data sheet for specifications

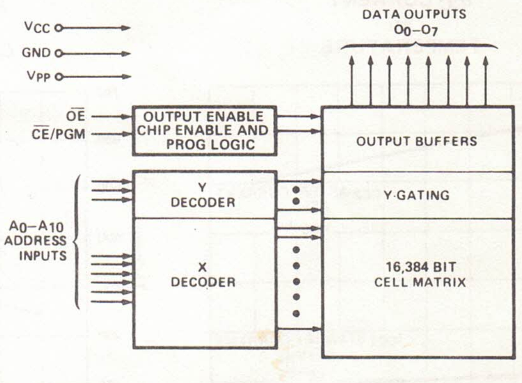
MODE SELECTION

MODE \ PINS	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

PIN NAMES

A_0–A_9	ADDRESSES
$\overline{CE}$/PGM	CHIP ENABLE/PROGRAM
$\overline{OE}$	OUTPUT ENABLE
O_0–O_7	OUTPUTS

BLOCK DIAGRAM



**Pin 18 and pin 20 have been renamed to conform with the entire family of 16K, 32K, and 64K EPROMs and ROMs. The die, fabrication process, and specifications remain the same and are totally uneffected by this change.*

FEBRUARY 1978

PROGRAMMING

The programming specifications are described in the Data Catalog PROM/ROM Programming Insutrctions on Page 4-83.

Absolute Maximum Ratings*

Temperature Under Bias . . . . –10°C to +80°C
Storage Temperature . . . . –65°C to +125°C
All Input or Output Voltages with
Respect to Ground . . . . +6V to –0.3V
V_{PP} Supply Voltage with Respect
to Ground During Program . . . . +26.5V to –0.3V

**COMMENT:* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Conditions During Read

	2716	2716-1	2716-2
Temperature Range	0°C – 70°C	0°C – 70°C	0°C – 70°C
V_{CC} Power Supply [1,2]	5V ± 5%	5V ± 10%	5V ± 5%
V_{PP} Power Supply [2]	$V_{CC} \pm 0.6V$ [3]	$V_{CC} \pm 0.6V$ [3]	$V_{CC} \pm 0.6V$ [3]

READ OPERATION

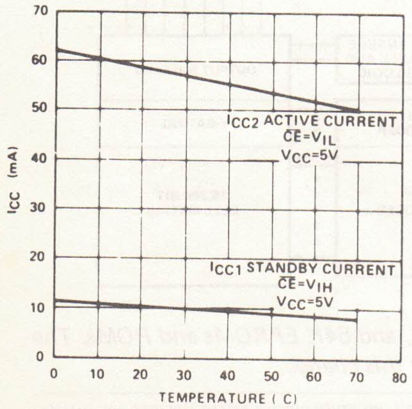
D.C. and Operating Characteristics

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[4]	Max.		
I_{LI}	Input Load Current			10	µA	$V_{IN} = 5.25V$
I_{LO}	Output Leakage Current			10	µA	$V_{OUT} = 5.25V$
I_{PP1} [2]	V_{PP} Current			5	mA	$V_{PP} = 5.85V$
I_{CC1} [2]	V_{CC} Current (Standby)		10	25	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$
I_{CC2} [2]	V_{CC} Current (Active)		57	100	mA	$\overline{OE} = \overline{CE} = V_{IL}$
V_{IL}	Input Low Voltage	-0.1		0.8	V	
V_{IH}	Input High Voltage	2.0		$V_{CC}+1$	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -400$ µA

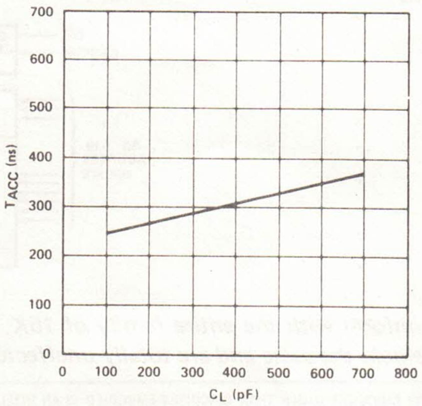
NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. The tolerance of 0.6V allows the use of a driver circuit for switching the V_{PP} supply pin from V_{CC} in read to 25V for programming.
4. Typical values are for T_A = 25°C and nominal supply voltages.
5. This parameter is only sampled and is not 100% tested.

Typical Characteristics

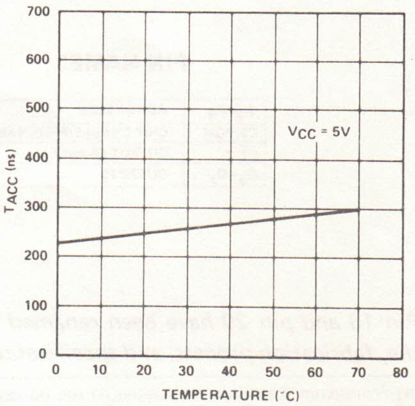
I_{CC} CURRENT vs. TEMPERATURE



ACCESS TIME vs. CAPACITANCE



ACCESS TIME vs. TEMPERATURE



A.C. Characteristics

Symbol	Parameter	2716 Limits			2716-1 Limits			2716-2 Limits			Unit	Test Conditions
		Min	Typ[4]	Max	Min	Typ[4]	Max	Min	Typ[4]	Max		
t_{ACC}	Address to Output Delay			450			350			390	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay			450			350			390	ns	$\overline{OE} = V_{IL}$
t_{OE}	Output Enable to Output Delay			120			120			120	ns	$\overline{CE} = V_{IL}$
t_{DF}	Output Enable High to Output Float	0		100	0		100	0		100	ns	$\overline{CE} = V_{IL}$
t_{OH}	Address to Output Hold	0			0			0			ns	$\overline{CE} = \overline{OE} = V_{IL}$

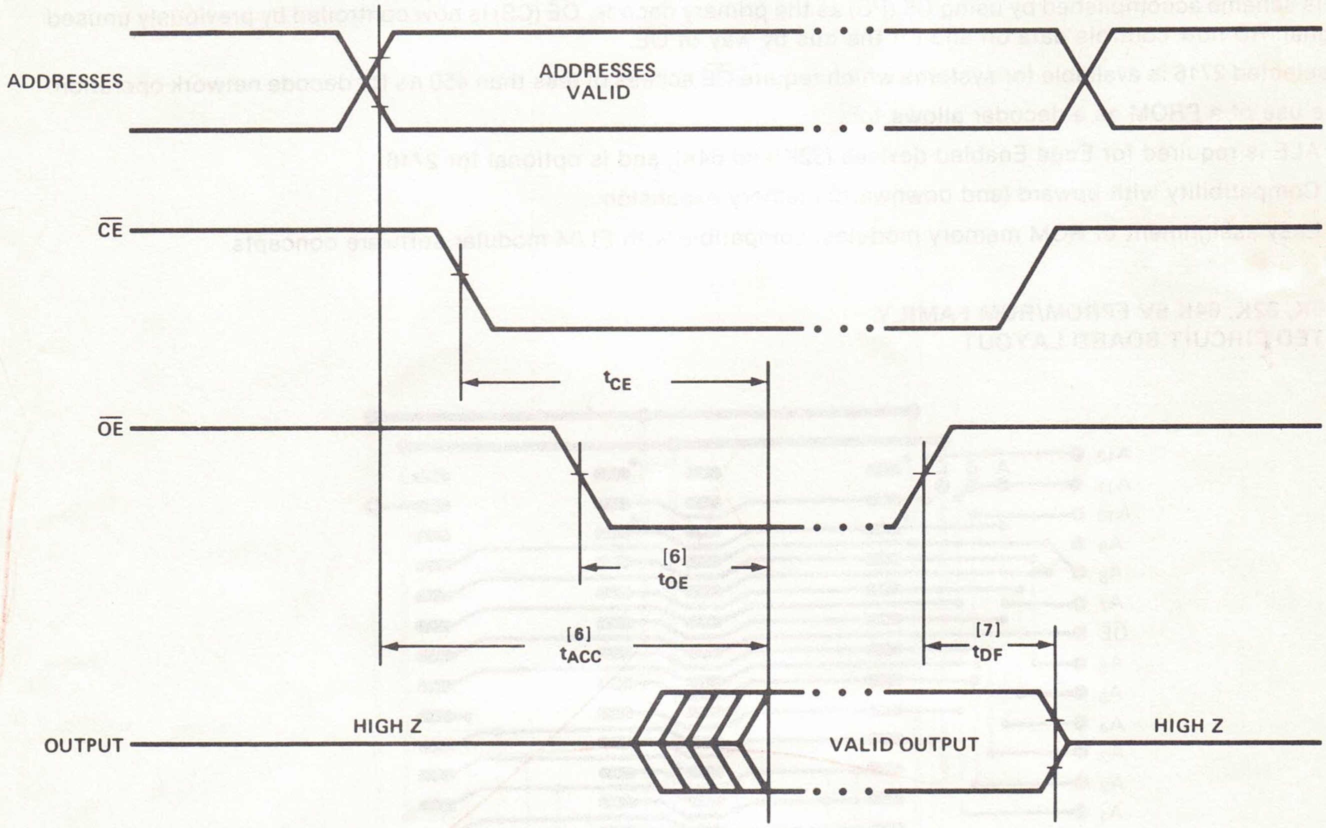
Capacitance[5] $T_A = 25°C$, f = 1 MHz

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

A.C. Test Conditions:

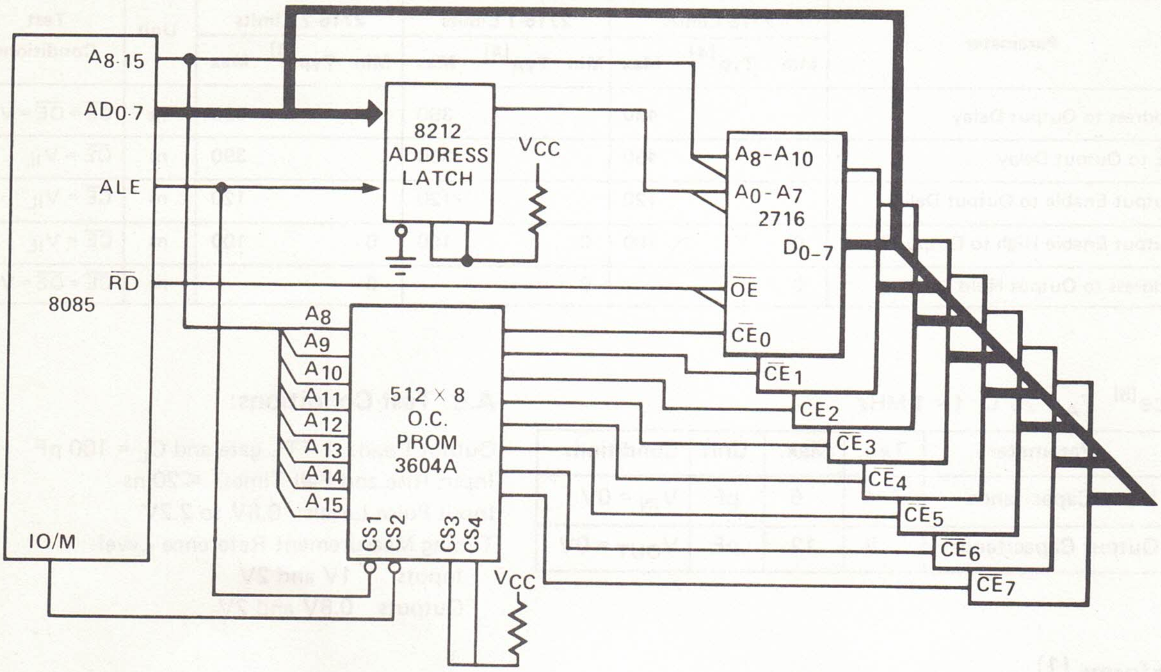
Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤20 ns
Input Pulse Levels: 0.8V to 2.2V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

A. C. Waveforms (1)



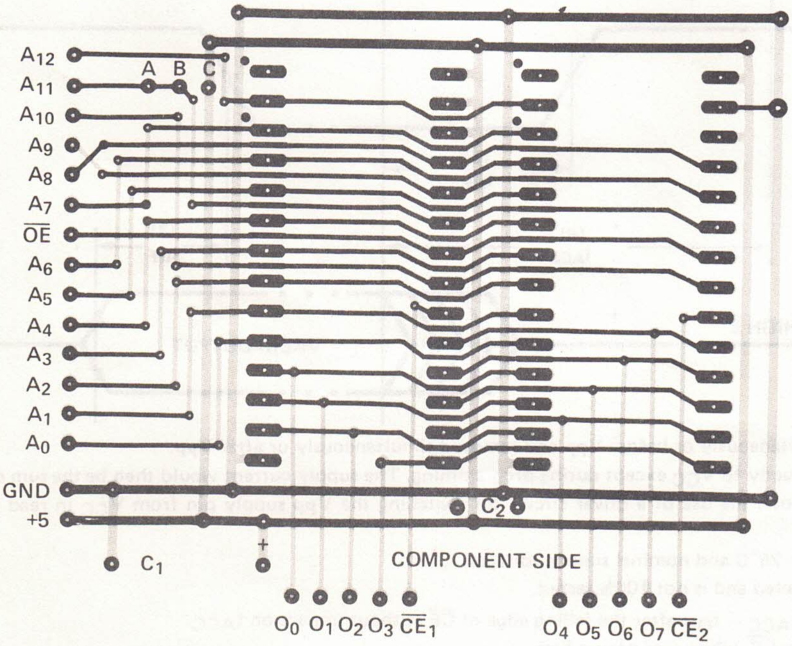
NOTE:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. The tolerance of 0.6V allows the use of a driver circuit for switching the V_{PP} supply pin from V_{CC} in read to 25V for programming.
4. Typical values are for T_A = 25°C and nominal supply voltages.
5. This parameter is only sampled and is not 100% tested.
6. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
7. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

TYPICAL 16K EPROM SYSTEM



- This scheme accomplished by using $\overline{\text{CE}}$ (PD) as the primary decode. $\overline{\text{OE}}$ (CS) is now controlled by previously unused signal. RD now controls data on and off the bus by way of $\overline{\text{OE}}$.
- A selected 2716 is available for systems which require $\overline{\text{CE}}$ access of less than 450 ns for decode network operation.
- The use of a PROM as a decoder allows for:
  - a) ALE is required for Edge Enabled devices (32K and 64K), and is optional for 2716.
  - b) Compatibility with upward (and downward) memory expansion.
  - c) Easy assignment of ROM memory modules, compatible with PL/M modular software concepts.

8K, 16K, 32K, 64K 5V EPROM/ROM FAMILY PRINTED CIRCUIT BOARD LAYOUT



ERASURE CHARACTERISTICS

The erasure characteristics of the 2716 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical 2716 in approximately 3 years, while it would take approximatley 1 week to cause erasure when exposed to direct sunlight. If the 2716 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 2716 window to prevent unintentional erasure.

The recommended erasure procedure (see Data Catalog page 4-83) for the 2716 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The 2716 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

DEVICE OPERATION

The five modes of operation of the 2716 are listed in Table I. It should be noted that all inputs for the five modes are at TTL levels. The power supplies required are a +5V V_{CC} and a V_{PP}. The V_{PP} power supply must be at 25V during the three programming modes, and must be at 5V in the other two modes.

TABLE I. MODE SELECTION

PINS / MODE	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

READ MODE

The 2716 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs 120 ns (t_{OE}) after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE

The 2716 has a standby mode which reduces the active power dissipation by 75%, from 525 mW to 132 mW. The 2716 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedence state, independent of the $\overline{OE}$ input.

OUTPUT DESELECTION

The outputs of two or more 2716s may be OR-tied together on the same data bus. Only one 2716 should have its output selected ($\overline{OE}$ low) to prevent data bus contention between 2716s in this configuration. The outputs of the other 2716s should be deselected by raising the $\overline{OE}$ input to a TTL high level.

PROGRAMMING

Initially, and after each erasure, all bits of the 2716 are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The 2716 is in the programming mode when the V_{PP} power supply is at 25V and $\overline{OE}$ is at V_{IH}. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 msec, active high, TTL program pulse is applied to the $\overline{CE}$/PGM input. A program pulse must be applied at each address location to be programmed. You can program any location at any time – either individually, sequentially, or at random. The program pulse has a maximum width of 55 msec. The 2716 must not be programmed with a DC signal applied to the $\overline{CE}$/PGM input.

Programming of multiple 2716s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled 2716s may be connected together when they are programmed with the same data. A high level TTL pulse applied to the $\overline{CE}$/PGM input programs the paralleled 2716s.

PROGRAM INHIBIT

Programming of multiple 2716s in parallel with different data is also easily accomplished. Except for $\overline{CE}$/PGM, all like inputs (including $\overline{OE}$) of the parallel 2716s may be common. A TTL level program pulse applied to a 2716's $\overline{CE}$/PGM input with V_{PP} at 25V will program that 2716. A low level $\overline{CE}$/PGM input inhibits the other 2716 from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify may be performed wth V_{PP} at 25V. Except during programming and program verify, V_{PP} must be at 5V.

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