Rockwell

R6500 MICROCOMPUTER SYSTEM PRODUCT DESCRIPTION

R6501Q ONE-CHIP MICROPROCESSOR

SECTION 1 INTRODUCTION

1.1 FEATURES OF THE R6501Q

- Enhanced 6502 CPU
  - —Four new bit manipulation instructions
    - Set Memory Bit (SMB)
    - Reset Memory Bit (RMB)
    - Branch on Bit Set (BBS)
    - Branch on Bit Reset (BBR)
  - —Decimal and binary arithmetic modes
  - —13 addressing modes
  - —True indexing
- 192-byte static RAM
- 32 bidirectional, TTL-compatible I/O lines (four ports)
- One 8-bit port may be tri-stated under software control
- One 8-bit port may have latched inputs under software control
- Two 16-bit programmable counter/timers, with latches
  - —Pulse width measurement
  - —Asymmetrical pulse generation
  - —Pulse generation
  - —Interval timer
  - —Event counter
  - —Retriggerable interval timer
- Serial port
  - —Full-duplex asynchronous operation mode
  - —Selectable 5- to 8-bit characters
  - —Wake-up feature
  - —Synchronous shift register mode
  - —Standard programmable bit rates programmable up to 62.5K bits/sec @ 1 MHz
- Ten interrupts
  - —Four edge-sensitive lines; two positive, two negative
  - —Reset
  - —Non-maskable
  - —Two counter underflows
  - —Serial data received
  - —Serial data transmitted
- Bus expandable to 64K bytes of external memory
- Flexible clock circuitry
  - —2-MHz or 1-MHz internal operation
  - —Internal clock with external XTAL at four times internal frequency
  - —External clock input divided by one or four
- 1 μs minimum instruction execution time at 2 MHz
- NMOS-3 silicon gate, depletion load technology
- Single +5V power supply
- 12 mW stand-by power for 32 bytes of the 192-byte RAM
- 64-pin QUIP

1.2 SUMMARY

The Rockwell R6501Q is a complete, high-performance 8-bit NMOS-3 microcomputer on a single chip and is compatible with all members of the R6500 family.

The R6501Q consists of an enhanced 6502 CPU, an internal clock oscillator, 192 bytes of Random Access Memory (RAM), and versatile interface circuitry. The interface circuitry includes two 16-bit programmable timer/counters, 32 bidirectional input/output lines (including four edge-sensitive lines and input latching on one 8-bit port), a full-duplex serial I/O channel, ten interrupts, and bus expandability.

The innovative architecture and the demonstrated high performance of the R6502 CPU, as well as instruction simplicity, results in system cost-effectiveness and a wide range of computational power. These features make the R6501Q a leading candidate for microcomputer applications.

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Rockwell supports development of the R6501Q with the System 65 Microcomputer Development System and the R6500/* Family of Personality Modules. Complete in-circuit emulation with the R6500/* Family of Personality Modules allows total system test and evaluation.

This product description assumes that the reader is familiar with the R6502 CPU hardware and programming capabilities. A detailed description of the R6502 CPU hardware is included in the R6500 Microcomputer System Hardware Manual (Document Number 29650N31). A description of the instruction capabilities of the R6502 CPU is contained in the R6500 Microcomputer System Programming Manual (Document Number 29650N30).

1.3 CUSTOMER OPTIONS

The R6501Q has no customer specified mask options. It has the following characteristics.

- Crystal Oscillator
- Clock Divide by 4
- Clock MASTER Mode
- Reset Vector at FFFC
- Internal pull-up resistors on Ports PA, PB, and PC

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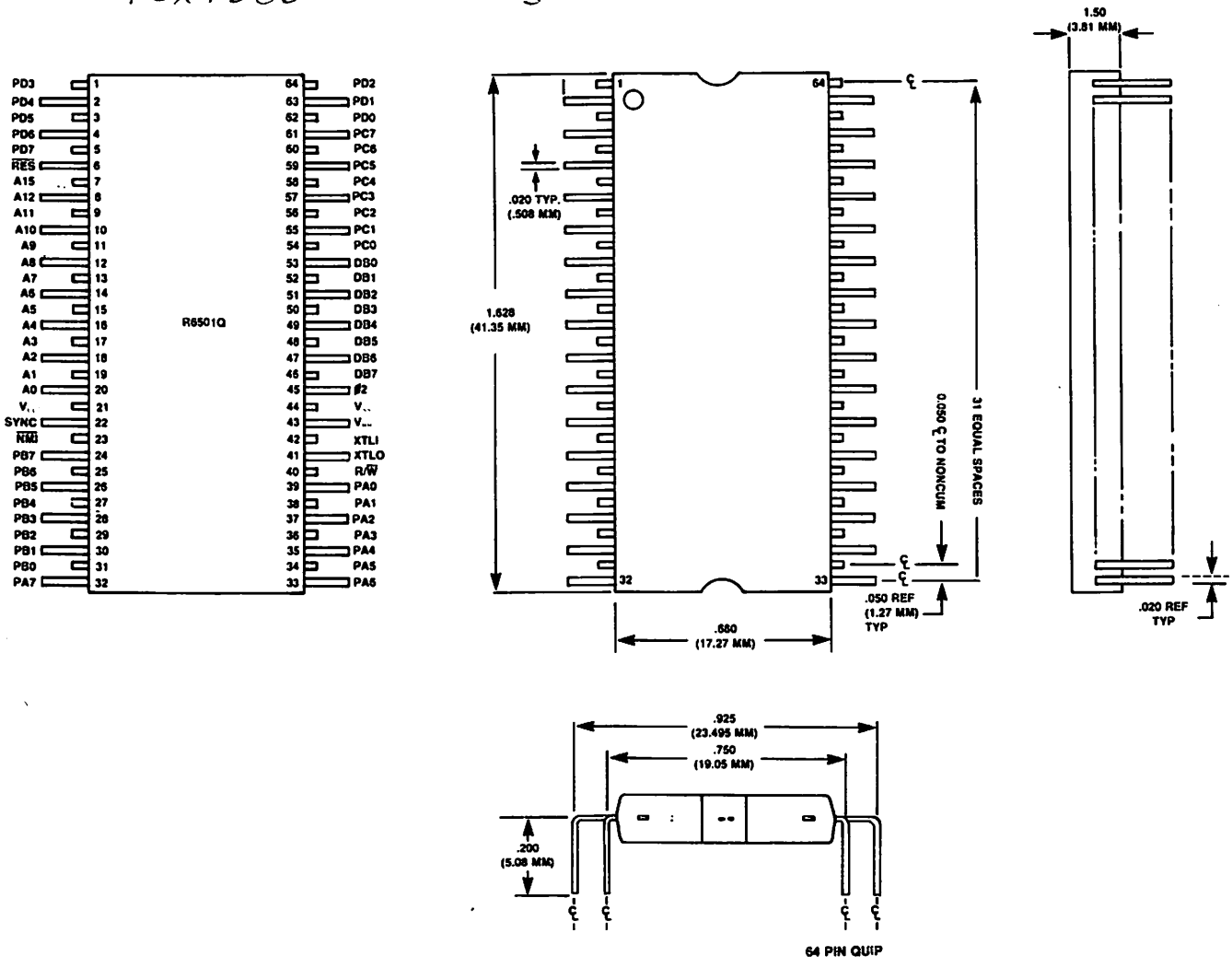


FIGURE 2-1. Mechanical Outline & Pin Out Configuration

SECTION 2
R6501Q INTERFACE REQUIREMENTS

This section describes the interface requirements for the R6501Q. Figure 2-1 and 2-2 show the Interface Diagram and the pin out configuration for both devices. Table 2-1 describes the function of each pin. Figure 3-1 has a detailed block diagram of the R6501Q ports which illustrates the internal function of the device.

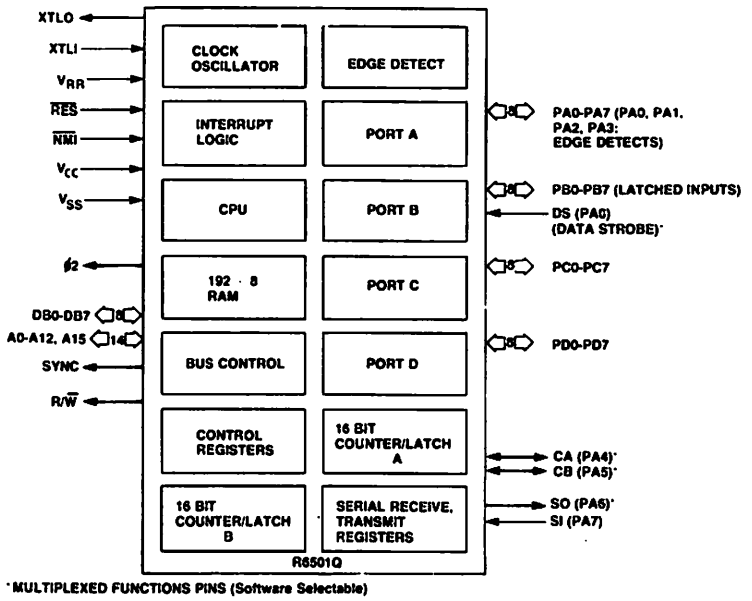


FIGURE 2-2. Interface Diagram

TABLE 2-1. R6501Q Pin Descriptions

SIGNAL NAME	PIN NO.	DESCRIPTION
V_{CC}	21	Main power supply +5V
V_{RR}	43	Separate power pin for RAM. In the event that V_{CC} power is off, this power retains RAM data.
V_{SS}	44	Signal and power ground (0V)
XTLI	42	Crystal or clock input for internal clock oscillator. Allows input of X1 clock signal if XTLO is connected to V_{SS} or of X4 clock if XTLO is floated.
XTLO	41	Crystal output from internal clock oscillator.
$\overline{RES}$	6	The Reset input is used to initialize the device. This signal must not transition from low to high for at least eight cycles after V_{CC} reaches operating range and the internal oscillator has stabilized.
$\phi 2$	45	Clock signal output at internal frequency.
$\overline{NMI}$	23	A negative going edge on the Non-Maskable Interrupt signal requests that a non-maskable interrupt be generated with the CPU.
PA0-PA7 PB0-PB7 PC0-PC7 PD0-PD7	39-32 31-24 54-61 62-64, 1-5	Four 8-bit ports used for either input/output. Each line of Ports A, B and C consists of an active transistor to V_{SS} and a passive pull-up to V_{CC}. Port D functions as either an 8-bit input or 8-bit output port. It has active pull-up and pull-down transistors.
A0-A12, A15	20-7	Fourteen address lines used to address a complete 65K external address space. Note: A13 & A14 are sourced through PC6 & PC7 when in the Full Address Mode.
DB0-DB7	53-46	Eight bidirectional data bus lines used to transmit data to and from external memory.
SYNC	22	SYNC is a positive going signal for the full clock cycle whenever the CPU is performing an OP CODE fetch.
R/$\overline{W}$	40	Controls the direction of data transfer between the CPU and the external 65K address space. The signal is high when reading and low when writing.

SECTION 3
SYSTEM ARCHITECTURE

This section provides a functional description of the R6501Q. Functionally the R6501Q consists of a CPU, RAM, four 8-bit parallel I/O ports, a serial I/O port, dual counter/latch circuits, a mode control register, and an interrupt flag/enable dual register circuit. A block diagram of the system is shown in Figure 3-1.

> **NOTE**
>
> Throughout this document, unless specified otherwise, all memory or register address locations are specified in hexadecimal notation.

3.1 CPU LOGIC

The R6501Q internal CPU is a standard 6502 configuration with an 8-bit Accumulator register, two 8-bit Index Registers (X and Y); an 8-bit Stack Pointer register, an ALU, a 16-bit Program Counter, and standard instruction register/decode and internal timing control logic.

3.1.1 Accumulator

The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of the two data words used in these operations.

3.1.2 Index Registers

There are two 8-bit index registers, X and Y. Each index register can be used as a base to modify the address data program counter and thus obtain a new address—the sum of the program counter contents and the index register contents.

When executing an instruction which specifies indirect addressing, the CPU fetches the op code and the address and modifies the address from memory by adding the index register to it prior to loading or storing the value of memory.

Indexing greatly simplifies many types of programs, especially those using data tables.

3.1.3 Stack Pointer

The Stack Pointer is an 8-bit register. It is automatically incremented and decremented under control of the microprocessor to perform stack manipulation in response to either user instructions, an internal $\overline{IRQ}$ interrupt, or the external interrupt line $\overline{NMI}$. The Stack Pointer must be initialized by the user program.

The stack allows simple implementation of multiple level interrupts, subroutine nesting and simplification of many types of data manipulation. The JSR, BRK, RTI and RTS instructions use the stack and Stack Pointer.

The stack can be envisioned as a deck of cards which may be accessed only from the top. The address of a memory location is stored (or "pushed") onto the stack. Each time data are to be pushed onto the stack, the Stack Pointer is placed on the Address Bus, data are written into the memory location addressed by the Stack Pointer, and the Stack Pointer is decremented by 1. Each time data are read (or "pulled") from the stack, the Stack Pointer is incremented by 1. The Stack Pointer is then placed on the Address Bus and data are read from the memory location addressed by the Pointer.

The stack is located on zero page, i.e., memory locations 00FF-0040. After reset, which leaves the Stack Pointer indeterminate, normal usage calls for its initialization at 00FF.

3.1.4 Arithmetic And Logic Unit (ALU)

All arithmetic and logic operations take place in the ALU, including incrementing and decrementing internal registers (except the Program Counter). The ALU cannot store data for more than one cycle. If data are placed on the inputs to the ALU at the beginning of a cycle, the result is always gated into one of the storage registers or to external memory during the next cycle.

Each bit of the ALU has two inputs. These inputs can be tied to various internal buses or to a logic zero; the ALU then generates the function (AND, OR, SUM, and so on) using the data on the two inputs.

3.1.5 Program Counter

The 16-bit Program Counter provides the addresses that are used to step the processor through sequential instructions in a program. Each time the processor fetches an instruction from program memory, the lower (least significant) byte of the Program Counter (PCL) is placed on the low-order bits of the Address Bus and the higher (most significant) byte of the Program Counter (PCH) is placed on the high-order 8 bits of the Address Bus. The Counter is incremented each time an instruction or data is fetched from program memory.

3.1.6 Instruction Register and Instruction Decode

Instructions are fetched from ROM or RAM and gated onto the Internal Data Bus. These instructions are latched into the Instruction Register, then decoded along with timing and interrupt signals to generate control signals for the various registers.

3.1.7 Timing Control

The Timing Control Logic keeps track of the specific instruction cycle being executed. This logic is set to T0 each time an instruction fetch is executed and is advanced at the beginning of each Phase One clock pulse for as many cycles as are required to complete the instruction. Each data transfer which takes place between the registers is caused by decoding the contents of both the instruction register and timing control unit.

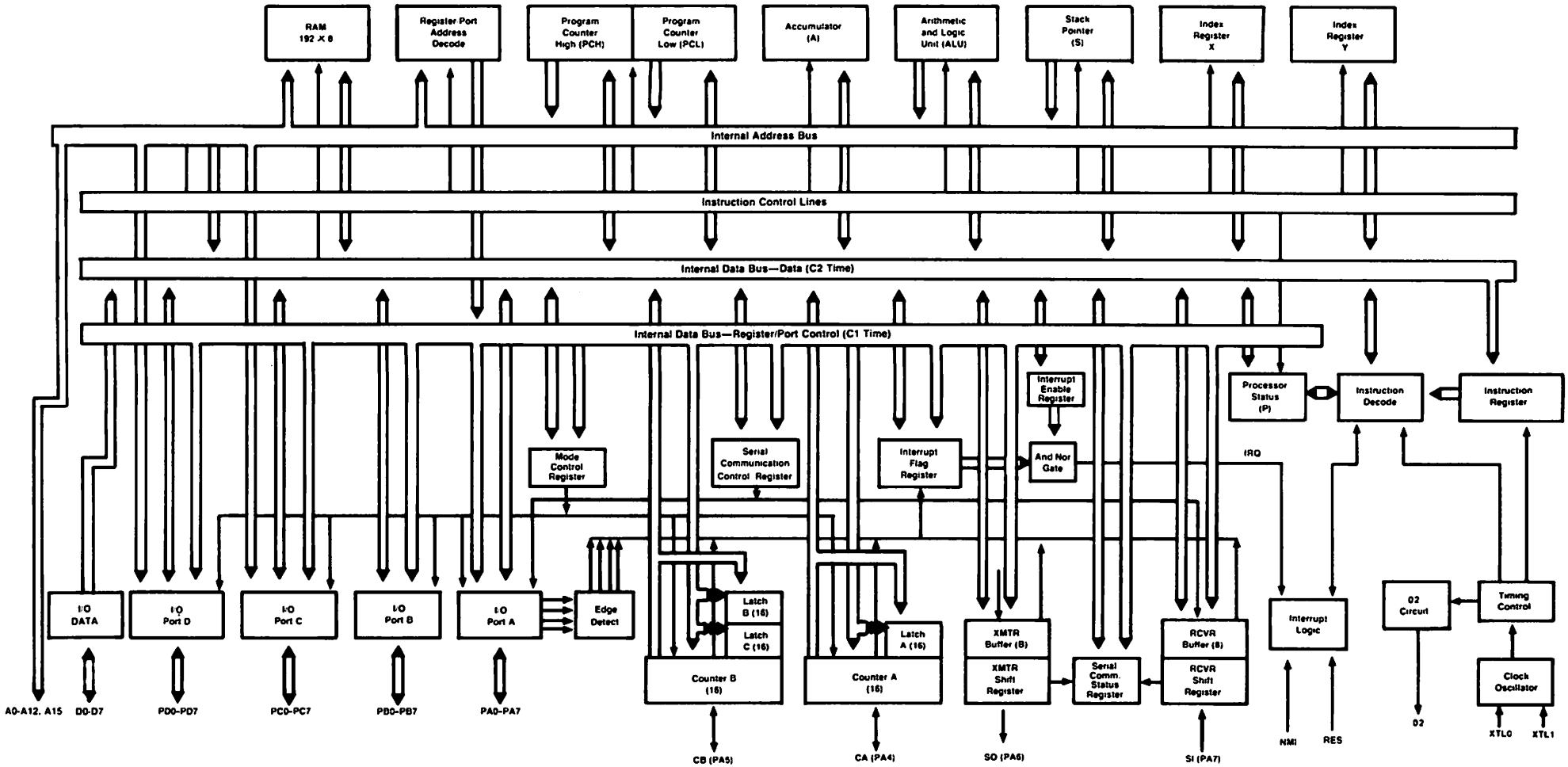


FIGURE 3-1. Detailed Block Diagram

3.1.8 Interrupt Logic

Interrupt logic controls the sequencing of three interrupts; $\overline{RES}$, $\overline{NMI}$ and $\overline{IRQ}$. $\overline{IRQ}$ is generated by any one of eight conditions: 2 Counter Overflows, 2 Positive Edge Detects, 2 Negative Edge Detects, and 2 Serial Port Conditions.

3.2 NEW INSTRUCTIONS

In addition to the standard R6502 instruction set, four new bit manipulation instructions have been added to the R6501Q. The added instructions and their format are explained in the following paragraphs. Refer to Appendix A for the Op Code mnemonic addressing matrix for these added instructions. The four added instructions do not impact the CPU processor status register.

3.2.1 Set Memory Bit (SMB m, Addr.)

This instruction sets to "1" one of the 8-bit data field specified by the zero page address (memory or I/O port). The first byte of the instruction specifies the SMB operation and one of eight bits to be set. The second byte of the instruction designates address (0-255) of the byte to be operated upon.

3.2.2 Reset Memory Bit (RMB m, Addr.)

This instruction is the same operation and format as SMB instruction except a reset to "0" of the bit results.

3.2.3 Branch On Bit Set Relative (BBS m, Addr, DEST)

This instruction tests one of eight bits designated by a 3-bit immediate field within the first byte of the instruction. The second byte is used to designate the address of the byte to be tested within the zero page address range (memory or I/O ports). The third byte of the instruction is used to specify the 8-bit relative address to which the instruction branches if the bit tested is a "1". If the bit tested is not set, the next sequential instruction is executed.

3.2.4 Branch On Bit Reset Relative (BBR m, Addr, DEST)

This instruction is the same operation and format as the BBS instruction except that a branch takes place if the bit tested is a "0".

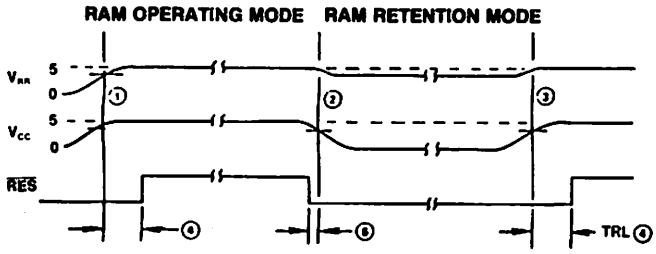
3.3 READ-ONLY-MEMORY (ROM)

The R6501Q has no ROM and its Reset vector is at FFFC.

3.4 RANDOM ACCESS MEMORY (RAM)

The RAM consists of 192 bytes of read/write memory with an assigned page zero address of 0040 through 00FF. The R6501Q provides a separate power pin (V_{RR}) which may be used for standby power for 32 bytes located at 0040-005F. In the event of the loss of V_{CC} power, the lowest 32 bytes of RAM data will be retained if standby power is supplied to the V_{RR} pin. If the RAM data retention is not required then V_{RR} must be connected to V_{CC}. During operation V_{RR} must be at the V_{CC} level.

For the RAM to retain data upon loss of V_{CC}, V_{RR} must be supplied within operating range and $\overline{RES}$ must be driven low at least eight Ø2 clock pulses before V_{CC} falls out of operating range. $\overline{RES}$ must then be held low while V_{CC} is out of operating range and until at least eight Ø2 clock cycles after V_{CC} is again within operating range and the internal Ø2 oscillator is stabilized. V_{RR} must remain within V_{CC} operating range during normal operation. When V_{CC} is out of operating range, V_{RR} must remain within the V_{RR} retention range in order to retain data. Figure 3.2 shows typical waveforms.



1 INITIAL APPLICATION OF V_{CC} AND V_{RR}.
2 LOSS OF V_{CC}, RAM ON STANDBY POWER.
3 REAPPLICATION OF V_{CC}.
4 >8 Ø2 CLOCK PULSES AFTER OSCILLATOR STABILIZATION.
5 >8 Ø2 CLOCK PULSES.

FIGURE 3-2. Data Retention Timing

3.5 CLOCK OSCILLATOR

The R6501Q has been configured for a crystal oscillator, a divide by 4 countdown network, and for Master Mode Operation.

A reference frequency can be generated with the on-chip oscillator using either an external crystal or an external oscillator. The oscillator reference frequency passes through an internal countdown network (divide by 4) to obtain the internal operating frequency (see Figures 3-3a and 3-3b). The external crystal generated reference frequency is a preferred method since the resistor method can have tolerances approaching 50%.

Internal timing can also be controlled by driving the XTLI pin with an external frequency source. Figure 3-3c shows typical connections. If XTLO is left floating, the external source is divided by the internal countdown network. However, if XTLO is tied to V_{SS}, the internal countdown network is bypassed causing the chip to operate at the frequency of the external source.

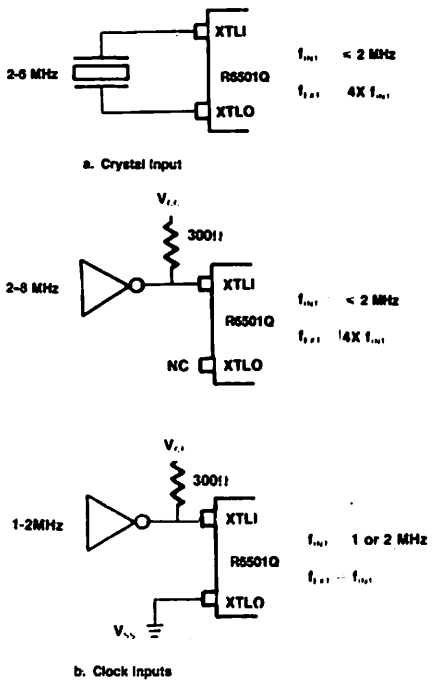


FIGURE 3-3. Clock Oscillator Input Options

3.6 MODE CONTROL REGISTER (MCR)

The Mode Control Register contains control bits for the multifunction I/O ports and mode select bits for Counter A and Counter B. Its setting, along with the setting of the Serial Communications Control Register (SCCR), determines the basic configuration of the R6501Q in any application. Initializing this register is one of the first actions of any software program. The Mode Control Register bit assignment is shown in Figure 3-5.

3.7 INTERRUPT FLAG REGISTER (IFR) AND INTERRUPT ENABLE REGISTER (IER)

An $\overline{IRQ}$ interrupt request can be initiated by any or all of eight possible sources. These sources are all capable of being enabled or disabled by the use of the appropriate interrupt enabled bits in the Interrupt Enable Register (IER). Multiple simultaneous interrupts cause the $\overline{IRQ}$ interrupt request to remain active until all interrupting conditions have been serviced and cleared.

The Interrupt Flag Register contains the information that indicates which I/O or counter needs attention. The contents of the Interrupt Flag Register may be examined at any time by reading at address: 0011. Edge detect IFR bits may be cleared by executing a RMB instruction at address location 0010. The RMB X, (0010) instruction reads FF, modifies bit X to a "0", and writes the modified value at address location 0011. In this way IFR bits set to a "1" after the read cycle of a Read-Modify-Write instruction (such as RMB) are protected from being cleared. A logic "1" is ignored when writing to edge detect IFR bits.

Each IFR bit has a corresponding bit in the Interrupt Enable Register which can be set to a "1" by writing a "1" in the respective bit position at location 0012. Individual IER bits may be cleared by writing a "0" in the respective bit position, or by $\overline{RES}$. If set to a "1", an IRQ will be generated when the corresponding IFR bit becomes true. The Interrupt Flag Register and Interrupt Enable Register bit assignments are shown in Figure 3-6 and the functions of each bit are explained in Table 3-1.

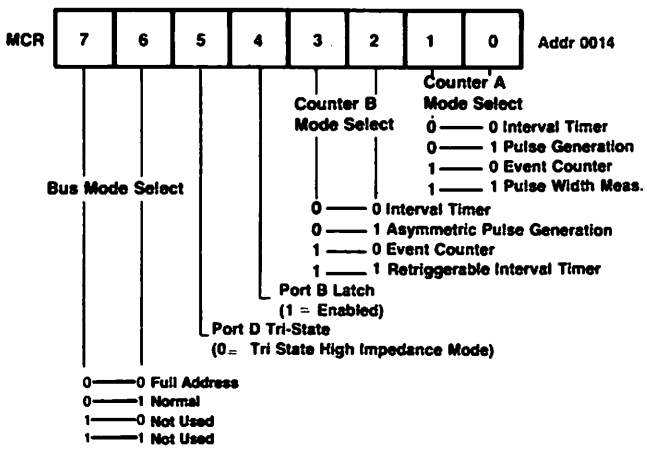


FIGURE 3-5. Mode Control Register

The use of Counter A Mode Select is shown in Section 6.1.

The use of Counter B Mode Select is shown in Section 6.2.

The use of Port B Latch Enable is shown in Section 4.4.

The use of Port D in Tri-State Enable is shown in Section 4.6.

The use of Bus Mode Select is shown in Section 4.5 and 4.6.

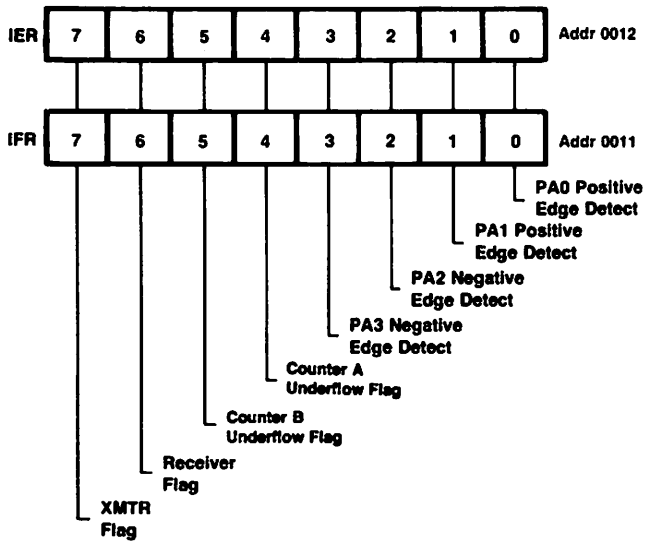


FIGURE 3-6. Interrupt Enable and Flag Registers

3.8 PROCESSOR STATUS REGISTER

The 8-bit Processor Status Register, shown in Figure 3-7, contains seven status flags. Some of these flags are controlled by the user program; others may be controlled both by the user's program and the CPU. The R6500 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags. Each of the eight processor status flags is described in the following sections.

3.8.1 Carry Bit (C)

The Carry Bit (C) can be considered as the ninth bit of an arithmetic operation. It is set to logic 1 if a carry from the eighth bit has occurred or cleared to logic 0 if no carry occurred as the result of arithmetic operations.

The Carry Bit may be set or cleared under program control by use of the Set Carry (SEC) or Clear Carry (CLC) instruction, respectively. Other operations which affect the Carry Bit are ADC, ASL, CMP, CPX, CPY, LSR, PLP, ROL, ROR, RTI, and SBC.

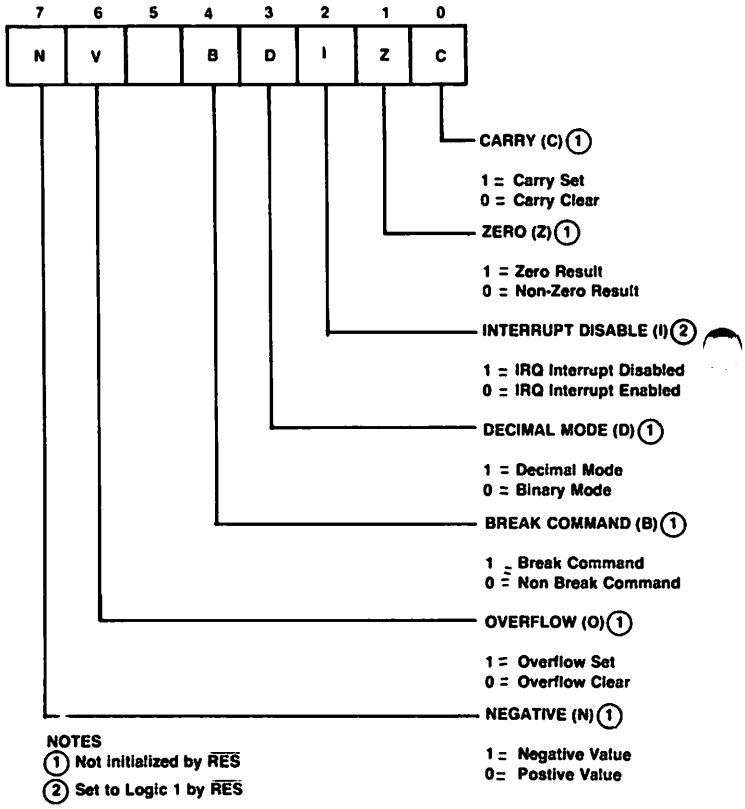


FIGURE 3-7. Processor Status Register

TABLE 3-1. Interrupt Flag Register Bit Codes

BIT CODE	FUNCTION
IFR 0:	PA0 Positive Edge Detect Flag—Set to a "1" when a positive going edge is detected on PA0. Cleared by RMB O (0010) instruction or by $\overline{RES}$.
IFR 1:	PA1 Positive Edge Detect Flag—Set to a 1 when a positive going edge is detected on PA1. Cleared by RMB 1 (0010) instruction or by $\overline{RES}$.
IFR 2:	PA2 Negative Edge Detect Flag—Set to a 1 when a negative going edge is detected on PA2. Cleared by RMB 2 (0010) instruction or by $\overline{RES}$.
IFR 3:	PA3 Negative Edge Detect Flag—Set to 1 when a negative going edge is detected on PA3. Cleared by RMB 3 (0010) instruction or by $\overline{RES}$.
IFR 4:	Counter A Underflow Flag—Set to a 1 when Counter A underflow occurs. Cleared by reading the Lower Counter A at location 0018, by writing to address location 001A, or by $\overline{RES}$.
IFR 5:	Counter B Underflow Flag—Set to a 1 when Counter B underflow occurs. Cleared by reading the Lower Counter B at location 001C, by writing to address location 001E, or by $\overline{RES}$.
IFR 6:	Receiver Interrupt Flag—Set to a 1 when any of the Serial Communication Status Register bits 0 through 3 is set to a 1. Cleared when the Receiver Status bits (SCSR 0-3) are cleared or by $\overline{RES}$.
IFR 7:	Transmitter Interrupt Flag—Set to a 1 when SCSR 6 is set to a 1 while SCSR 5 is a 0 or SCSR 7 is set to a 1. Cleared when the Transmitter Status bits (SCSR 6 & 7) are cleared or by $\overline{RES}$.

3.8.2 Zero Bit (Z)

The Zero Bit (Z) is set to logic 1 by the CPU during any data movement or calculation which sets all 8 bits of the result to zero. This bit is cleared to logic 0 when the resultant 8 bits of a data movement or calculation operation are not all zero. The R6500 instruction set contains no instruction to specifically set or clear the Zero Bit. The Zero Bit is, however, affected by the following instructions; ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TXA, TSX, and TYA.

3.8.3 Interrupt Disable Bit (I)

The Interrupt Disable Bit (I) is used to control the servicing of an interrupt request ($\overline{IRQ}$). If the I Bit is reset to logic 0, the $\overline{IRQ}$ signal will be serviced. If the bit is set to logic 1, the $\overline{IRQ}$ signal will be ignored. The CPU will set the Interrupt sable Bit to logic 1 if a RESET ($\overline{RES}$), $\overline{IRQ}$, or Non-Maskable Interrupt ($\overline{NMI}$) signal is detected.

The I bit is cleared by the Clear Interrupt Mask Instruction (CLI) and is set by the Set Interrupt Mask Instruction (SEI). This bit is set by the BRK Instruction. The Return from Interrupt (RTI) and Pull Processor Status (PLP) instructions will also affect the I bit.

3.8.4 Decimal Mode Bit (D)

The Decimal Mode Bit (D) is used to control the arithmetic mode of the CPU. When this bit is set to logic 1, the adder operates as a decimal adder. When this bit is cleared to logic 0, the adder operates as a straight binary adder. The adder mode is controlled only by the programmer. The Set Decimal Mode (SED) instruction will set the D bit; the Clear Decimal Mode (CLD) instruction clears it. The PLP and RTI instructions also affect the Decimal Mode Bit.

CAUTION

The Decimal Mode Bit will either set or clear in an unpredictable manner upon power application. This bit must be initialized to the desired state by the user program or erroneous results may occur.

3.8.5 Break Bit (B)

The Break Bit (B) is used to determine the condition which caused the $\overline{IRQ}$ service routine to be entered. If the $\overline{IRQ}$ service routine was entered because the CPU executed a BRK command, the Break Bit will be set to logic 1. If the $\overline{IRQ}$ routine was entered as the result of an $\overline{IRQ}$ signal being generated, the B bit will be cleared to logic 0. There are no instructions which can set or clear this bit.

3.8.6 Overflow Bit (V)

The Overflow Bit (V) is used to indicate that the result of a signed, binary addition, or subtraction, operation is a value that cannot be contained in seven bits ($-128 \leq n \leq 127$). This indicator only has meaning when signed arithmetic (sign and seven magnitude bits) is performed. When the ADC or SBC instruction is performed, the Overflow Bit is set to logic 1 if the polarity of the sign bit (bit 7) is changed because the result exceeds $+127$ or -128; otherwise the bit is cleared to logic 0. The V bit may also be cleared by the programmer using a Clear Overflow (CLV) instruction.

The Overflow Bit may also be used with the BIT instruction. The BIT instruction—which may be used to sample interface devices—allows the overflow flag to reflect the condition of bit 6 in the sampled field. During a BIT instruction the Overflow Bit is set equal to the content of the bit 6 on the data tested with BIT instruction. When used in this mode, the overflow has nothing to do with signed arithmetic, but is just another sense bit for the microprocessor. Instructions affecting the V flag are ADC, BIT, CLV, PLP, RTI and SBC.

3.8.7 Negative Bit (N)

The Negative Bit (N) is used to indicate that the sign bit (bit 7) in the resulting value of a data movement or data arithmetic operation is set to logic 1. If the sign bit is set to logic 1, the resulting value of the data movement or arithmetic operation is negative; if the sign bit is cleared, the result of the data movement or arithmetic operation is positive. There are no instructions that set or clear the Negative Bit since the Negative Bit represents only the status of a result. The instructions that effect the state of the Negative Bit are: ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TSX, TXA, and TYA.

SECTION 4
PARALLEL INPUT/OUTPUT PORTS & BUS MODES

The devices have 32 I/O lines grouped into four 8-bit ports (PA, PB, PC, and PD). Ports A through C may be used either for input or output individually or in groups of any combination. Port D may be used as all inputs or all outputs.

Multifunction I/O's such as Port A and Port C are protected from normal port I/O instructions when they are programmed to perform a multiplexed function.

Internal pull-up resistors (FET's with an impedance range of $3K \leq R_L \leq 12K$ ohm) are provided on all port pins except Port D.

The direction of the 32 I/O lines are controlled by four 8-bit port registers located in page zero. This arrangement provides quick programming access using simple two-byte zero page address instructions. There are no direction registers associated with the I/O ports, thus simplifying I/O handling. The I/O addresses are shown in Table 4-1. Appendix E.4 shows the I/O Port Timing.

TABLE 4-1. I/O Port Addresses

PORT	ADDRESS
A	0000
B	0001
C	0002
D	0003

4.1 INPUTS

Inputs for Ports A, B, and C are enabled by loading logic 1 into all I/O port register bit positions that are to correspond to I/O input lines. A low (<0.8V) input signal will cause a logic 0 to be read when a read instruction is issued to the port register. A high (>2.0V) input will cause a logic 1 to be read. An $\overline{RES}$ signal forces all I/O port registers to logic 1 thus initially treating all I/O lines as inputs.

Port D may only be all inputs or all outputs. All inputs is selected by setting bit 5 of the Mode Control Register (MCR5) to a "0".

The status of the input lines can be interrogated at any time by reading the I/O port addresses. Note that this will return the actual status of the input lines, not the data written into the I/O port registers.

Read/Modify/Write instructions can be used to modify the operation of PA, PB, PC, & PD. During the Read cycle of a Read/Modify/Write instruction the Port I/O register is read. For all other read instructions the port input lines are read. Read/Modify/Write instructions are: ASL, DEC, INC, LSR, RMB, ROL, ROR, and SMB.

4.2 OUTPUTS

Outputs for Ports A thru D are controlled by writing the desired I/O line output states into the corresponding I/O port register bit positions. A logic 1 will force a high (>2.4V) output while a logic 0 will force a low (<0.4V) output.

Port D all outputs is selected by setting MCR5 to a "1".

4.3 Port A (PA)

Port A can be programmed via the Mode Control Register (MCR) and the Serial Communications Control Register (SCCR) as a standard parallel 8-bit, bit independent, I/O port or as serial channel I/O lines, counter I/O lines, or an input data strobe for the Port B input latch option. Table 4-2 tabulates the control and usage of Port A.

In addition to their normal I/O functions, PA0 and PA1 can detect positive going edges and PA2 and PA3 can detect negative going edges. A proper transition on these pins will set a corresponding status bit in the IFR and generate an interrupt request if the respective Interrupt Enable Bit is set. The maximum rate at which an edge can be detected is one-half the $\phi 2$ clock rate. Edge detection timing is shown in Appendix E.3.

TABLE 4-2. Port A Control & Usage

PA0 (2) PIN 39	PA0 I/O		PORT B LATCH MODE	
	MCR4 = 0		MCR4 = 1	
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE
	PA0	I/O	PORT B LATCH STROBE	INPUT (1)

PA1 (2) PIN 38 PA2 (3) PIN 37 PA3 (3) PIN 36	PA1-PA3 I/O	
	SIGNAL	
	NAME	TYPE
	PA1 PA2 PA3	I/O I/O I/O

PA4 PIN 35	PA4 I/O		COUNTER A I/O			
	MCR0 = 0 MCR1 = 0 SCCR7 = 0 RCVR S/R MODE = 0 (4) (5)		MCR0 = 1 MCR1 = 0 SCCR7 = 0 RCVR S/R MODE = 0 (4)		SCCR7 = 0 SCCR6 = 0 MCR1 = 1	
	SIGNAL		SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE	NAME	TYPE
	PA4	I/O	CNTA	OUTPUT	CNTA	INPUT (1)
	SERIAL I/O SHIFT REGISTER CLOCK					
	SCCR7 = 1 SCCR5 = 1		RCVR S/R MODE = 1 (4)			
	SIGNAL		SIGNAL			
	NAME	TYPE	NAME	TYPE		
	XMTR CLOCK	OUTPUT	RCVR CLOCK	INPUT (1)		

PA5 PIN 34	PA5 I/O		COUNTER B I/O			
	MCR3 = 0 MCR2 = 0		MCR3 = 0 MCR2 = 1		MCR3 = 1 MCR2 = X	
	SIGNAL		SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE	NAME	TYPE
	PA5	I/O	CNTB	OUTPUT	CNTB	INPUT (1)

PA6 PIN 33	PA6 I/O		SERIAL I/O XMTR OUTPUT	
	SCCR7 = 0		SCCR7 = 1	
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE
	PA6	I/O	XMTR	OUTPUT

PA7 PIN 32	PA7 I/O		SERIAL I/O RCVR INPUT	
	SCCR6 = 0		SCCR6 = 1	
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE
	PA7	I/O	RCVR	INPUT (1)

(5) Under the following conditions PA4 will function as an Input Only pin:

A. Serial I/O XMTR off, RCVR in Asynchronous Mode, and MCR1 = 1.

B. Serial I/O XMTR on and neither XMTR nor RCVR operating in the Synchronous S/R Mode.

(1) HARDWARE BUFFER FLOAT
(2) POSITIVE EDGE DETECT
(3) NEGATIVE EDGE DETECT
(4) RCVR S/R MODE = 1 WHEN SCCR6 · $\overline{\text{SCCR5}}$ · SCCR4 = 1

4.4 PORT B (PB)

Port B can be programmed as an 8-bit, bit-independent I/O port. It has a latched input capability which may be enabled or disabled via the Mode Control Register (MCR). Table 4-3 tabulates the control and usage of Port B. An Input Data Strobe signal must be provided thru PA0 when Port B is programmed to be used with latched input option. Input data latch timing for Port B is shown in Appendix E.3.

TABLE 4-3. Port B Control & Usage

		I/O MODE		LATCH MODE	
		MCR4 = 0		MCR4 = 1 (2)	
PIN #	PIN NAME	SIGNAL		SIGNAL	
		NAME	TYPE (1)	NAME	TYPE
31	PB0	PB0	I/O	PB0	INPUT
30	PB1	PB1	I/O	PB1	INPUT
29	PB2	PB2	I/O	PB2	INPUT
28	PB3	PB3	I/O	PB3	INPUT
27	PB4	PB4	I/O	PB4	INPUT
26	PB5	PB5	I/O	PB5	INPUT
25	PB6	PB6	I/O	PB6	INPUT
24	PB7	PB7	I/O	PB7	INPUT

(1) RESISTIVE PULL-UP, ACTIVE BUFFER PULL DOWN
(2) INPUT DATA IS STORED IN PORT B LATCH BY PA0 PULSE

4.5 PORT C (PC)

Port C can be programmed as an I/O port, or as part of the full address bus. When operating in the Full Address Mode PC6 and PC7 serve as A13 and A14 with PC0-PC5 operating as normal I/O pins.

4.6 PORT D (PD)

Port D can be programmed as an I/O Port. Mode selection for Port D is made by the Mode Control Register (MCR). The Port D output drivers can be selected as tri-state drivers by setting bit 5 of the MCR to 1 (one). Table 4-5 shows the necessary settings for the MCR to achieve the various modes for Port D.

4.7 BUS MODES

In the Full Address Mode, the separate address and data bus are used in conjunction with PC6 and PC7, which automatically provide A13 and A14. The remaining ports perform the normal I/O function.

In the I/O Bus Mode all ports serve as I/O. The address and data bus are still functional but without A13 and A14. Since the internal RAM and registers are in the OOXX location, A15 can be used for chip select and A0-A12 used for selecting 8K of external memory.

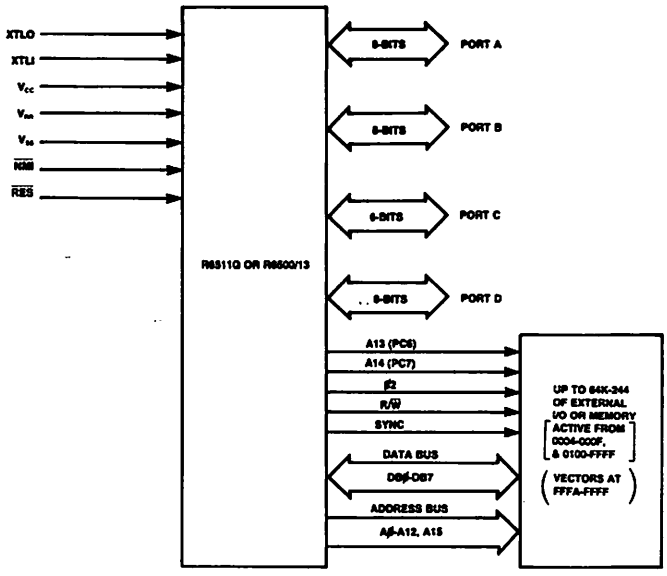


FIGURE 4-1a. Full Address Mode

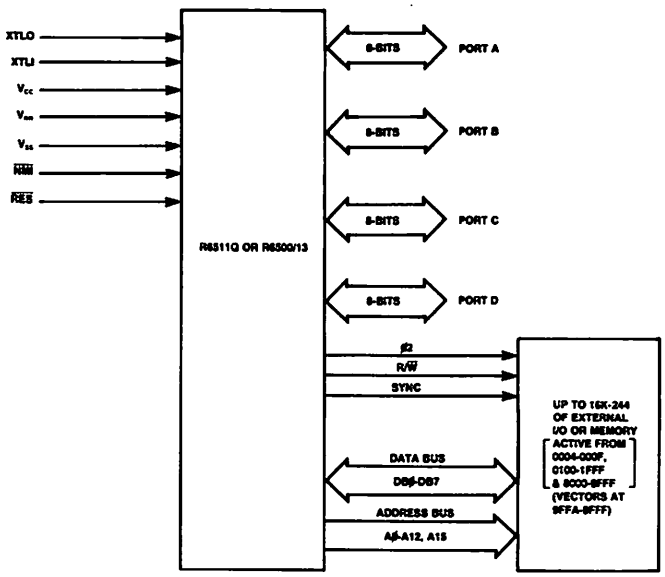


FIGURE 4-1b. Normal Bus Mode

TABLE 4-4. Port C Control and Usage

		FULL ADDRESS MODE		I/O MODE	
		MCR7 0 MCR6 0		MCR7 0 MCR6 1	
PIN #	PIN NAME	SIGNAL		SIGNAL	
		NAME	TYPE	NAME	TYPE (1)
54	PC0	PC0	I/O (1)	PC0	I O
55	PC1	PC1	I O (1)	PC1	I O
56	PC2	PC2	I/O (1)	PC2	I O
57	PC3	PC3	I/O (1)	PC3	I O
58	PC4	PC4	I/O (1)	PC4	I O
59	PC5	PC5	I/O (1)	PC5	I O
60	PC6	A13	OUTPUT (2)	PC6	I O
61	PC7	A14	OUTPUT (2)	PC7	I O

NOTES:
1. Resistive Pull-Up, Active Buffer Pull-Down
2. Active Buffer Pull-Up and Pull-Down

TABLE 4-5. Port D Control and Usage

		I/O MODES			
		MCR7 = 0 MCR6 = X MCR5 = 0		MCR7 = 0 MCR6 = X MCR5 = 1	
PIN #	PIN NAME	SIGNAL		SIGNAL	
		NAME	TYPE (1)	NAME	TYPE (2)
62	PD0	PD0	INPUT	PD0	OUTPUT
63	PD1	PD1	INPUT	PD1	OUTPUT
64	PD2	PD2	INPUT	PD2	OUTPUT
1	PD3	PD3	INPUT	PD3	OUTPUT
2	PD4	PD4	INPUT	PD4	OUTPUT
3	PD5	PD5	INPUT	PD5	OUTPUT
4	PD6	PD6	INPUT	PD6	OUTPUT
5	PD7	PD7	INPUT	PD7	OUTPUT

NOTES:
1. Tri-State Buffer is in High Impedance Mode
2. Tri-State Buffer is in Active Mode

SECTION 5
SERIAL INPUT/OUTPUT CHANNEL

The device provides a full duplex Serial I/O channel with programmable bit rates and operating modes. The serial I/O functions are controlled by the Serial Communication Control Register (SCCR). The SCCR bit assignment is shown in Figure 5-1. The serial bit rate is determined by Counter A for all modes except the Receiver Shift Register (RCVR S/R) mode for which an external shift clock must be provided. The maximum data rate using the internal clock is 62.5K bits per second (at $\phi 2$ = 1 MHZ). The transmitter (XMTR) and receiver (RCVR) can be independently programmed to operate in different modes and can be independently enabled or disabled.

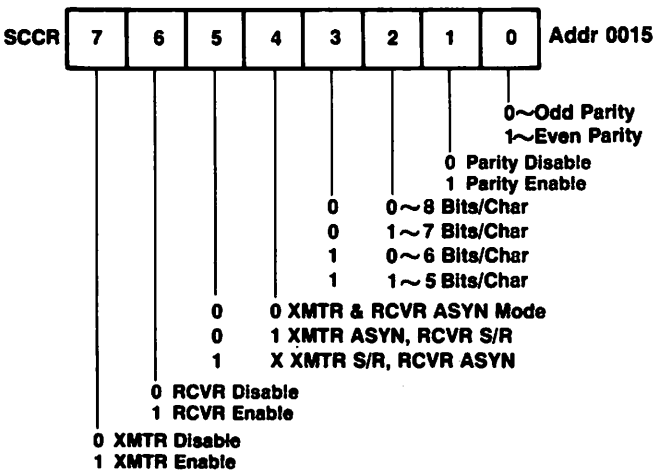


FIGURE 5-1. Serial Communication Control Register

Except for the Receiver Shift Register Mode (RCVR S/R), all XMTR and RCVR bit rates will occur at one sixteenth of the Counter A interval timer rate. Counter A is forced into an interval timer mode whenever the serial I/O is enabled in a mode requiring an internal clock.

Whenever Counter A is required as a timing source it must be loaded with the hexadecimal code that selects the data rate for the serial I/O Port. Refer to Counter A (paragraph 6.1) for a table of hexadecimal values to represent the desired data rate.

5.1 TRANSMITTER OPERATION (XTMR)

The XTMR operation and the transmitter related control/status functions are enabled by bit 7 of the Serial Communications Control Register (SCCR). The transmitter, when in the Asynchronous (ASYN) mode, automatically adds a start bit, one or two stop bits, and, when enabled, a parity bit to the transmitted data. A word of transmitted data (in asynchronous parity mode) can have 5, 6, 7, or 8 bits of data. The nine data modes are shown in Figure 5-2. When parity is disabled, the 5, 6, 7 or 8 bits of data are terminated with two stop bits.

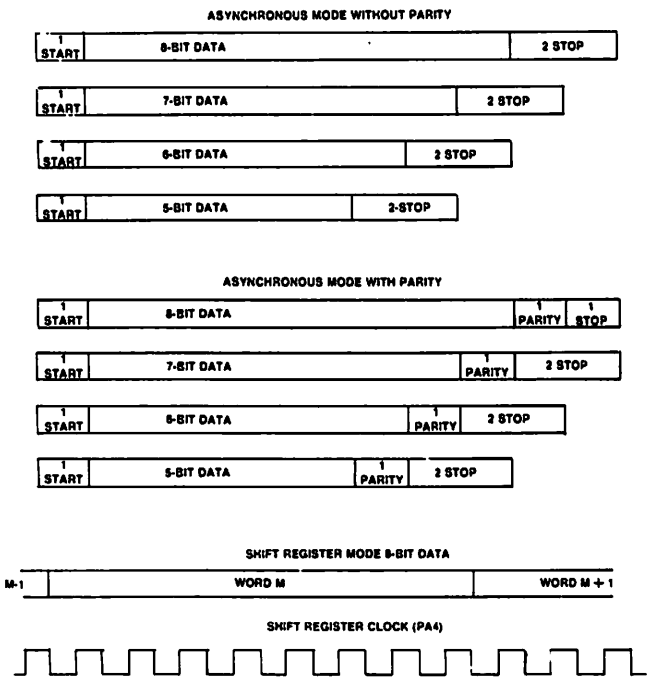


FIGURE 5-2. SIO Data Modes

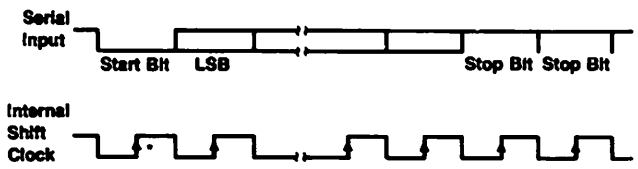
In the S/R mode, eight data bits are always shifted out. Bits/character and parity control bits are ignored. The serial data is shifted out via the SO output (PA6) and the shift clock is available at the CA (PA4) pin. When the transmitter underruns in the S/R mode the SO output and shift clock are held in a high state.

The XMTR Interrupt Flag bit (IFR7) is controlled by Serial Communication Status Register bits SCSR5, SCSR6 and SCSR7.

$$IFR7 = SCSR6\ (\overline{SCSR5} + SCSR7)$$

5.2 RECEIVER OPERATION (RCVR)

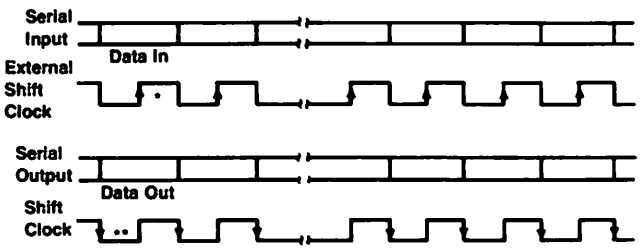
The receiver and its selected control and status functions are enabled when SCCR-6 is set to a "1." In the ASYN mode, data format must have a start bit, the appropriate number of data bits, a parity bit (if enabled), and one stop bit. Refer to paragraph 5.1 for a diagram of bit allocations. The receiver bit period is divided into 8 sub-intervals for internal synchronization. The receiver bit stream is synchronized by the start bit and a strobe signal is generated at the approximate center of each incoming bit. Refer to Figure 5-3 for ASYN Receive Data Timing. The character assembly process does not start if the start bit signal is less than one-half the bit time after a low level is detected on the Receive Data Input. Framing error, over-run, and parity error conditions or a RCVR Data Register Full will set the appropriate status bits. Any of the above conditions will cause an Interrupt Request if the Receiver Interrupt Enable bit is set to logic 1.



*Serial Input Data Shifted In

FIGURE 5-3. ASYN Receive Data Timing

In the S/R mode, an external shift clock must be provided at CA (PA4) pin along with 8 bits of serial data (LSB first) at the SI input (PA7). The maximum data rate using an external shift clock is one-eighth the internal clock rate. Refer to Figure 5-4 for S/R Mode Timing.



* Serial Input Data Shifted In
** Serial Output Data Makes Transition

FIGURE 5-4. S/R Mode Timing

A RCVR interrupt (IFR6) is generated whenever any of SCSR0-3 are true.

5.3 SERIAL COMMUNICATION STATUS REGISTER (SCSR)

The Serial Communication Status Register (SCSR) holds information on various communication error conditions, status of the transmitter and receiver data registers, a transmitter end-of-transmission condition, and a receiver idle line condition (Wake-Up Feature). The SCSR bit assignment is shown in Figure 5-5. Bit assignments and functions of the SCSR are as follows:

SCSR 0: *Receiver Data Register Full*—Set to a logic 1 when a character is transferred from the Receiver Shift Register to the Receiver Data Register. This bit is cleared by reading the Receiver Data Register, or by $\overline{RES}$ and is disabled if SCCR 6 = 0. The SCSR 0 bit will not be set to a logic 1 if the received data contains an error condition; instead, a corresponding error bit will be set to a logic 1.

SCSR 1: *Over-Run Error*—Set to a logic 1 when a new character is transferred from the Receiver Shift Register with the last character still in the Receiver Data Register. This bit is cleared by reading the Receiver Data Register or by $\overline{RES}$.

SCSR 2: *Parity Error*—Set to logic 1 when the RCVR is in the ASYN Mode, Parity Enable bit is set, and the received data has a parity error. This bit is cleared by reading the Receiver Data Register or by $\overline{RES}$.

SCSR 3: *Framing Error*—Set to a logic 1 when the received data contains a zero bit after the last data or parity bit in the stop bit slot. Cleared by reading the Receiver Data Register or by $\overline{RES}$ (ASYN Mode only).

SCSR 4: *Wake-Up*—Set to a logic 1 by writing a "1" in bit 4 of address: 0016. The Wake-Up bit is cleared by $\overline{RES}$ or when the receiver detects a string of ten consecutive 1's. When the Wake-Up bit is set SCSR0 through SCSR3 are inhibited.

SCSR 5: *End of Transmission*—Set to a logic 1 by writing a "1" in bit position 5 of address: 0016. The End of Transmission bit is cleared by $\overline{RES}$ or upon writing a new data word into the Transmitter Data Register. When the End-of-Transmission bit is true the Transmitter Register Empty bit is disabled until a Transmitter Under-Run occurs.

SCSR 6: *Transmitter Data Register Empty*—Set to a logic 1 when the contents of the Transmitter Data Register are transferred to the Transmitter Shift Register. Cleared upon writing new data into the Transmit Data Register. This bit is initialized to a logic 1 by $\overline{RES}$.

SCSR 7: *Transmitter Under-Run*—Set to a logic 1 when the last data bit is transmitted if the transmitter is in a S/R Mode or when the last stop bit is transmitted if the XMTR is in the ASYN Mode while the Transmitter Data Register Empty Bit is set. Cleared by a transfer of new data into the Transmitter Shift Register or by $\overline{RES}$.

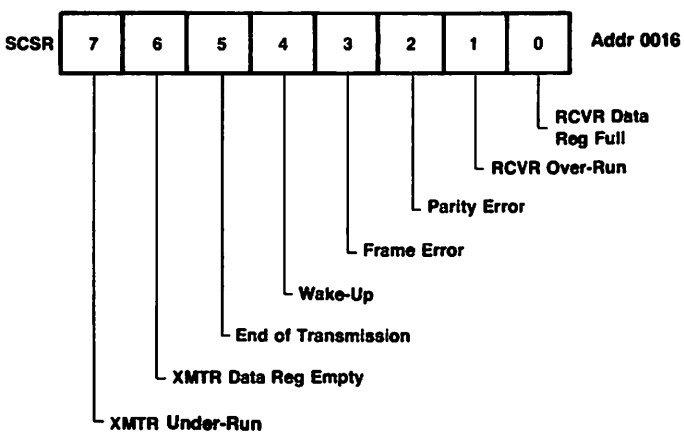


FIGURE 5-5. SCSR Bit Allocations

5.4 WAKE-UP FEATURE

In a multi-distributed microprocessor or microcomputer applications, a destination address is usually included at the beginning of the message. The Wake-Up Feature allows non-selected CPU's to ignore the remainder of the message until the beginning of the next message by setting the Wake-Up bit. As long as the Wake-Up flag is true, the Receiver Data Register Full Flag remains false. The Wake-Up bit is automatically cleared when the receiver detects a string of ten consecutive 1's which indicates an idle transmit line. When the next byte is received, the Receiver Data Register Full Flag signals the CPU to wake-up and read the received data.

SECTION 6
COUNTER/TIMERS

The device contains two 16-bit counters (Counter A and Counter B) and three 16-bit latches associated with the counters. Counter A has one 16-bit latch and Counter B has two 16-bit latches. Each counter can be independently programmed to operate in one of four modes:

Counter A	Counter B
• Pulse width measurement	• Retriggerable Interval Counter
• Pulse Generation	• Asymmetrical Pulse Generation
• Interval Timer	• Interval Timer
• Event Counter	• Event Counter

Operating modes of Counter A and Counter B are controlled by the Mode Control Register. All counting begins at the initialization value and decrements. When modes are selected requiring a counter input/output line, PA4 is automatically selected for Counter A and PA5 is automatically selected for Counter B (see Table 4.2).

6.1 COUNTER A

Counter A consists of a 16-bit counter and a 16-bit latch organized as follows: Lower Counter A (LCA), Upper Counter A (UCA), Lower Latch A (LLA), and Upper Latch A (ULA). The counter contains the count of either $\phi 2$ clock pulses or external events, depending on the counter mode selected. The contents of Counter A may be read any time by executing a read at location 0019 for the Upper Counter A and at location 001A or location 0018 for the Lower Counter A. A read at location 0018 also clears the Counter A Underflow Flag (IFR4).

The 16-bit latch contains the counter initialization value and can be loaded at any time by executing a write to the Upper Latch A at location 0019 and the Lower Latch A at location 0018. In either case, the contents of the accumulator are copied into the applicable latch register.

Counter A can be started at any time by writing to address: 001A. The contents of the accumulator will be copied into the

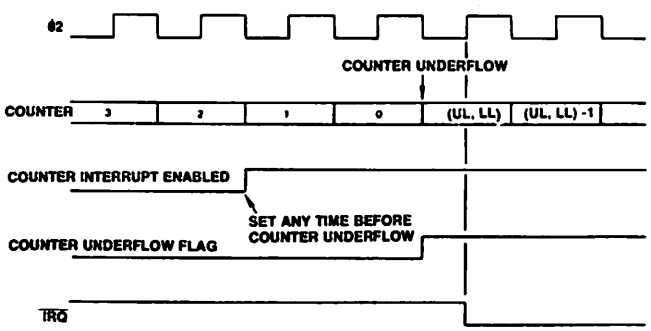


FIGURE 6-1. Interval Timer Timing Diagram

Upper Latch A before the contents of the 16-bit latch are transferred to Counter A. Counter A is set to the latch value whenever Counter A underflows. When Counter A decrements from 0000 the next counter value will be the latch value—not FFFF—and the Counter A Underflow Flag (IFR 4) will be set to "1". This bit may be cleared by reading the Lower Counter A at location 0018, by writing to address location 001A, or by $\overline{RES}$.

Counter A operates in any of four modes. These modes are selected by the Counter A Mode Control bits in the Control Register.

MCR1 (bit 1)	MCR0 (bit 0)	Mode
0	0	Interval Timer
0	1	Pulse Generation
1	0	Event Counter
1	1	Pulse Width Measurement

The Interval Timer, Pulse Generation, and Pulse Width Measurement Modes are $\phi 2$ clock counter modes. The Event Counter Mode counts the occurrences of an external event on the CNTR line.

The Counter is set to the Interval Timer Mode (00) when a $\overline{RES}$ signal is generated.

6.1.1 Interval Timer

In the Interval Timer mode the Counter is initialized to the Latch value by either of two conditions:

1. When the Counter is decremented from 0000, the next Counter value is the Latch value (not FFFF).

2. When a write operation is performed to the Load Upper Latch and Transfer Latch to Counter address 001A, the Counter is loaded with the Latch value. Note that the contents of the Accumulator are loaded into the Upper Latch before the Latch value is transferred to the Counter.

The Counter value is decremented by one count at the 02 clock rate. The 16-bit Counter can hold from 1 to 65535 counts. The Counter Timer capacity is therefore 1μs to 65.535 ms at the 1 MHz $\phi 2$ clock rate or 0.5 μs to 32.767 ms at the 2 MHz $\phi 2$ clock rate. Time intervals greater than the maximum Counter value can be easily measured by counting $\overline{IRQ}$ interrupt requests in the counter $\overline{IRQ}$ interrupt routine.

When Counter A decrements from 0000, the Counter A Underflow (IFR4) is set to logic 1. If the Counter A Interrupt Enable Bit (IER4) is also set, an $\overline{IRQ}$ interrupt request will be generated. The Counter A Underflow bit in the Interrupt Flag Register can be examined in the $\overline{IRQ}$ interrupt routine to determine that the $\overline{IRQ}$ was generated by the Counter A Underflow.

While the timer is operating in the Interval Timer Mode, PA4 operates as a PA I/O bit.

A timing diagram of the Interval Timer Mode is shown in Figure 6-1.

6.1.2 Pulse Generation Mode

In the Pulse Generation mode, the CA line operates as a Counter Output. The line toggles from low to high or from high to low whenever a Counter A Underflow occurs or a write is performed to address 001A.

The normal output waveform is a symmetrical square-wave. The CA output is initialized high when entering the mode and transitions low when writing to 001A.

Asymmetric waveforms can be generated if the value of the latch is changed after each counter underflow.

A one-shot waveform can be generated by changing from Pulse Generation to Interval Timer mode after only one occurrence of the output toggle condition.

6.1.3 Event Counter Mode

In this mode the CA is used as an Event Input line, and the Counter will decrement with each rising edge detected on this line. The maximum rate at which this edge can be detected is one-half the $\phi 2$ clock rate.

The Counter can count up to 65,535 occurrences before underflowing. As in the other modes, the Counter A Underflow bit (IER4) is set to logic 1 if the underflow occurs.

Figure 6.2 is a timing diagram of the Event Counter Mode.

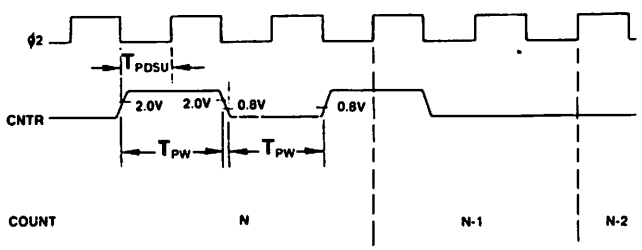


FIGURE 6-2. Event Counter Mode

6.1.4 Pulse Width Measurement Mode

This mode allows the accurate measurement of a low pulse duration on the CA line. The Counter decrements by one count at the $\phi 2$ clock rate as long as the CA line is held in the low state. The Counter is stopped when CA is in the high state.

The Counter A underflow flag will be set only when the count in the timer reaches zero. Upon reaching zero the timer will be loaded with the latch value and continue counting down as long as the CA pin is held low. After the counter is stopped by a high level on CA, the count will hold as long as CA remains high. Any further low levels on CA will again cause the counter to count down from its present value. The state of the CA line can be determined by testing the state of PA4.

A timing diagram for the Pulse Width Measurement Mode is shown in Figure 6.3.

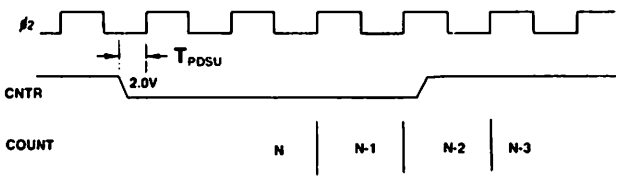


FIGURE 6-3. Pulse Width Measurement

6.1.5 Serial I/O Data Rate Generation

Counter A also provides clock timing for the Serial I/O which establishes the data rate for the Serial I/O port. When the Serial I/O is enabled, Counter A is forced to operate at the internal clock rate. Counter A is not required for the RCVR S/R mode. The Counter I/O (PA4) may also be required to support the Serial I/O (see Table 4-2).

Table 6-1 identifies the values to be loaded in Counter A for selecting standard data rates with a $\phi 2$ clock rate of 1 MHz and 2 MHz. Although Table 6-1 identifies only the more common data rates, any data rate from 1 to 62.5K bps can be selected by using the formula:

$$N = \frac{\phi 2}{16 \times \text{bps}} - 1$$

where

N = decimal value to be loaded into Counter A using its hexadecimal equivalent.
$\phi 2$ = the clock frequency (1 MHz or 2 MHz)
bps = the desired data rate.

NOTE

In Table 6-1 you will notice that the standard data rate and the actual data rate may be slightly different. Transmitter and receiver errors of 1.5% or less are acceptable. A revised clock rate is included in Table 6-1 for those baud rates which fall outside this limit.

TABLE 6-1. Counter A Values for Baud Rate Selection

STANDARD BAUD RATE	HEXADECIMAL VALUE		03 ACTUAL BAUD RATE AT		CLOCK RATE NEEDED TO GET STANDARD BAUD RATE	
	1 MHz	2 MHz	1 MHz	2 MHz	1 MHz	2 MHz
50	04E1	09C3	50.00	50.00	1.0000	2.0000
75	0340	0682	75.03	74.99	1.0000	2.0000
110	0237	046F	110.04	110.04	1.0000	2.0000
150	01A0	0340	149.88	150.06	1.0000	2.0000
300	00CF	01A0	300.48	299.76	1.0000	2.0000
600	0067	00CF	600.96	600.96	1.0000	2.0000
1200	0033	0067	1201.92	1201.92	1.0000	2.0000
2400	0019	0033	2403.85	2403.85	1.0000	2.0000
3600	0010	0021	3676.47	3676.47	0.9792	1.9584
4800	000C	0019	4807.69	4807.69	1.0000	2.0000
7200	0008	0010	6944.44	7352.94	1.0368	1.9584
9600	0006	000C	8928.57	9615.38	1.0752	2.0000

6.2 COUNTER B

Counter B consists of a 16-bit counter and two 16-bit latches organized as follows: Lower Counter B (LCB), Upper Counter B (UCB), Lower Latch B (LLB), Upper Latch B (ULB), Lower Latch C (LLC), and Upper Latch C (ULC). Latch C is used only in the asymmetrical pulse generation mode. The counter contains the count of either ø2 clock pulses or external events depending on the counter mode selected. The contents of Counter B may be read any time by executing a Read at location 001D for the Upper Counter B and at location 001E or 001C for the Lower Counter B. A Read at location 001C also clears the Counter B Underflow Flag.

Latch B contains the counter initialization value and can be loaded at any time by executing a Write to the Upper Latch B at location 001D and the Lower Latch B at location 001C. In each case, the contents of the accumulator are copied into the applicable latch register.

Counter B can be initialized at any time by writing to address: 001E. The contents of the accumulator is copied into the Upper Latch B before the value in the 16-bit Latch B is transferred to Counter B. Counter B will also be set to the latch value and the Counter B Underflow Flag bit (IFR5) will be set to a "1" whenever Counter B underflows by decrementing from 0000.

IFR 5 may be cleared by reading the Lower Counter B at location 001C, by writing to address location 001E, or by $\overline{RES}$.

Counter B operates in the same manner as Counter A in the Interval Timer and Event Counter modes. The Pulse Width Measurement Mode is replaced by the Retriggerable Interval Timer mode and the Pulse Generation mode is replaced by the Asymmetrical Pulse Generation Mode. Mode Control Register bits MCR2 and MCR3 select the four Counter B modes in a similar manner and coding as MCR0 and MCR1 select the modes of Counter A.

6.2.1 Retriggerable Interval Timer Mode

When operating in the Retriggerable Interval Timer mode, Counter B is initialized to the latch value by writing to address 001E, by a Counter B underflow, or whenever a positive edge occurs on the CB pin (PA5). The Counter B interrupt flag will be set if the counter underflows before a positive edge occurs on the CB line. Figure 6-4 illustrates the operation.

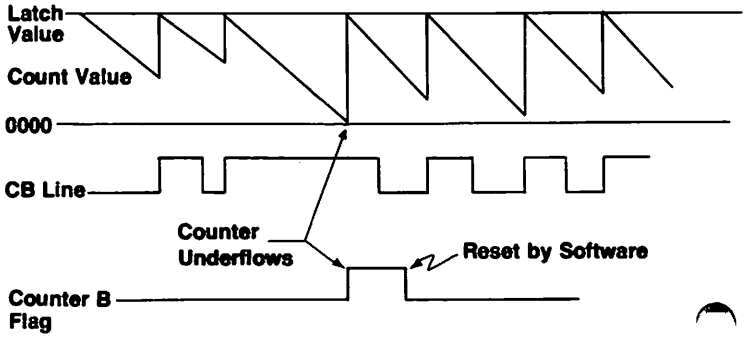


FIGURE 6-4. Counter B. Retriggerable Interval Timer Mode

6.2.2 Asymmetrical Pulse Generation Mode

Counter B has a special Asymmetrical Pulse Generation Mode whereby a pulse train with programmable pulse width and period can be generated without the processor intervention once the latch values are initialized.

In this mode, the 16-bit Latch B is initialized with a value which corresponds to the duration between pulses (referred to as D in the following descriptions). The 16-bit Latch C is initialized with a value corresponding to the desired pulse width (referred to as P in the following descriptions). The initialization sequence for Latch B and C and the starting of a counting sequence are as follows:

1. The lower 8 bits of P are loaded into LLB by writing to address 001C; the upper 8 bits of P are loaded into ULB and the full 16 bits are transferred to Latch C by writing to address location 001D. At this point both Latch B and Latch C contain the value of P.

2. The lower 8 bits of D are loaded into LLB by writing to address 001C; the upper 8 bits of D are loaded into ULB by writing to address location 001E. Writing to address location 001E also causes the contents of the 16-bit Latch B to be downloaded into the Counter B and the CB output to go low as shown in Figure 6-5.

3. When Counter B underflow occurs the contents of the Latch C are loaded into the Counter B and the CB output toggles to a high level, staying high until another underflow occurs. Latch B is then down-loaded and the CB output toggles to a low level repeating the whole process.

SECTION 7
POWER ON/INITIALIZATION CONSIDERATIONS

7.1 POWER ON TIMING

After application of V_{CC} and V_{RR} power to the device, $\overline{RES}$ must be held low for at least eight $\phi 2$ clock cycles after V_{CC} reaches operating range and the internal oscillator has stabilized. This stabilization time is dependent upon the input V_{CC} voltage and performance of the internal oscillator. The clock can be monitored at $\phi 2$ (pin 3). Figure 7-1 illustrates the power turn-on waveforms. Clock stabilization time is typically 20 ms.

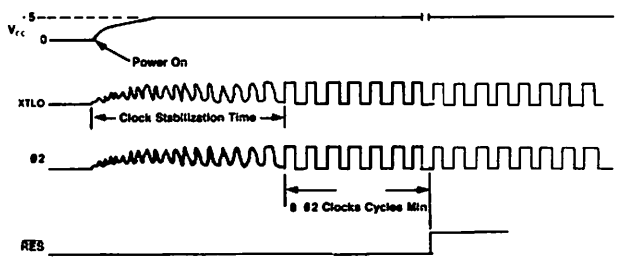


FIGURE 7-1. Power Turn-On Timing Detail

7.2 POWER-ON RESET

When $\overline{RES}$ goes from low to high, the device sets the Interrupt Mask Bit—bit 2 of the Processor Status Register—and initiates a reset vector fetch at address FFFC and FFFD to begin user program execution. All of the I/O ports (PA, PB, PC, PD) will be forced to the high (logic 1) state. All bits of the Control Register will be cleared to logic 0 causing the Interval Timers counter mode (mode 00) to be selected and all interrupt enabled bits to be reset.

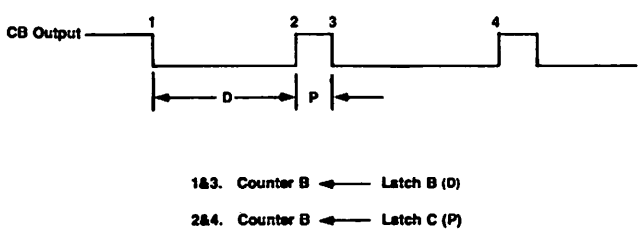


FIGURE 6-5. Counter B Pulse Generation

7.3 RESET ($\overline{RES}$) CONDITIONING

When $\overline{RES}$ is driven from low to high the device is put in a reset state causing the registers and I/O ports to be configured as shown in Table 7-1.

TABLE 7-1. $\overline{RES}$ Initialization of I/O Ports and Registers

	7	6	5	4	3	2	1	0
REGISTERS								
Processor Status	—	—	—	—	—	1	—	—
Mode Control (MCR)	0	0	0	0	0	0	0	0
Int. Enable (IER)	0	0	0	0	0	0	0	0
Int. Flag (IFR)	0	0	0	0	0	0	0	0
Ser. Com. Control (SCCR)	0	0	0	0	0	0	0	0
Ser. Com. Status (SCSR)	0	1	0	0	0	0	0	0
PORTS								
PA Latch	1	1	1	1	1	1	1	1
PB Latch	1	1	1	1	1	1	1	1
PC Latch	1	1	1	1	1	1	1	1
PD Latch	1	1	1	1	1	1	1	1

All RAM and other CPU registers will initialize in a random, non-repeatable data pattern.

7.4 INITIALIZATION

Any initialization process for the device should include a $\overline{RES}$, as indicated in the preceeding paragraphs. After stabilization of the internal clock (if a power on situation) an initialization routine should be executed to perform (as a minimum) the following functions:

1. The Stack Pointer should be set
2. Clear or Set Decimal Mode
3. Set or Clear Carry Flag
4. Set up Mode Controls as required
5. Clear Interrupts

A typical initialization subroutine could be as follows:

```
LDX     Load stack pointer starting address into
        X Register
TXS     Transfer X Register value to Stack Pointer
CLD     Clear Decimal Mode
SEC     Set Carry Flag
....    Set-up Mode Control and
....    special function registers
....    and clear RAM as required
CLI     Clear Interrupts
```

APPENDIX A
ENHANCED R6502 INSTRUCTION SET

This appendix contains a summary of the Enhanced R6502 instruction set. For detailed information, consult the R6502 Microcomputer System Programming Manual, Document 29650 N30. The four instructions notated with a * are added instructions to enhance the standard 6502 instruction set.

A.1 INSTRUCTION SET IN ALPHABETIC SEQUENCE

ADC	Add Memory to Accumulator with Carry
AND	"AND" Memory with Accumulator
ASL	Shift Left One Bit (Memory or Accumulator)
*BBR	Branch on Bit Reset Relative
*BBS	Branch on Bit Set Relative
BCC	Branch on Carry Clear
BCS	Branch on Carry Set
BEQ	Branch on Result Zero
BIT	Test Bits in Memory with Accumulator
BMI	Branch on Result Minus
BNE	Branch on Result not Zero
BPL	Branch on Result Plus
BRK	Force Break
BVC	Branch on Overflow Clear
BVS	Branch on Overflow Set
CLC	Clear Carry Flag
CLD	Clear Decimal Mode
CLI	Clear Interrupt Disable Bit
CLV	Clear Overflow Flag
CMP	Compare Memory and Accumulator
CPX	Compare Memory and Index X
CPY	Compare Memory and Index Y
DEC	Decrement Memory by One
DEX	Decrement Index X by One
DEY	Decrement Index Y by One
EOR	"Exclusive-Or" Memory with Accumulator
INC	Increment Memory by One
INX	Increment Index X by One
INY	Increment Index Y by One
JMP	Jump to New Location
JSR	Jump to New Location Saving Return Address
LDA	Load Accumulator with Memory
LDX	Load Index X with Memory
LDY	Load Index Y with Memory
LSR	Shift One Bit Right (Memory or Accumulator)
NOP	No Operation
ORA	"OR" Memory with Accumulator
PHA	Push Accumulator on Stack
PHP	Push Processor Status on Stack
PLA	Pull Accumulator from Stack
PLP	Pull Processor Status from Stack
*RMB	Reset Memory Bit
ROL	Rotate One Bit Left (Memory or Accumulator)
ROR	Rotate One Bit Right (Memory or Accumulator)
RTI	Return from Interrupt
RTS	Return from Subroutine
SBC	Subtract Memory from Accumulator with Borrow
SEC	Set Carry Flag
SED	Set Decimal Mode
SEI	Set Interrupt Disable Status
*SMB	Set Memory Bit
STA	Store Accumulator in Memory
STX	Store Index X in Memory
STY	Store Index Y in Memory
TAX	Transfer Accumulator to Index X
TAY	Transfer Accumulator to Index Y
TSX	Transfer Stack Pointer to Index X
TXA	Transfer Index X to Accumulator
TXS	Transfer Index X to Stack Register
TYA	Transfer Index Y to Accumulator

A.2 INSTRUCTION SET SUMMARY TABLE

ENHANCED R6502 INSTRUCTION SET

INSTRUCTIONS		IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM.			IMPLIED			(IND, X)			(IND), Y			Z. PAGE, X			ABS, X			ABS, Y			RELATIVE			INDIRECT			Z. PAGE, Y			BIT ADDRESSING (OP BY BIT #)								PROCESSOR STATUS CODES							
MNEMONIC	OPERATION	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	0	1	2	3	4	5	6	7	7	6	5	4	3	2	1	0
																																																		N	V	-	-	-	-	Z	C
ADC	A + M + C → A (4)(1)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3																										
AND	A M → A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3																										
ASL	C ← [7 6 5 4 3 2 1 0] ← 0				0E	6	3	06	5	2	0A	2	1										16	6	2	1E	7	3																														
BBR[#(0-7)]	Branch on M_n 0 (5)(2)																																																							
BBS[#(0-7)]	Branch on M_n 1 (5)(2)																																																						
BCC	Branch on C 0 (2)																															90	2	2																							
BCS	Branch on C 1 (2)																															B0	2	2																							
BEQ	Branch on Z 1 (2)																															F0	2	2																							
BIT	A ∧ M				2C	4	3	24	3	2																																											M	M.	-	-	-	Z	-
BMI	Branch on N 1 (2)																															30	2	2																							
BNE	Branch on Z 0 (2)																															D0	2	2																							
BPL	Branch on N 0 (2)																															10	2	2																							
BRK	Break (See Fig. 1)													00	7	1																																										
BVC	Branch on V 0 (2)																															50	2	2																							
BVS	Branch on V 1 (2)																															70	2	2																							
CLC	0 → C													18	2	1																																										
CLD	0 → D													D8	2	1																																									
CLI	0 → I													58	2	1																																									
CLV	0 → V													B8	2	1																																									
CMP	A M (1)	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3																										
CPX	X M	E0	2	2	EC	4	3	E4	3	2																																															
CPY	Y M	C0	2	2	CC	4	3	C4	3	2																																															
DEC	M 1 → M				CE	6	3	C6	5	2													D6	6	2	DE	7	3																														
DEX	X 1 → X													CA	2	1																																									
DEY	Y 1 → Y													88	2	1																																								
EOR	A ⊻ M → A (1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3																										
INC	M + 1 → M				EE	6	3	E6															F6	6	2	FE	7	3																														
INX	X + 1 → X													EB	2	1																																									
INY	Y + 1 → Y													C8	2	1																																								
JMP	Jump to New Loc				4C	3	3																															6C	5	3																		
JSR	Jump Sub (See Fig. 2)				20	6	3																																																		
LDA	M → A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3																										
LDX	M → X (1)	A2	2	2	AE	4	3	A6	3	2																			BE	4	3							B6	4	2																		
LDY	M → Y (1)	A0	2	2	AC	4	3	A4	3	2													B4	4	2	BC	4	3																														
LSR	0 → [7 6 5 4 3 2 1 0] → C				4E	6	3	46	5	2	4A	2	1										56	6	2	5E	7	3																														
NOP	No Operation													EA	2	1																																								
ORA	A ∨ M → A (1)	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3																										
PHA	A → M_S S − 1 → S													48	3	1																																								
PHP	P → M_S S − 1 → S													08	3	1																																								
PLA	S + 1 → S M_S → A													68	4	1																																								
PLP	S + 1 → S M_S → P													28	4	1																																								
RMB[#(0-7)]	0 → M_n (5)																																																							
R0L	[7 6 5 4 3 2 1 0] ← C				2E	6	3	26	5	2	2A	2	1										36	6	2	3E	7	3																														
R0R	C → [7 6 5 4 3 2 1 0]				6E	6	3	66	5	2	6A	2	1										76	6	2	7E	7	3																														
RTI	Rtrn Int (See Fig. 1)													40	6	1																																								
RTS	Rtrn Sub (See Fig. 2)													60	6	1																																								
SBC	A M C → A (1)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3																										
SEC	1 → C													38	2	1																																								
SED	1 → D													F8	2	1																																								
SEI	1 → T													78	2	1																																								
SMB[#(0-7)]	1 → M_n (5)																																																						
STA	A → M				8D	4	3	85	3	2							81	6	2	91	6	2	95	4	2	9D	5	3	[illegible]	5	3																										
STX	X → M				8E	4	3	86	3	2																													96	4	2																		
STY	Y → M				8C	4	3	84	3	2													94	4	2																																		
TAX	A → X													AA	2	1																																								
TAY	A → Y													A8	2	1																																								
TSX	S → X													BA	2	1																																								
TXA	X → A													8A	2	1																																								
TXS	X → S													9A	2	1																																								
TYA	Y → A													98	2	1																																								

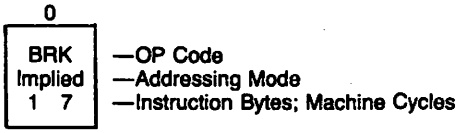
NOTES

1. Add 1 to N if page boundary is crossed
2. Add 1 to N if branch occurs to same page
   Add 2 to N if branch occurs to different page
3. Carry not = Borrow
4. If in decimal mode Z flag is invalid
   accumulator must be checked on zero result.
5. Effects 8-bit data field of the specified zero page address.

LEGEND

X	= Index X	M_6	= Memory Bit 6		
Y	= Index Y	•	Add		
A	= Accumulator		Subtract		
M	= Memory per effective address	∧	= And		
M_s	= Memory per stack pointer	∨	= Or		
M_b	= Selecter zero page memory bit	⊻	= Exclusive Or		
M_7	= Memory Bit 7	n	= Number of cycles		
		#	= Number of Bytes		

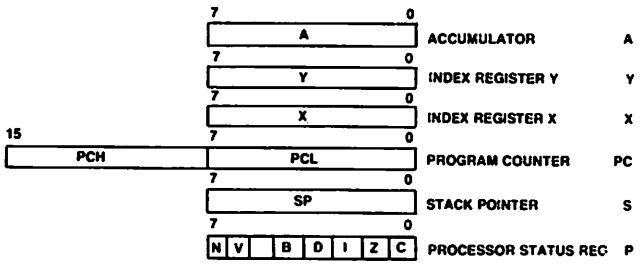
A.3 INSTRUCTION CODE MATRIX



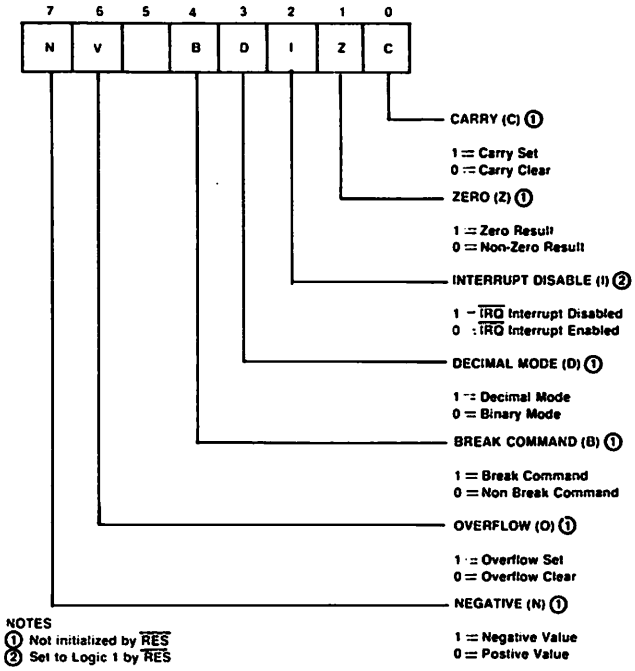
MSD \ LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	MSD
0	BRK Implied 1 7	ORA (IND, X) 2 6				ORA ZP 2 3	ASL ZP 2 5	RMB0 ZP 2 5	PHP Implied 1 3	ORA IMM 2 2	ASL Accum 1 2			ORA ABS 3 4	ASL ABS 3 6	BBR0 ZP 3 5**	0
1	BPL Relative 2 2**	ORA (IND), Y 2 5*				ORA ZP, X 2 4	ASL ZP, X 2 6	RMB1 ZP 2 5	CLC Implied 1 2	ORA ABS, Y 3 4*				ORA ABS, X 3 4*	ASL ABS, X 3 7	BBR1 ZP 3 5**	1
2	JSR Absolute 3 6	AND (IND, X) 2 6			BIT ZP 2 3	AND ZP 2 3	ROL ZP 2 5	RMB2 ZP 2 5	PLP Implied 1 4	AND IMM 2 2	ROL Accum 1 2		BIT ABS 3 4	AND ABS 3 4	ROL ABS 3 6	BBR2 ZP 3 5**	2
3	BMI Relative 2 2**	AND (IND, Y) 2 5*				AND ZP, X 2 4	ROL ZP, X 2 6	RMB3 ZP 2 5	SEC Implied 1 2	AND ABS, Y 3 4*				AND ABS, X 3 4*	ROL ABS, X 3 7	BBR3 ZP 3 5**	3
4	RTI Implied 1 6	EOR (IND, X) 2 6				EOR ZP 2 3	LSR ZP 2 5	RMB4 ZP 2 5	PHA Implied 1 3	EOR IMM 2 2	LSR Accum 1 2		JMP ABS 3 3	EOR ABS 3 4	LSR ABS 3 6	BBR4 ZP 3 5**	4
5	BVC Relative 2 2**	EOR (IND), Y 2 5*				EOR ZP, X 2 4	LSR ZP, X 2 6	RMB5 ZP 2 5	CLI Implied 1 2	EOR ABS, Y 3 4*				EOR ABS, X 3 4*	LSR ABS, X 3 7	BBR5 ZP 3 5**	5
6	RTS Implied 1 6	ADC (IND, X) 2 6				ADC ZP 2 3	ROR ZP 2 5	RMB6 ZP 2 5	PLA Implied 1 4	ADC IMM 2 2	ROR Accum 1 2		JMP Indirect 3 5	ADC ABS 3 4	ROR ABS 3 6	BBR6 ZP 3 5**	6
7	BVS Relative 2 2**	ADC (IND, Y) 2 5*				ADC ZP, X 2 4	ROR ZP, X 2 6	RMB7 ZP 2 5	SEI Implied 1 2	ADC ABS, Y 3 4*				ADC ABS, X 3 4*	ROR ABS, X 3 7	BBR7 ZP 3 5**	7
8		STA (IND, X) 2 6			STY ZP 2 3	STA ZP 2 3	STX ZP 2 3	SMB0 ZP 2 5	DEY Implied 1 2		TXA Implied 1 2		STY ABS 3 4	STA ABS 3 4	STX ABS 3 4	BBS0 ZP 3 5**	8
9	BCC Relative 2 2**	STA (IND, Y) 2 6			STY ZP, X 2 4	STA ZP, X 2 4	STX ZP, Y 2 4	SMB1 ZP 2 5	TYA Implied 1 2	STA ABS, Y 3 5	TXS Implied 1 2			STA ABS, X 3 5		BBS1 ZP 3 5**	9
A	LDY IMM 2 2	LDA (IND, X) 2 6	LDX IMM 2 2		LDY ZP 2 3	LDA ZP 2 3	LDX ZP 2 3	SMB2 ZP 2 5	TAY Implied 1 2	LDA IMM 2 2	TAX Implied 1 2		LDY ABS 3 4	LDA ABS 3 4	LDX ABS 3 4	BBS2 ZP 3 5**	A
B	BCS Relative 2 2**	LDA (IND), Y 2 5*			LDY ZP, X 2 4	LDA ZP, X 2 4	LDX ZP, Y 2 4	SMB3 ZP 2 5	CLV Implied 1 2	LDA ABS, Y 3 4*	TSX Implied 1 2		LDY ABS, X 3 4*	LDA ABS, X 3 4*	LDX ABS, Y 3 4*	BBS3 ZP 3 5**	B
C	CPY IMM 2 2	CMP (IND, X) 2 6			CPY ZP 2 3	CMP ZP 2 3	DEC ZP 2 5	SMB4 ZP 2 5	INY Implied 1 2	CMP IMM 2 2	DEX Implied 1 2		CPY ABS 3 4	CMP ABS 3 4	DEC ABS 3 6	BBS4 ZP 3 5**	C
D	BNE Relative 2 2**	CMP (IND), Y 2 5*				CMP ZP, X 2 4	DEC ZP, X 2 6	SMB5 ZP 2 5	CLD Implied 1 2	CMP ABS, Y 3 4*				CMP ABS, X 3 4*	DEC ABS, X 3 7	BBS5 ZP 3 5**	D
E	CPX IMM 2 2	SBC (IND, X) 2 6			CPX ZP 2 3	SBC ZP 2 3	INC ZP 2 5	SMB6 ZP 2 5	INX Implied 1 2	SBC IMM 2 2	NOP Implied 1 2		CPX ABS 3 4	SBC ABS 3 4	INC ABS 3 6	BBS6 ZP 3 5**	E
F	BEQ Relative 2 2**	SBC (IND), Y 2 5*				SBC ZP, X 2 4	INC ZP, X 2 6	SMB7 ZP 2 5	SED Implied 1 2	SBC ABS, Y 3 4*				SBC ABS, X 3 4*	INC ABS, X 3 7	BBS7 ZP 3 5**	F
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

*Add 1 to N if page boundary is crossed.
**Add 1 to N if branch occurs to same page;
add 2 to N if branch occurs to different page.

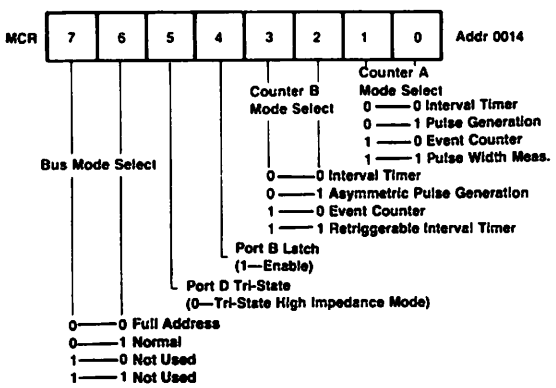
APPENDIX B
KEY REGISTER SUMMARY



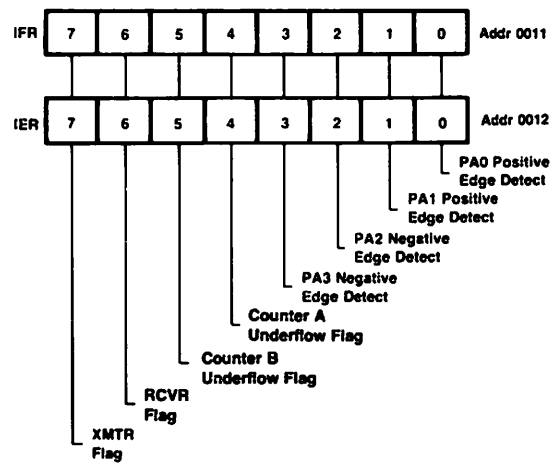
CPU Registers



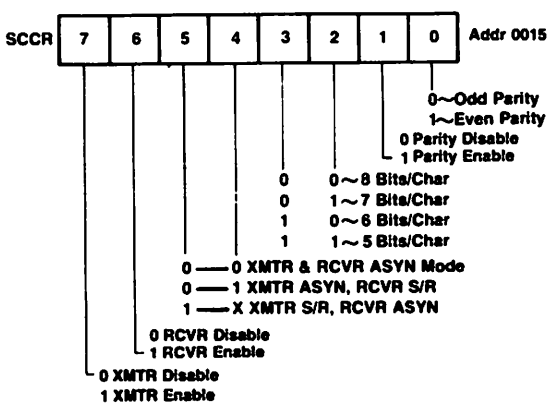
Processor Status Register



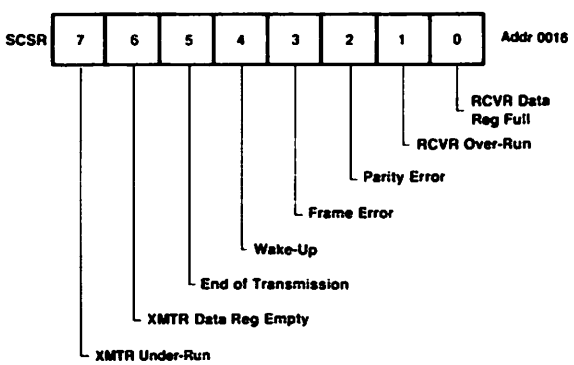
Mode Control Register



Interrupt Enable and Flag Registers



Serial Communications Control Register



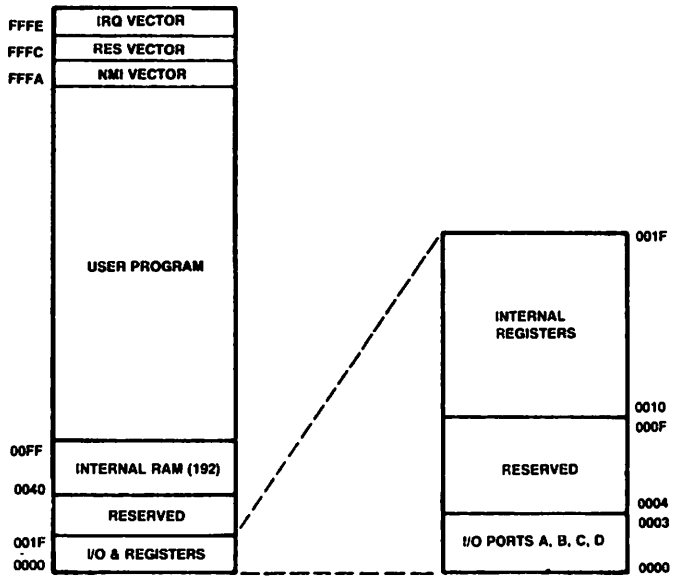
Serial Communications Status Register

APPENDIX C
ADDRESS ASSIGNMENTS/MEMORY MAPS/PIN FUNCTIONS

C.1 I/O AND INTERNAL REGISTER ADDRESSES

ADDRESS (HEX)	READ	WRITE
001F	— —	— —
1E	Lower Counter B	Upper Latch B, Cntr B←Latch B, CLR Flag
1D	Upper Counter B	Upper Latch B, Latch C←Latch B
1C	Lower Counter B, CLR Flag	Lower Latch B.
1B	— —	— —
1A	Lower Counter A	Upper Latch A, Cntr A←Latch A, CLR Flag
19	Upper Counter A	Upper Latch A
18	Lower Counter A, CLR Flag	Lower Latch A
17	Serial Receiver Data Register	Serial Transmitter Data Register
16	Serial Comm. Status Register	Serial Comm. Status Reg. Bits 4 & 5 only
15	Serial Comm. Control Register	Serial Comm. Control Register
14	Mode Control Register	Mode Control Register
13	— —	— —
12	Interrupt Enable Register	Interrupt Enable Register
11	Interrupt Flag Register	— —
0010	Read FF	Clear Int Flag (Bits 0-3 only, Write 0's only)
0F 0E 0D 0C	**RESERVED** These addresses are reserved and are used by the CPU during Read and Write operation over the external Data Bus (D0-D7).	
0B 0A 09 08		
07 06 05 04		
03	Port D	Port D
02	Port C	Port C
01	Port B	Port B
0000	Port A	Port A

C.2 FULL ADDRESS MODE MEMORY MAP R6501Q



C.4 MULTIPLE FUNCTION PIN ASSIGNMENTS —PORT C AND PORT D

PIN NUMBER	FULL ADDRESS MODE	I/O PORT FUNCTION
54	PC0	PC0
55	PC1	PC1
56	PC2	PC2
57	PC3	PC3
58	PC4	PC4
59	PC5	PC5
60	A13	PC6
61	A14	PC7
62	PD0	PD0
63	PD1	PD1
64	PD2	PD2
1	PD3	PD3
2	PD4	PD4
3	PD5	PD5
4	PD6	PD6
5	PD7	PD7

APPENDIX D
ELECTRICAL SPECIFICATIONS

Maximum Ratings

RATING	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC} & V_{RR}	−0.3 to +7.0	Vdc
Input Voltage	V_{in}	−0.3 to +7.0	Vdc
Operating Temperature Range, Commercial		0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

NOTE: This device contains circuitry to protect the inputs against damage due to high static voltages; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

D.C. Characteristics (V_{CC} = 5V ±5%; V_{RR} = V_{CC}; V_{SS} = 0; TA = 0 to 70°C)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
Power Dissipation (Outputs High) Commercial @ 0°C	P_D	—	750[1]	1100	mW
RAM Standby Voltage (Retention Mode)	V_{RR}	3.0	—	V_{CC}	Vdc
RAM Standby Current (Retention Mode) Commercial @ 25°C	I_{RR}	—	4	—	mAdc
Input High Voltage (Except XTLI)	V_{IH}	+2.0	—	V_{CC}	Vdc
Input High Voltage (XTLI)	V_{IH}	+4.0	—	V_{CC}	Vdc
Input Low Voltage	V_{IL}	−0.3	—	+0.8	Vdc
Input Leakage Current ($\overline{RES}$, $\overline{NMI}$) V_{in} = 0 to 5.0 Vdc	I_{IN}			±10.0	μAdc
Input Low Current PA, PB, PC, PD (V_{IL} = 0.4 Vdc)	I_{IL}	—	−1.0	−1.6	mAdc
Output High Voltage (Except XTLO) (I_{Load} = .100 μAdc)	V_{OH}	+2.4	—	V_{CC}	Vdc
Output Low Voltage (I_{Load} = 1.6 mAdc)	V_{OL}	—	—	+0.4	Vdc
Input Capacitance (V_{in} −0, T_A = 25°C, f = 1.0 MHz) XTLI, XTLO All Others	C_{in}	 — —	 — —	 50 10	pF
I/O Port Pull-Up Resistance PA0-PA7, PB0-PB7, PC0-PC7	R_L	3.0	6.0	11.5	KΩ
Output Leakage Current Tri-State I/O's while in High Impedance State	I_{OUT}	—	—	±10	μAdc
Output Capacitance Tri-State I/O's while in High Impedance State V_{IN} = 0V, TA = 25°C, f = 1.0 MHz	C_{OUT}	—	—	10	pF

NOTE: Negative sign indicates outward current flow, positive indicates inward flow.
(1) at 25°C

APPENDIX E
TIMING REQUIREMENTS AND CHARACTERISTICS

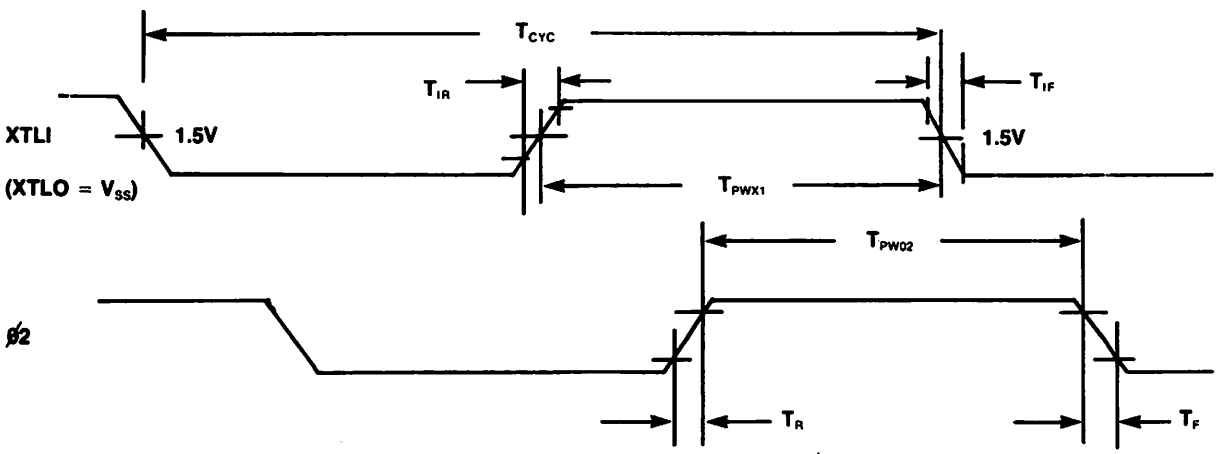
E.1 GENERAL NOTES

1. V_{CC} = 5V ±5%, 0°C ≤ TA ≤ 70°C
2. A valid V_{CC} – $\overline{RES}$ sequence is required before proper operation is achieved.
3. All timing reference levels are 0.8V and 2.0V, unless otherwise specified.
4. All time units are nanoseconds, unless otherwise specified.
5. All capacitive loading is 130pf maximum, except as noted below:

PA, PB	—	50pf maximum
PC (I/O Modes Only)	—	50pf maximum
PC (ABB and Mux Mode)	—	130pf maximum
PC6, PC7 (Full Address Mode)	—	130pf maximum

E.2 CLOCK TIMING

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{CYC}	Cycle Time	1000	10 μs	500	10 μs
T_{PWX1}	XTLI Input Clock Pulse Width XTLO = VSS	500 ± 25	—	250 ± 10	—
T_{PW02}	Output Clock Pulse Width at Minimum T_{CYC}	T_{PWX1}	T_{PWX1} ± 25	T_{PWX1}	T_{PWX1} ± 20
T_R, T_F	Output Clock Rise, Fall Time	—	25	—	15
T_{IR}, T_{IF}	Input Clock Rise, Fall Time	—	10	—	10

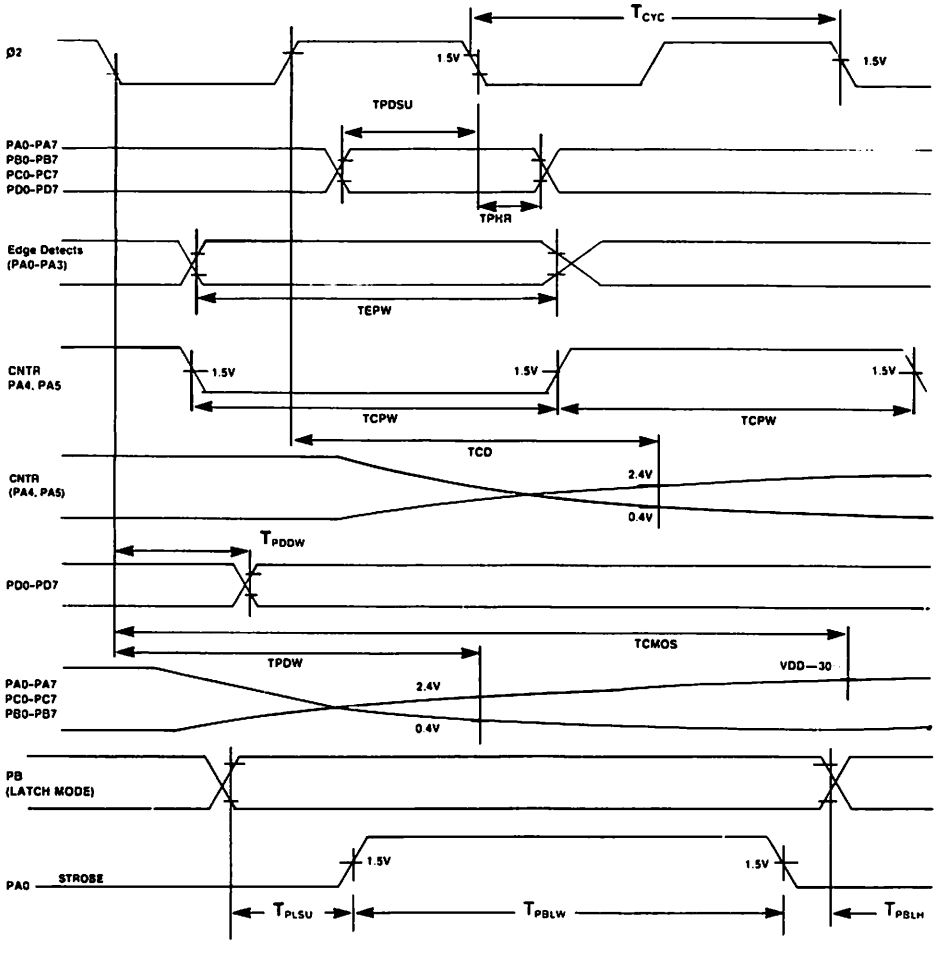


E.3 I/O, EDGE DETECT, COUNTERS, AND SERIAL I/O TIMING

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
	Internal Write to Peripheral Data Valid				
T_{PDW}[1]	PA, PB, PC TTL	—	500	—	500
T_{CMOS}[1]	PA, PB, PC CMOS	—	1000	—	1000
T_{PDDW}	PD	—	175	—	150
	Peripheral Data Setup Time				
T_{PDSU}	PA, PB, PC	200	—	200	—
T_{PDSU}	PD	50	—	50	—
	Peripheral Data Hold Time				
T_{PHR}	PA, PB, PC	75	—	75	—
T_{PHR}	PD	10	—	10	—
T_{EPW}	PA0-PA3 Edge Detect Pulse Width	T_{CYC}	—	T_{CYC}	—
	Counters A and B				
T_{CPW}	PA4, PA5 Input Pulse Width	T_{CYC}	—	T_{CYC}	—
T_{CD}[1]	PA4, PA5 Output Delay	—	500	—	500
	Port B Latch Mode				
T_{PBLW}	PA0 Strobe Pulse Width	T_{CYC}	—	T_{CYC}	—
T_{PLSU}	PB Data Setup Time	175	—	150	—
T_{PBLH}	PB Data Hold Time	30	—	30	—
	Serial I/O				
T_{PDW}[1]	PA6 XMTR TTL	—	500	—	500
T_{CMOS}[1]	PA6 XMTR CMOS	—	1000	—	1000
T_{CPW}	PA4 RCVR S/R Clock Width	4 T_{CYC}	—	4 T_{CYC}	—
T_{PDW}[1]	PA4 XMTR Clock—S/R Mode (TTL)	—	500	—	500
T_{CMOS}[1]	PA4 XMTR Clock—S/R Mode (CMOS)	—	1000	—	1000

NOTE 1: Maximum Load Capacitance: 50pF
Passive Pull-Up Required

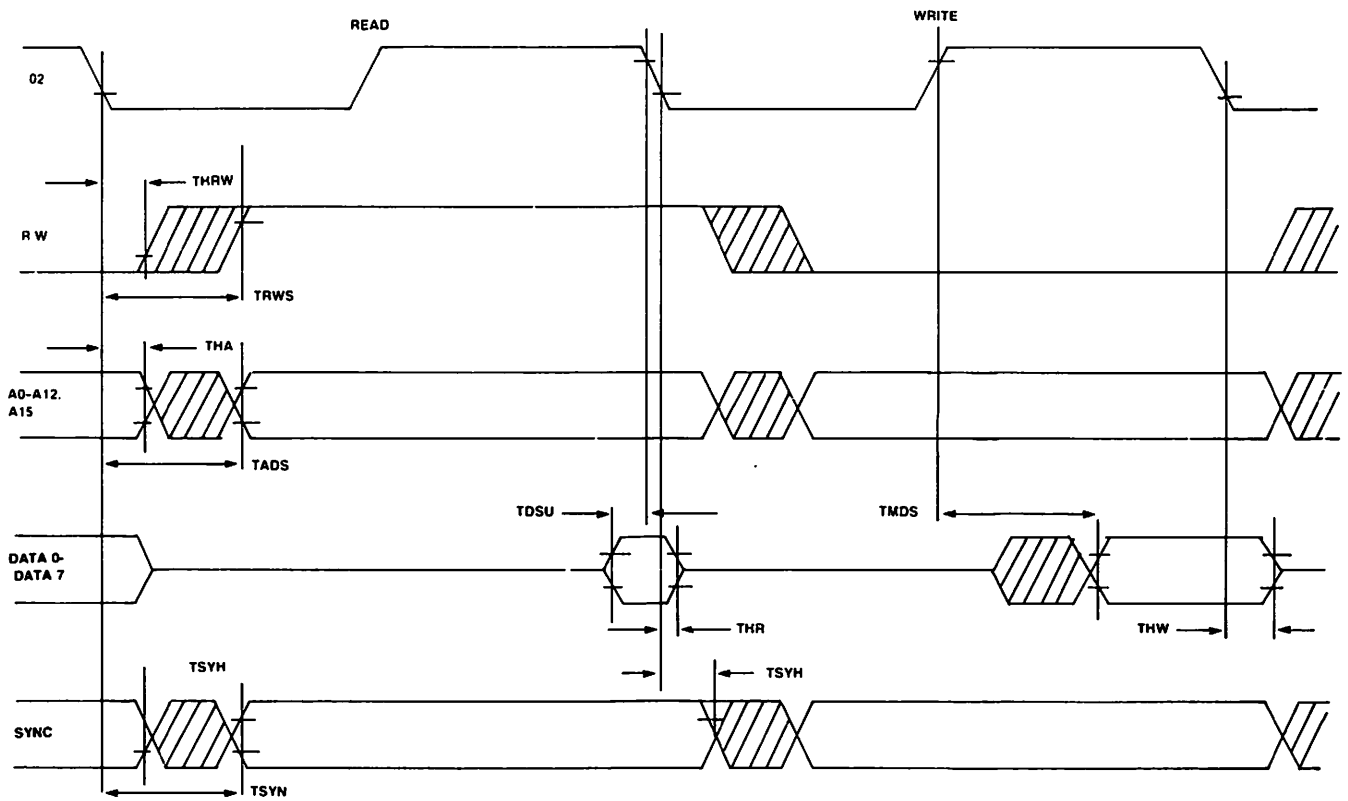
E.3.1 I/O, Edge Detect, Counter, and Serial I/O Timing



E.4 MICROPROCESSOR TIMING (D0–D7, A0–A12, A15, SYNC, R/W)

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{RWS}	R/W Setup Time	—	225	—	140
T_{ADS}	A0-A12, A15 Setup Time	—	150	—	75
T_{DSU}	D0-D7 Data Setup Time	50	—	35	—
T_{HR}	D0-D7 Read Hold Time	10	—	10	—
T_{HW}	D0-D7 Write Hold Time	30	—	30	—
T_{MDS}	D0-D7 Write Output Delay	—	175	—	130
T_{SYN}	SYNC Setup	—	225	—	175
T_{HA}	A0-A12, A15 Hold Time	30	—	30	—
T_{HRW}	R/W Hold Time	30	—	30	—
T_{ACC}	External Memory Access Time $T_{ACC} = T_{CYC} - T_F - T_{ADS} - T_{DSU}$	—	T_{ACC}	—	T_{ACC}
T_{SYH}	SYNC Hold Time	30	—	30	—

E.4.1 Microprocessor Timing Diagram



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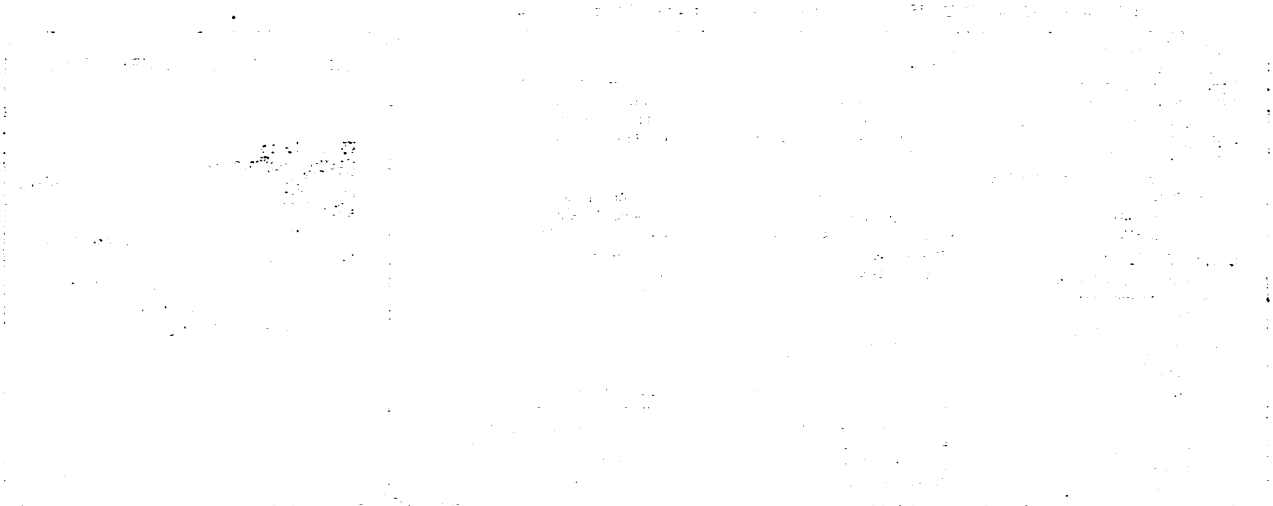

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