DATASHEET **BEMBUS COMPATIBLE**

B.E.M B.E.M - SBC4D(2)

6809 based "HIPER" boards with RTC, Battery backup, VIA, Serial I/O port(s), Watchdog timer and Page mode option

GENERAL DESCRIPTION

The B.E.M-SBC4D series of 6809 based, BEMBUS compatible, single board computers are high performance ("HIPER" series) boards, standard provided with Real Time Clock, battery backup for (CMOS) RAM and RTC, parallel I/O (VIA), serial I/O port(s) and watchdog timer circuit. The boards can optionally be delivered with a Hitachi 6309 CMOS CPU.

The basic SBC4D board is provided with a 2651 USART for synchronous as well as asynchronous serial I/O applications. The 2651, available only in NMOS, is implemented to maintain compatibility with previous designs (e.g. SBC4C). Optionally, the SBC4D can also be delivered with a 65C51 ACIA, enabling an all CMOS design. The SBC4D requires an adapter to convert the TTL signal levels to RS-232C or other interface levels. Many adapters (e.g. B.E.M-AD3, -AD6, -AD7, -AD8, -AD9) are suitable for this purpose.

The SBC4D2 is standard provided with two 65C51 ACIA's together with on-board RS-232C drivers and receivers for asynchronous serial I/O communications. Only TxD, RxD, RTS and CTS are supported on these ports, generally sufficient for most applications.

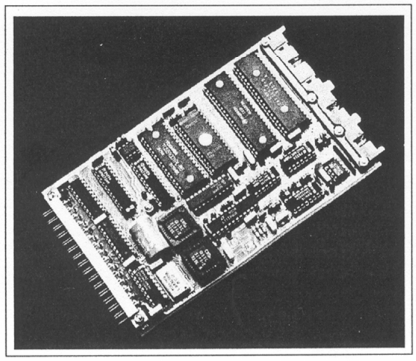
Both boards can be delivered with an optional page mode controller. With this controller, the on-board (CMOS) RAM capacity can be expanded to 512 kbyte max. in pages of 16 kbyte. With a special map configuration 32 kbyte pages are also possible.

The GAL decoder allows almost any user map configuration within the limits of the 64 kbyte addressing range of the processor. Both boards will standard be delivered with a general purpose decoder enabling the selection of two useful map configurations. User map configurations can be delivered on request at additional cost.

"continued on page 2"

FEATURES

- ☐ BEMBUS COMPATIBLE, 6809 BASED, SINGLE BOARD COMPUTER, STANDARD DELIVERED IN 2MHz VERSION. OPTIONALLY AVAILABLE WITH HITACHI 6309 CMOS CPU
- ☐ REAL TIME CLOCK AND (CMOS) RAM WITH LITHIUM BACKUP BATTERY (BACKUP CAPACITY OVER 10 YEARS)
- ☐ ONE VIA (65C22) FOR PARALLEL I/O WITH 16 PARALLEL I/O LINES, 4 HANDSHAKE LINES, A SHIFT REGISTER (8-BIT) AND 2 INTERVAL TIMERS/COUNTERS (16-BIT)
- ☐ SBC4D PROVIDED WITH ONE USART (2651) OR ACIA (65C51) TO BE USED WITH EXTERNAL ADAPTER. SBC4D2 PROVIDED WITH TWO ACIA's WITH ON-BOARD RS-232C INTERFACE CIRCUIT (SUPPORTING TxD, RxD, RTS AND CTS)
- ☐ SERIAL PORT(S) OFFER, AMONG OTHER FEATURES, PARITY CONTROL, VARIABLE WORD LENGTH, ONE OR TWO STOP BITS AND BAUD RATE SELECTION (15 BAUD RATES FROM 50 UP TO 19200 BAUD ARE SELECTABLE)
- ☐ WATCHDOG TIMER CIRCUIT WITH SEVERAL RETRIGGER SOURCE, MODE (AC/DC) AND DELAY TIME SETTINGS
- ☐ REAL TIME CLOCK (8573A) WITH CALENDAR, YEAR REGISTER, SEVERAL ALARM FUNCTIONS AND AUTOMATIC LOG OF TIME INTO RAM AT POWER FAILURE
- ☐ GAL DECODER ALLOWS PRACTICALLY ANY RAM/EPROM COMBINATION WITHIN THE 64 KBYTE ADDRESSING RANGE
- ☐ PAGE MODE OPTION ALLOWS ON-BOARD RAM EXPANSION UP TO 512 KBYTE IN PAGES OF 16 KBYTE
- ☐ ALSO SUITABLE FOR STAND-ALONE APPLICATIONS
- ☐ SINGLE 5V POWER SUPPLY REQUIRED
- ☐ CUSTOMIZED VERSIONS WITHIN THE LIMITS OF THE DESIGN ARE POSSIBLE
- ☐ HIGH QUALITY MACHINE TOOLED SOCKETS FOR DIL DEVICES, SPECIAL SOCKETS FOR PLCC DEVICES
- ☐ GENEROUS OEM DISCOUNTS AVAILABLE



BEMBUS CONNECTIONS

Pin	Function
1	N.C. (1)
2	VSS (GND)
3	D7
4	D6
5	D5
6	D4
7	D3
8	D2
9	D1
10	D0

Pin	Function
11	Q (2)
12	R/WN
13	E
14	A15
15	A14
16	A13
17	A12
18	A11
19	A10
20	A9

Pin	Function
21	A8
22	A7
23	A6
24	A5
25	A4
26	A3
27	A2
28	A1
29	A0
30	VCC (+5V)
31	N.C. (3)

NOTES: (1) Not connected but reserved for VEE (-12V). (2) Not connected but reserved for Q clock via J12. (3) Not connected but reserved for VDD (+12V)

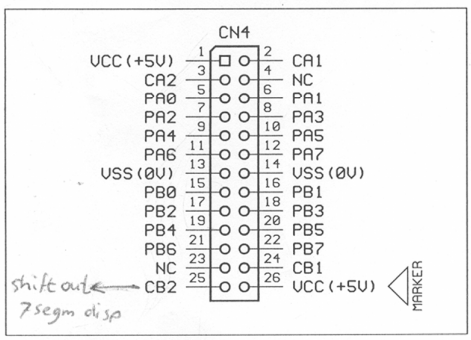
"continued from page 1"

CPU and USART / ACIA('s) are provided with independent crystal clocks. The RTC has its own precision tuning fork crystal with calibration circuit.

Basic properties of the on-board (local) devices are summarized below:

1) VIA The 65C22 VIA (Versatile Interface Adapter) provides two 8-bit bi-directional ports, each with 2 programmable control lines for handshake or other purposes. Each I/O line can individually be programmed to be used either as an input or an output. Moreover, two 16-bit programmable interval timers/counters and one 8-bit shift register are available to the user. The VIA can be used in many different modes. Connections are made via a 26-pin flat cable header with a pin lay-out equal to those on other BEM application cards (provided with VIA's or PIA's) and compatible series of parallel I/O adapters (see connection table below). See also page 9 for location of the VIA in the standard map configurations.

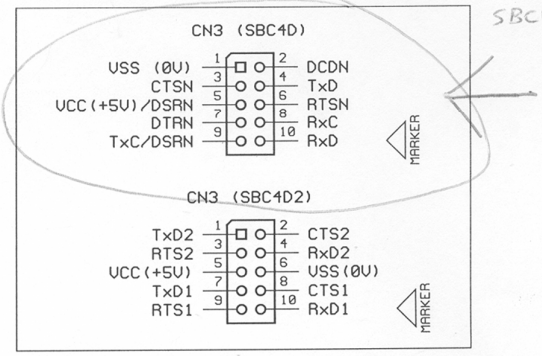
PARALLEL I/O HEADER CONNECTIONS



2) USART & ACIA('s) One 2651 USART (Universal Synchronous Asynchronous Receiver Transmitter) is standard delivered on the SBC4D. However, the board design allows optional installation of a 65C51 (CMOS) ACIA (Asynchronous Communication Interface Adapter). The USART, only obtainable in NMOS, is implemented to maintain compatibility with previous designs (e.g. SBC4C). The USART and ACIA are sophisticated communication devices, of which all parameters can be programmed (baud rate, parity, word length, number of stop bits etc). Applications range from simple terminal/peripheral control to complex synchronous multi-user networks (USART only). 15 Different baud rates from 50 up to 19200 baud can be selected. The USART even allows baud rates from DC up to 1 megabaud in the synchronous mode. The serial port connections on the SBC4D are made via a 10-pin flat cable header with a pin lay-out equal to those on other BEM application cards (provided with USART's or ACIA's) and compatible series of serial I/O adapters (see connection table in the column to the right). In standard version pin 5 is strapped to VCC and pin 9 to DSRN. If necessary, the functions of pin 5 and 9 can be changed (see jumper section on page 11 for more details).

The SBC4D2 is standard provided with two ACIA's together with on-board RS-232C interface circuitry, practically eliminating the need for external adapters. For simplicity reasons only RxD, TxD, RTS and CTS are supported on these ports. Both ports are routed to a single 10-pin flat cable header together with the VCC (+5V) and VSS (0V) power connections. Header connections are listed below. **NOTE:** A simple passive adapter is available (B.E.M-AD15M) to convert the single flat cable connection to two 9-pin subminiature D connectors (male). See page 11 for details on memory map and register locations.

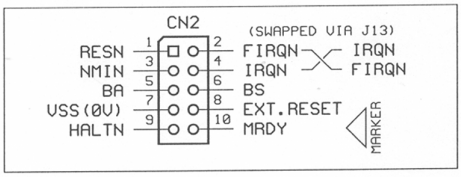
SERIAL I/O HEADER CONNECTIONS



3) BEMBUS The BEMBUS main interface section contains all address, data and basic control lines (R/WN, E and Q clock) minimally required to control most of the available BEMBUS compatible applications cards. All bus interface signals are buffered enabling expansion up to twenty bus cards. For more advanced applications, e.g. requiring external interrupt handling, the BEMBUS extension (see next paragraph) must be used in addition. Details on external map considerations can be found on page 9. BEMBUS connections are made via a 31 pin (DIN 41617) connector, standardized within the BEMBUS concept. The pin description table is printed on page 1.

4) BUS EXTENSION The bus extension header connections (see table below) are used to control more complex BEMBUS cards, in particular those cards requiring interrupt handling. For detailed description of the CPU and the specific control functions available via the bus extension header see the manual or datasheet of the original or second source manufacturer. CPU status is indicated by the BA (Bus Available) and BS (Bus Status) lines, listed to the right.

BUS EXTENSION HEADER CONNECTIONS



CPU State		Description
BA	BS	
0	0	Normal (Running)
0	1	Interrupt Acknowledge
1	0	Sync Acknowledge
1	1	HALT

5) RTC All "HIPER" boards are provided with the DP8573A Real Time Clock from National Semiconductor. Backup power is so low that RAM and RTC can share the same Lithium backup battery (backup capacity over 10 years). From the programmers point of view the clock behaves like a block of memory (32 bytes) in the map (see page 9 for more details). The clock not only offers 12/24

hour mode time keeping but also a day of week counter and a calendar with year register. Other important features are automatic log of time into RAM at power failure and several alarm functions. See also pages 9 and 10 for more details.

6) POR & WATCHDOG The Power On Reset circuit is controlled by a 7705 device, generating a reset signal for CPU, VIA and USART / ACIA('s) at power up and power down conditions. The circuit keeps or turns RESN low (RES high) as long as or as soon as the power supply voltage deviates more than 5% from the ideal value of 5V. The circuit reacts fast. In particular, transients and noise on the +5V power supply line must be avoided to prevent incidental resetting during operation. RESN is also routed to the bus extension header to reset other bus cards or to allow resetting from an external source (RESN is an open collector line). The header also allows the connection of an external reset switch (between pin 7 and 8) for manual reset control.

The watchdog timer consists of an RC oscillator, driving a resettable 14 stage binary counter. One of the three final counter outputs can be selected to activate the reset line, enabling the user to select one of three practical delay times, respectively 1x, 2x or 4x the timebase (approximately 1.25 sec.). The timebase can be changed, if necessary, by selecting different RC component values. If selected active, the programmer must take care to clear the timer within the selected delay time in order to prevent the system to be reset. On the SBC4D the user may select the CA2 or CB2 output of the VIA or the TxD output of the USART / ACIA as a possible source to clear the counter . On the SBC4D2, in addition, also the TxD of the second ACIA may be selected (TxD2).

Besides the source, the user may select the coupling mode to the source. In the AC mode, the counter will be cleared at a low to high transition. In the DC mode the counter is cleared at a high level. **NOTE:** In the DC mode the watchdog timer can be fixed in the cleared state, which can be useful if there is no time to service the watchdog timer at some moment during program execution. However, the danger exists, that an error can also clear the watchdog timer continuously. This will never happen in the AC mode. The AC mode will also be the only practical mode to select if TxD is used as a source.

7) MEMORY & BATTERY BACKUP All cards are provided with a 28-pin socket for EPROM/ROM and a 32-pin socket for RAM. EPROM's up to 64 kbyte and RAM's up to 512 kbyte (with page mode controller option) can be applied. Without page mode controller, RAM devices from 8 kbyte up to 128 kbyte can be used. Although, a high capacity RAM can be installed in this standard mode, the limited direct addressing range will practically allow access to less than 64 kbyte of RAM. The memory map configuration is determined by a GAL decoder. This decoder guarantees high flexibility in selecting custom map configurations. In standard version the user can select from two basic configurations, see page 9 for more details.

A special backup controller (Dallas DS1210) is used to control the (CMOS) RAM. The backup threshold can be selected to be within 5% or 10% tolerance from the ideal value of VCC = +5V. The RAM can only be accessed when VCC remains within the tolerance limits. When out of limits, the RAM is deselected. As soon as VCC drops below VB+ (approximately 3.5V) backup takes over. The Lithium battery used on these cards has a capacity of 850 mAh, sufficient for more than 10 years of backup performance under normal operating conditions. **NOTE:** When the battery is connected for the first time or via jumper J1 from off to on, backup will only be provided after VCC has been within the tolerance limits. If the battery voltage is less than 2.0V (or switched off), the second RAM select is inhibited. With appropriate software, this can be used to check the battery status.

The Lithium battery is also used to backup the Real Time Clock. A Led is installed in series with the backup line to reduce the backup voltage for the clock in order to decrease the current drain (the lower the voltage, the lower the backup current).

8) PAGE MODE CONTROLLER The Page Mode Controller, available as an option on both cards, will allow RAM expansion beyond the 64 kbyte basic limits. Up to 512 kbyte can be installed in a single device. In the standard configuration 16 kbyte RAM is fixed in the lower part of the map ($0000 to $3FFF) followed by a16 kbyte page ($4000 to $7FFF). Pages are swapped in this area. The active page is simply selected by writing the page address register located in the I/O field with the page number (see page 10 for more details). The highest usable page address depends on the page size and the RAM capacity. For instance with a 128 kbyte RAM device and 16 kbyte pages, only 7 pages are available (0 to 6). User software must take care that no higher page addresses are selected than available in the RAM to avoid overwriting the fixed part . In customized versions pages of 32 kbyte and/or different swap area addresses (selectable in steps of 16k) are also possible. Please contact factory or nearest distributor for more details and cost on customized memory map and special page mode controller configurations.

9) POWER SUPPLY REQUIREMENTS Only a single 5V (± 5%) power supply voltage is required for the SBC4D and SBC4D2 . Typical current requirement is 245 mA for a SBC4D with USART, 200 mA for a SBC4D with ACIA and 205 mA for a SBC4D2 with both ACIA's installed. Lower current values (down to 40 %) are possible with quarter power GAL's and a 63B09 CMOS CPU (Hitachi) installed. Power supply connections are preferably made via the BEMBUS connector (pin 2 = 0V, pin 30 = +5V).

10) GENERAL The boards are provided with high quality machine tooled sockets for DIL devices. Special sockets are installed for PLCC's (ACIA's). In OEM quantities, the SBC4D(2) series can be delivered in any stripped configuration within the technical limits of the design.

ABSOLUTE MAXIMUM RATINGS

Ambient temperature under bias	0°C to +70°C
Storage temperature	-55°C to +85°C
Voltage on any pin (RS-232C I/O lines excepted) with respect to ground	-0.3V to +7V
Voltage on RS-232C input pins in respect to ground	±30V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the B.E.M - SBC4D(2) cards. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

DC CHARACTERISTICS

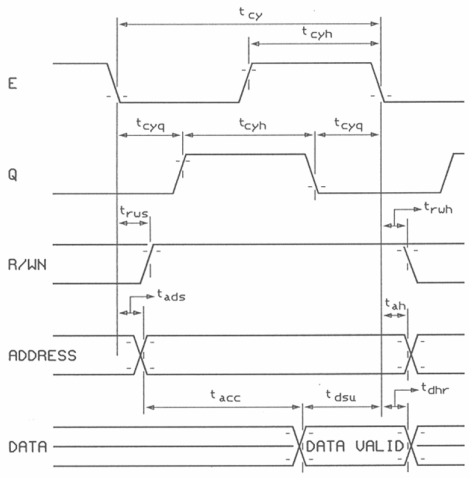
TA = 0°C to +70°C, VCC = +5V, ±5% (unless otherwise specified)

	Symbol	Parameter	Limits Min.	Typ.	Max.	Unit	Test conditions
BEMBUS & POWER SPECIFICATIONS	I_{CC1}	VCC Power supply current SBC4D in standard version with 32 kbyte CMOS RAM, without EPROM and Page Mode Controller (PMC)		245 200	400 365	mA mA	VCC = 5.25 V (with 2651 USART). VCC = 5.25 (with 65C51 ACIA). (Add 65 mA to typical value with PMC)
	ICC2	VCC Power supply current SBC4D2 in standard version with 32 kbyte CMOS RAM, without EPROM and Page Mode Controller (PMC)		205	345	mA	VCC = 5.25 V (with two 65C51 ACIA's). (Add 65 mA to typical value with PMC)
	CBB	Battery back-up capacity	750	850		mAh	I_{BB} =< 20 µA.
	ILIH	Input load current on any bus input pin "high level"			20 100	µA µA	VIN = 2.7 V. VIN = 7.0 V.
	ILIL	Input load current on any bus input pin "low level"			400	µA	VIN = 0.4 V
	ILD	Leakage current data bus pins "off state"			20	µA	VIN = 2.7 V.
	VIL	Input low voltage (any bus input pin)	-0.5		0.8	V	
	VIH	Input high voltage (any bus input pin)	2.0		VCC	V	
	VOL	Output low voltage (any bus output pin)			0.5	V	IOL = 24 mA.
	VOH	Output high voltage (any bus output pin)	2.0			V	IOH = -15 mA.
BUS EXT.	V_{IHT}	Input high threshold voltage IRQN, FIRQN NMIN, MRDY	2.0		VCC	V	All bus extension input lines are terminated with on-board pull-up resistors of 3k3.
	VIHTR	Input high threshold voltage RESN only	4.0		VCC	V	
	VILT	Input Low threshold voltage RESN, IRQN, FIRQN NMIN, MRDY	-0.3		0.8	V	
	VOL1	Output low voltage RESN			0.5	V	I_{OL1} = 8 mA.
	VOL2	Output low voltage BA, BS, HALTN			0.4	V	I_{OL2} = 4 mA.
	V_{OH2}	Output high voltage BA, BS	2.4			V	I_{OH2} = -400 µA.
	V_{IL1}	Input low voltage HALTN	0.5		0.8	V	
	V_{IH1}	Input high voltage HALTN	2.0		VCC	V	
PARALLEL I / O (VIA)	V_{IHV}	Input voltage high level	2.0		VCC +0.3	V	
	VILV	Input voltage low level	-0.3		0.8	V	
	IINV	Input leakage current CA1			±2.5	nA	V_{IN} = 0 to +5 V.
	IIHV	Input high current PA0 → PA7, CA2, PB0 → PB7, CB1 and CB2	-200			µA	VIN = 2.4 V (internal pull-up resistors).
	IILV	Input low current PA0 → PA7, CA2, PB0 → PB7, CB1 and CB2			2.4	mA	VIN = 0.4 V.
	VOHV	Output high voltage PA0 → PA7, CA2, PB0 → PB7, CB1 and CB2	2.4			V	IL = -200 µA.
	VOLV	Output low voltage PA0 → PA7, CA2, PB0 → PB7, CB1 and CB2			0.4	V	IL = 3.2 mA.
	IOHV	Output high current (sourcing)	-200 -3.0		-10.0	µA mA	VOH = 2.4 V. VOH = 1.5 V (PB0 → PB7 only).
	IOLV	Output low current (sinking)	3.2			mA	VOL = 0.4 V.
SERIAL I / O	V_{ILU}	Input low voltage any input pin	-0.3		0.8	V	
	VIHU	Input high voltage any input pin	2.0		VCC	V	
	VOLU	Output low voltage any output pin			0.4	V	I_L = 3.2 mA. **ACIA / USART**
	VOHU	Output high voltage any output pin	2.4			V	I_L = -200 µA. **(SBC4D)**
	IOLU	Output low current (sinking)	3.2			mA	V_{OL} = 0.4 V.
	IOHU	Output high current (sourcing)	-200			µA	V_{OH} = 2.4 V.
	V_{RIM}	RS-232C input voltage			±30	V	Absolute maximum value.
	VRIL	RS-232C input low threshold level	+0.2	+1.3		V	
	VRIH	RS-232C input high threshold level	+1.7	+3.0		V	**RS - 232C**
	VROL	RS-232C output voltage high level	+5.0	+7.3		V	With 3 kOhm load. **(SBC4D2)**
	VROH	RS-232C output voltage low level	-5.0	-6.5		V	With 3 kOhm load.

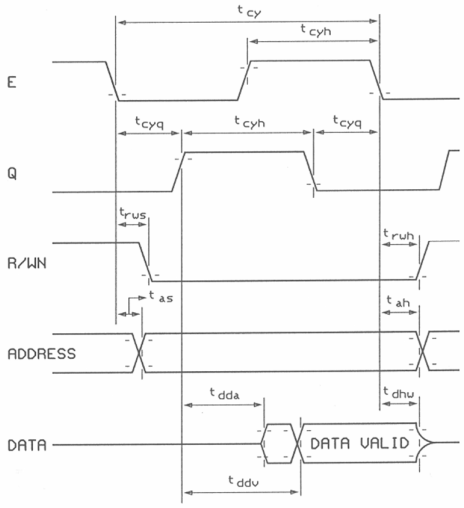
BEMBUS READ & WRITE TIMING

Symbol	Parameter	Limits 2MHz bus clock (8MHz CPU crystal)			Unit	Test conditions
		Min.	Typ.	Max.		
t_{cy}	Total read cycle time E clock		500		nsec	Crystal based clock
tcyh	Clock cycle high time (E, Q)		250		nsec	
tcyq	Clock quarter cycle time (basic clock cycle)		125		nsec	
t_{ads}	Address set-up time			110	nsec	VCC = +5.0V, TA = 0°C to +70°C
tah	Address hold time	30			nsec	
tdhw	Data hold time (write cycle)	30			nsec	
tdsu	Data set-up time (read cycle)	60			nsec	
tdhr	Data hold time (read cycle)	0			nsec	
trws	R/WN set-up time			110	nsec	
trwh	R/WN hold time	30			nsec	
tdda	Delay time Q high to data bus active			35	nsec	Timing figures and diagrams are for bus signals only.
tddv	Delay time Q high to data out valid			125	nsec	
tacc	Memory read access time			300	nsec	

READ CYCLE TIMING



WRITE CYCLE TIMING



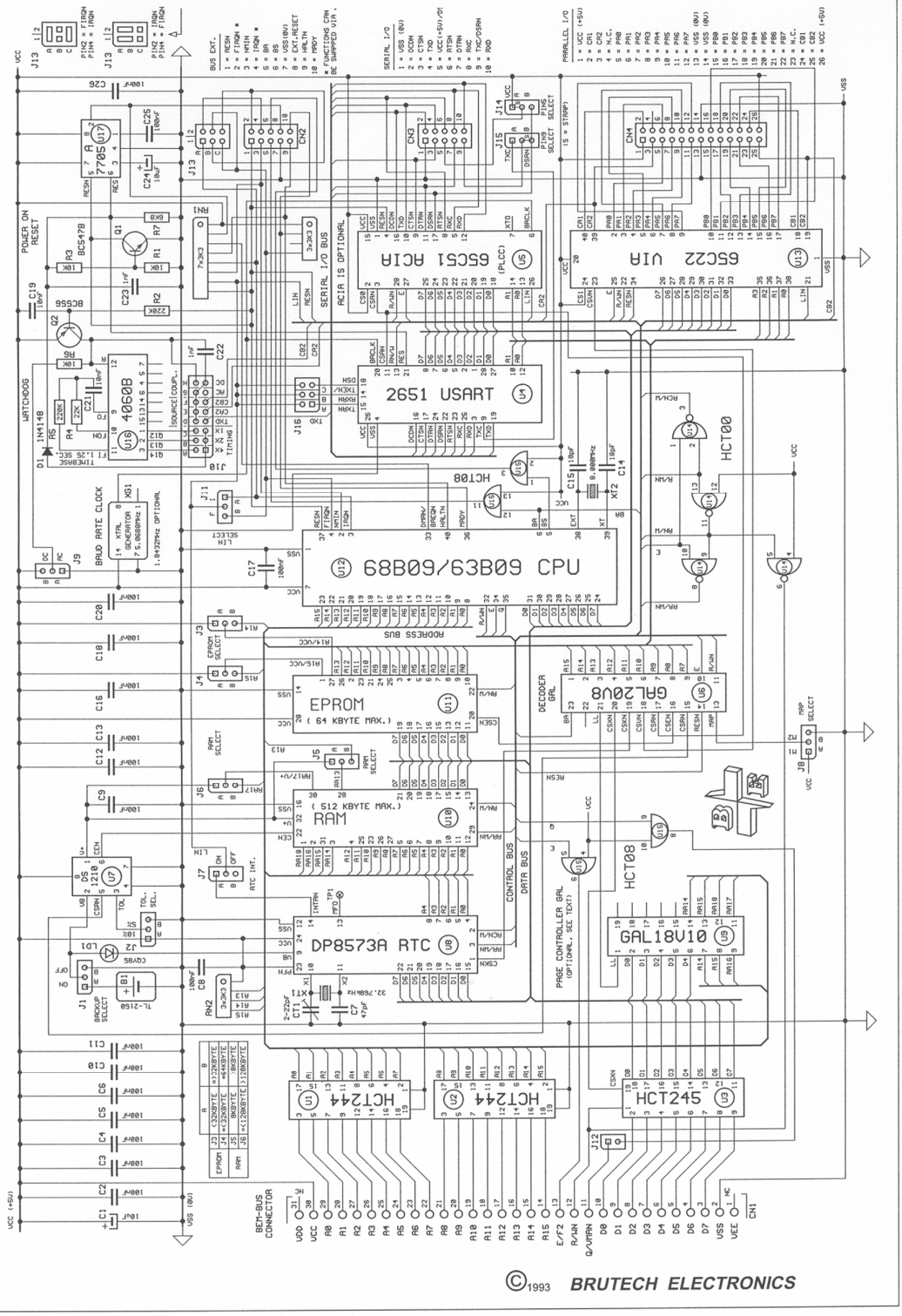
NOTES

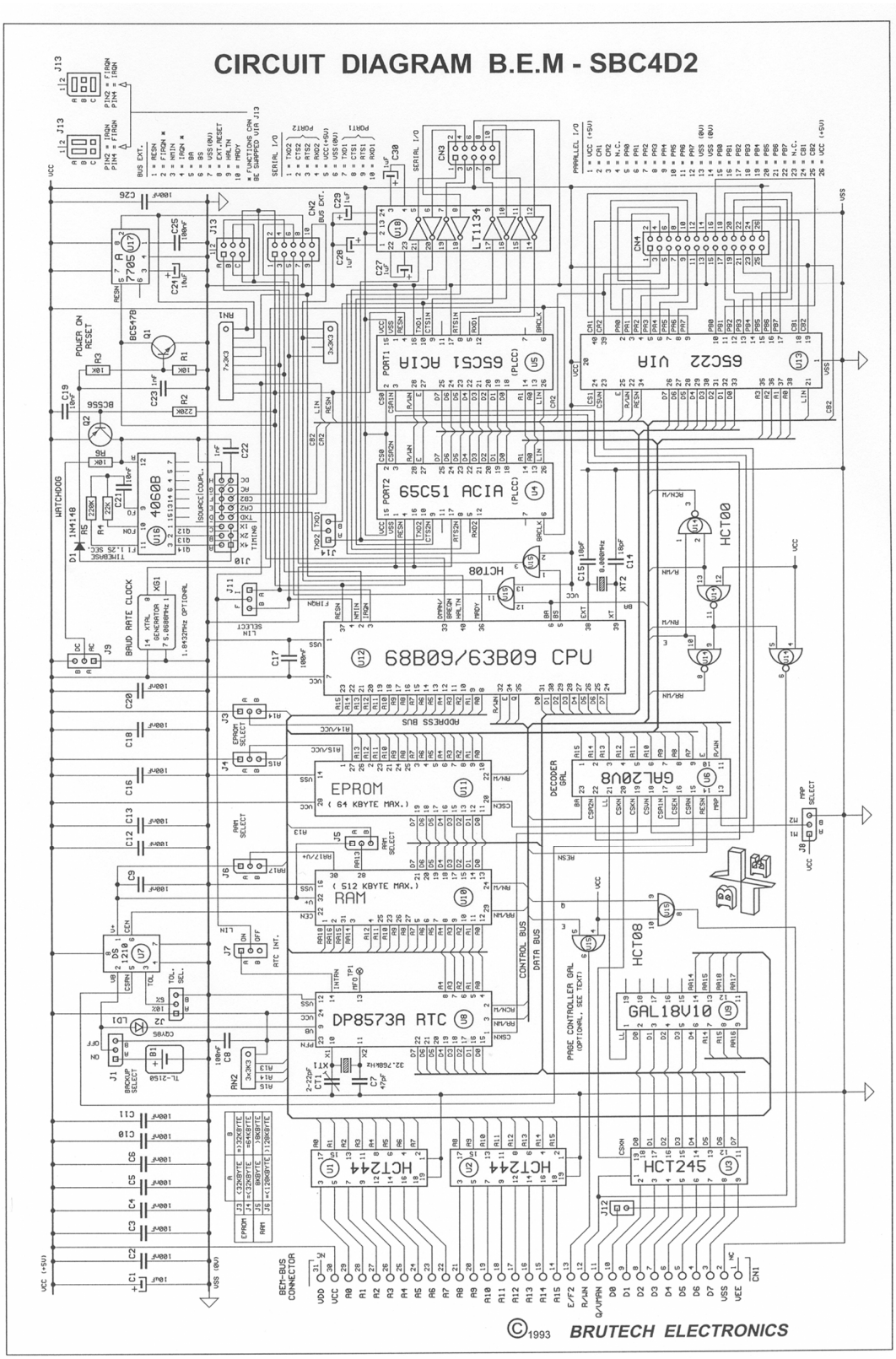
1 For detailed description of CPU, VIA, USART, ACIA and RTC, the data sheets and manuals of the original or second source manufacturer(s) are recommended. For example: Rockwell, UMC and GTE for the 65C22 and 65C51. Motorola, Thomson and Hitachi for the 6809 CPU (Hitachi only for the 6309). UMC, Philips and National Semiconductor for the 2651 USART and National Semiconductor for the 8573A RTC.

2 In this datasheet the notation to add a N to the name of low active signals is used instead of overscoring the name (e.g. RESN = $\overline{R}$).

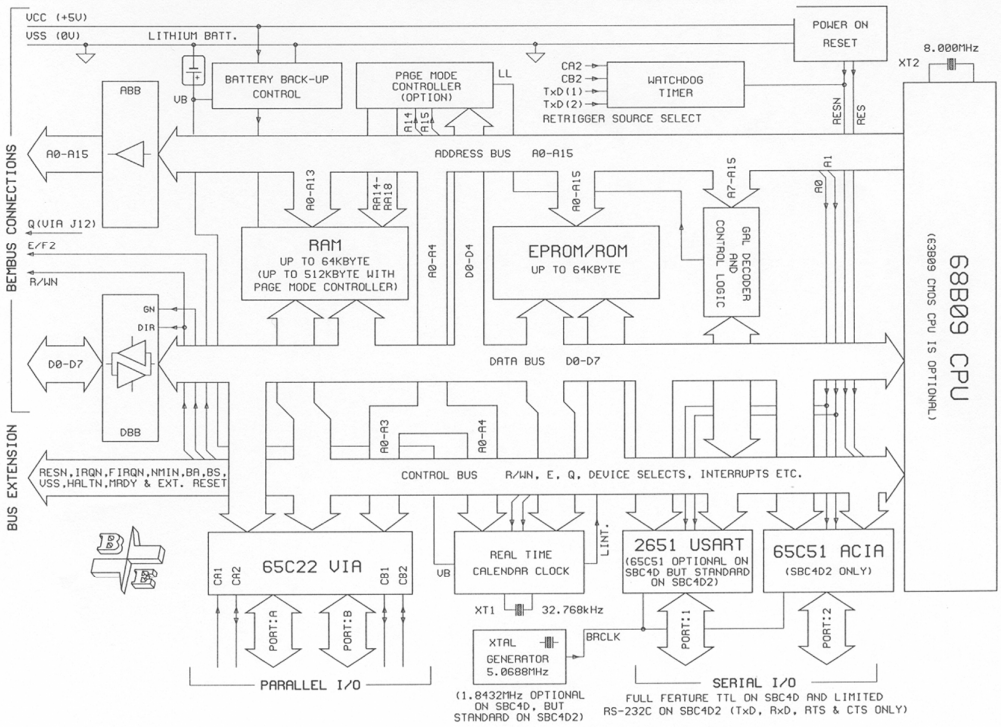
3 If a 28 pin RAM (32 kbyte max.) is used in the 32 pin socket, be sure to place the device with pin 1 in the pin 3 position of the socket.

CIRCUIT DIAGRAM B.E.M - SBC4D

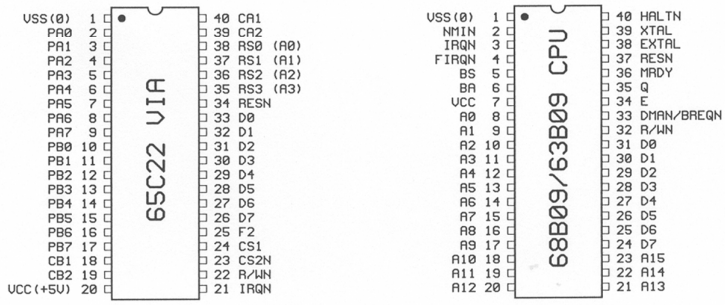



CIRCUIT DIAGRAM B.E.M - SBC4D2
68B09/63B09 CPU
EPROM
(64 KBYTE MAX.)
RAM
(512 KBYTE MAX.)
65C51 ACIA
65C22 VIA
DP8573A RTC
HCT00
HCT08
HCT32
HCT244
HCT245
GAL20V8
GAL18V10
PAGE CONTROLLER GAL
(OPTIONAL, SEE TEXT)
DECODER GAL
ADDRESS BUS
CONTROL BUS
DATA BUS
BRUTECH ELECTRONICS

BLOCK DIAGRAM B.E.M - SBC4D(2)



PIN LAY - OUT CPU, VIA, USART & ACIA

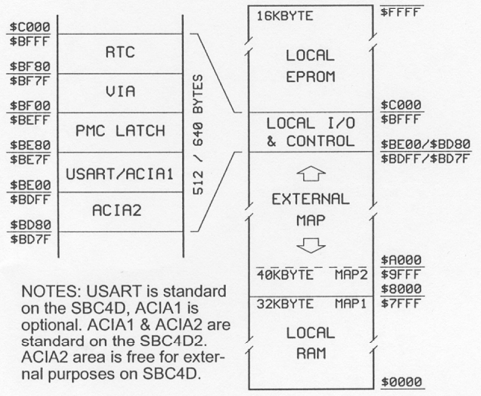


MEMORY MAP & REGISTER ADDRESSES

The drawing below shows the basic memory map configurations as been delivered with the standard SBC4D and SBC4D2 boards. One of two map configurations can be selected, differing only in the local RAM capacity (32 kbyte respectively 40 kbyte). The higher RAM capacity will reduce the address range available for external purposes.

The map area reserved for the local I/O and control

MEMORY MAP B.E.M - SBC4D / SBC4D2



NOTES: USART is standard on the SBC4D, ACIA1 is optional. ACIA1 & ACIA2 are standard on the SBC4D2. ACIA2 area is free for external purposes on SBC4D.

field is slightly different for both boards. The second ACIA, available only on the SBC4D2, is directly mapped below ACIA1. This particular area is free for external purposes on the SBC4D. For simplicity reasons all devices occupy 128 bytes in the map. As most devices require less space they can be accessed at several echo locations within the reserved address area. In this document only the lowest significant addresses are mentioned without further notice.

User map configurations are possible within the limits of the design. Please contact factory or nearest representative for details and cost. The several on-board I/O and control devices with their map implications will briefly be described below. Detailed description of IC's used on the boards is beyond the purpose of this datasheet, but can be found in the manuals and datasheets of the original or second source manufacturers.

RTC The Real Time Clock located in the map area from $BF80 up to $BFFF is controlled via 32 registers located from $BF80 up to $BF9F (relative addresses from $00 to $1F). Moreover, the RS bit (D6) of the main status register at $00 determines the functions of the four next registers ($01 to $04). The drawing in the next column shows the basic map and register locations of the RTC.

The clock has 8 bytes of counters which count from 1/100 of a second up to years. Each counter counts in BCD and is synchronously clocked. Upon initial application of power the counters will contain random data. The control and status register bit functions are summarized in the tables in the column to the right and on the next page.

VIA The VIA, located in the map area from $BF00 up to $BF7F, is controlled via 16 registers basically accessed from $BF00 to $BF0F (relative addresses from $0 to $F).

1F	RAM / TEST Register	
1E	RAM	
1D	Months Time Save RAM	
1C	Day of Month Time Save RAM	
1B	Hours Time Save RAM	
1A	Minutes Time Save RAM	
19	Seconds Time Save RAM	
18	Day of Week Compare RAM	(1 - 7)
17	Months Compare RAM	(1 - 12)
16	Day of Month Compare RAM	(1 - 28/29/30/31)
15	Hours Compare RAM	(1 - 12, 0 - 23)
14	Minutes Compare RAM	(0 - 59)
13	Seconds Compare RAM	(0 - 59)
12	N / A	
11	N / A	
10	N / A	
0F	N / A	
0E	Day of Week Clock Counter	(1 - 7)
0D	D0 and D1 Bits Only	
0C	RAM	
0B	Years Clock Counter	(0 - 99)
0A	Months Clock Counter	(1 - 12)
09	Day of Month Clock Counter	(1 - 28/29/30/31)
08	Hours Clock Counter	(1 - 12, 0 - 23)
07	Minutes Clock Counter	(0 - 59)
06	Seconds Clock Counter	(0 - 59)
05	1/00 Second Counter	(0 - 99)

	Main Status Register D6=0	Main Status Register D6=1
04	Time Save Control Register	Interrupt Control Register 1
03	Periodic Flag Register	Interrupt Control Register 0
02	N / A	Output Mode Register
01	N / A	Real Time Mode Register
00	Main Status Register	

MAIN STATUS REGISTER $00

Bit	Name	Function	
D0	INT	Interrupt Status	(1)
D1	PF	Power Fail Interrupt	(2)
D2	PER	Periodic Interrupt	(3)
D3	AL	Alarm Interrupt	(3)
D4	R	General Purpose RAM	
D5	R	General Purpose RAM	
D6	RS	Register Select Bit ($01 - $04)	
D7	R	General Purpose RAM	

NOTES: (1) - Reset when all pending interrupts are removed. (2) - PF bit not applicable on SBC4D(2) boards. (3) - Reset by writing a 1 to this bit

PERIODIC FLAG REGISTER $03 (RS = 0)

Bit	Name	Function	
D0	MF	Minutes Flag	(1)
D1	TSF	10 Seconds Flag	(1)
D2	SF	Seconds Flag	(1)
D3	HMSF	100 Milli-Seconds Flag	(1)
D4	TMSF	10 Milli-Seconds Flag	(1)
D5	MSF	Milli-Seconds Flag	(1)
D6	OSF	Oscillator Failed / Single Supply Bit	(2)
D7	TME	Test Mode Enable	

NOTES: (1) - Reset by read operation. (2) - Read 1, oscillator failure. Write 0 with battery backup installed, write 1 in single supply mode.

TIME SAVE CONTROL REGISTER $04 (RS = 0)

Bit	Name	Function
D0	R	General Purpose RAM
D1	R	General Purpose RAM
D2	R	General Purpose RAM
D3	R	General Purpose RAM
D4	R	General Purpose RAM
D5	R	General Purpose RAM
D6	NA	Not Applicable (reads zero)
D7	TSE	Time Save Enable Bit

REAL TIME MODE REGISTER $01 (RS = 1)

Bit	Name	Function
D0	LY0	Leap Year LSB (see table below)
D1	LY1	Leap Year MSB (see table below)
D2	H12	12 hour (high) / 24 hour (low) Mode
D3	CSS	Clock Start (high) / Stop (low)
D4	IPF	Interrupt Power Fail Operation
D5	R	General Purpose RAM
D6	R	General Purpose RAM
D7	R	General Purpose RAM

LY1	LY0	Leap Year Counter
0	0	Leap Year Current Year
0	1	Leap Year Last Year
1	0	Leap Year 2 Years Ago
1	1	Leap Year 3 Years Ago

OUTPUT MODE REGISTER $02 (RS = 1)

Bit	Name	Function
D0	R	General Purpose RAM
D1	R	General Purpose RAM
D2	R	General Purpose RAM
D3	R	General Purpose RAM
D4	R	General Purpose RAM
D5	R	General Purpose RAM
D6	R	General Purpose RAM
D7	MO	MFO (TP1). Low = Power Fail Interrupt, high = Buffered Oscillator Output

INTERRUPT CONTROL REGISTER - 0 $03 (RS = 1)

Bit	Name	Function
D0	MN	Minutes Enable Bit
D1	TS	10 Seconds Enable Bit
D2	S	Seconds Enable Bit
D3	HMS	100 Milli-Seconds Enable Bit
D4	TMS	10 Milli-Seconds Enable Bit
D5	MS	Milli-Seconds Enable Bit
D6	R	General Purpose RAM
D7	R	General Purpose RAM

INTERRUPT CONTROL REGISTER - 1 $04 (RS = 1)

Bit	Name	Function
D0	SC	Second Compare Enable Bit
D1	MN	Minute Compare Enable Bit
D2	HR	Hour Compare Enable Bit
D3	DOM	Day of Month Enable Bit
D4	MO	Month Compare Enable Bit
D5	DOW	Day of Week Enable Bit
D6	ALE	Alarm Interrupt Enable Bit
D7	PFE	Power Fail Interrupt Enable Bit

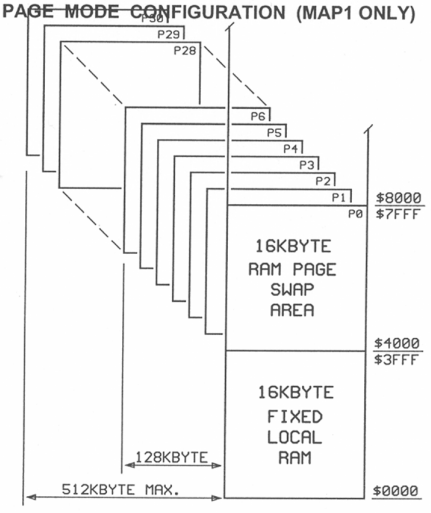
The table below shows the map and register locations of the VIA.

Addr.	Name	Function / Register	
		Write	Read
0	ORB/IRB	Output Register Port B	Input Register Port B
1	ORA/IRA	Output Register Port A	Input Register Port A
2	DDRB	Data Direction Register Port B	
3	DDRA	Data Direction Register Port A	
4	T1L/C - L	T1 Low-order Latch	T1 Low-order Counter
5	T1C - H	T1 High-order Counter	
6	T1L - L	T1 Low-order Latch	
7	T1L - H	T1 High-order Latch	
8	T2L/C - L	T2 Low-order Latch	T2 Low-order Counter
9	T2C - H	T2 High-order Counter	
A	SR	Shift Register	
B	ACR	Auxiliary Control Register	
C	PCR	Peripheral Control Register	
D	IFR	Interrupt Flag Register	
E	IER	Interrupt Enable Register	
F	ORA/IRA	Same as address 1, except no "handshake"	

PMC The Page Mode Controller is optional. The map area from $BE80 up to $BEFF is reserved for the page number register. Paging is controlled via this 5-bit latch that can be accessed (write only) at any location within the reserved area.

Independent of the RAM capacity applied, the lower 16 kbyte ($0000 up to $3FFF) is always fixed in the map. The next 16 kbyte field (page field), swapped in the area from $4000 up to $7FFF, is dependent on the value written in the page number register. Never write higher values in the latch than appropriate for the applied RAM (otherwise the lower 16 kbyte field may be overwritten with unpredictable results).

PAGE MODE CONFIGURATION (MAP1 ONLY)



Valid page address values are respectively 0 → 6, 0 → 14($E) and 0 → 30($1E) for respectively a 128 kbyte, 256 kbyte and 512 kbyte RAM. The drawing on the previous page shows the page mode configuration in detail. **NOTE:** If the PMC option is installed only map1 can be used.

USART & ACIA's The USART, standard delivered on the SBC4D, and ACIA(1), optional on the SBC4D but standard on the SBC4D2, are located in the map area from $BE00 up to $BE7F. ACIA2, standard only on the SBC4D2, is located from $BD80 up to $BDFF. Communication with each device goes via four registers respectively located from $BE00 to $BE03 and $BD80 to $BD83 (relative addresses 0 to 3). The tables below show the basic map and register functions for USART and ACIA.

NOTE: Each time a write is made to the SYN1/ SYN2

USART

Addr.	Name	Function / Register	
		Write	Read
0	TDR/RDR	Transmit Data Register	Receive Data Register
1	SSDR/SR	SYN1/SYN2/DLE Reg.	Status Register
2	MR	Mode Register 1/2	
3	CMR	Command Register	

/DLE address and a write or read is made to or from the Mode Register 1/2, an internal counter is incremented. The counters are wrapped around and are cleared by reading the command register or a reset.

ACIA

Addr.	Name	Function / Register	
		Write	Read
0	TDR/RDR	Transmit Data Register	Receive Data Register
1	PR/SR	Programmable Reset	Status Register
2	CMR	Command Register	
3	CR	Control Register	

NOTE: Data don't care for programmable Reset.

JUMPERS

The SBC4D and SBC4D2 are provided with many jumpers to allow the boards to be adapted to the users specific requirements. Unless otherwise specified, all jumpers are provided with jumper plugs for quick and simple modifications. The jumper functions will be described below in consecutive order. Most functions are also printed on the circuit boards. Jumper functions up to **J13** are the same on both boards. From **J14** the functions are different.

Jumper **J1**, located between U7 and U6, is used to connect or disconnect the battery to or from the back-up circuits.

Jumper **J2**, located next to **J1**, is used to set the power supply voltage tolerance for back-up mode switching (respectively to 5% or 10%).

The jumpers **J3 up to J6**, respectively located near pin 1 and pin 28 of the EPROM socket **(J4, J3)** and pin 1 and pin 32 of the RAM socket **(J5, J6)**, are used to select the EPROM respectively RAM type that can be applied in the sockets U10 (RAM) and U11 (EPROM). The table in the next column shows the several combinations.

		A	B
EPROM	J3	< 32 kbyte	= > 32 kbyte
	J4	= < 32 kbyte	= 64 kbyte
RAM	J5	= 8 kbyte	> 8 kbyte
	J6	= < 128 kbyte	> 128 kbyte

NOTE: The maximum RAM capacity is 512 kbyte.

Jumper **J7**, located next to XT2 (crystal for CPU) is used to connect/disconnect the Interrupt output of the RTC to/from the local interrupt line. Disconnection may be useful during RTC software development and calibration of the RTC clock frequency.

Jumper **J8**, located between the GAL decoder (U6) and the battery, is used to select the memory map M1 respectively M2 (see also page 9).

Jumper **J9** and a section of the **J10** array are used to select the coupling mode of the watchdog timer. Both jumpers must be set in the appropriate position, either AC or DC. In the AC mode, the watchdog timer is cleared at the low to high transition of the source signal. In the DC mode, the counter will be cleared at a low level.

Jumper array **J10**, located next to the watchdog timer chip, is used to select the retrigger source (respectively CA2 or CB2 of the VIA or TxD of the USART/ACIA) and the watchdog delay time (1x, 2x or 4x the timebase of approximately 1.25 sec.). The timer is not active if the delay time jumper is removed or put in a neutral position.

Jumper **J11**, located near pin 1 of the CPU (U12) is used to connect the local interrupt line to IRQN or FIRQN.

Jumper **J12** , located between the battery and the bus connector, is used to allow the connection of the Q clock to pin 11 of the bus connector. **J12** is not installed in the standard versions.

Jumper array **J13**, located near the serial I/O header (CN3), is used to swap the IRQN and FIRQN lines from the bus extension header (CN2). See circuit diagrams for details.

Jumper **J14** is used on the **SBC4D2** to select between TxD1 (ACIA1) or TxD2 (ACIA2) as a possible source for the watchdog timer if TxD is selected in the **J10** array.

Jumper **J14** and **J15**, on the **SBC4D**, are strapped in standard version. They are used to change pin functions in the serial I/O header (CN3). **J15** straps DSRN to pin 9 and **J14** straps VCC (+5V to pin 5, to power external adapters). Straps are located at the solder side of the printed circuit board and can be removed with a sharp knife or equivalent tool. If necessary **J15** can be rewired to TxC (USART only) and **J14** can be rewired to DSRN. **NOTE:** If the optional CMOS ACIA is installed (SBC4D), inputs not used must be connected to VSS or VCC. The DSRN line, generally not connected on external adapter, can be connected to VCC via **J14**.

Jumper array **J16** is used on the **SBC4D** to select up to three possible interrupt sources from the USART to be connected to the local interrupt line. If the optional ACIA is installed, **J16** is not used.

NOTE: Standard boards, without page mode controller, are delivered with three wire bridges interconnecting the pins 9 → 10, 8 → 13 and 7 → 14 of socket U9.

MECHANICAL SPECIFICATIONS

1 **PRINTED CIRCUIT:** 1.6 mm epoxy glass fiber reinforced in eurocard format 160.0 x 100.0 mm. Double sided metallized with plated through holes and covered with a green epoxy mask on both sides. Finally covered with a white component overprint.

2 **BEMBUS CONNECTOR:** 31-pin (gold plated) DIN connector conform DIN 41617.

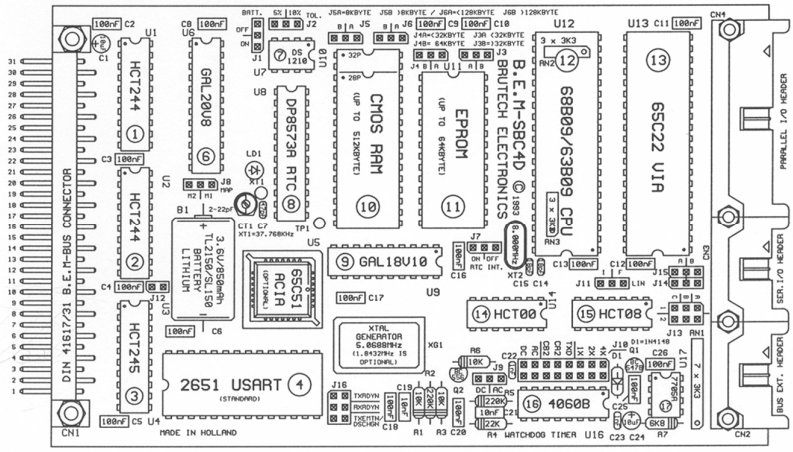
3 **HEADERS:** 1 x 26-pin and 2 x 10-pin right angle slim line flat cable headers accepting standard female flat cable socket connectors designed for flat cable with 0.050" (1.27 mm.) conductor spacing.

4 **SOCKETS:** Standard provided with high quality machine tooled sockets. Special sockets for PLCC devices (ACIA's).

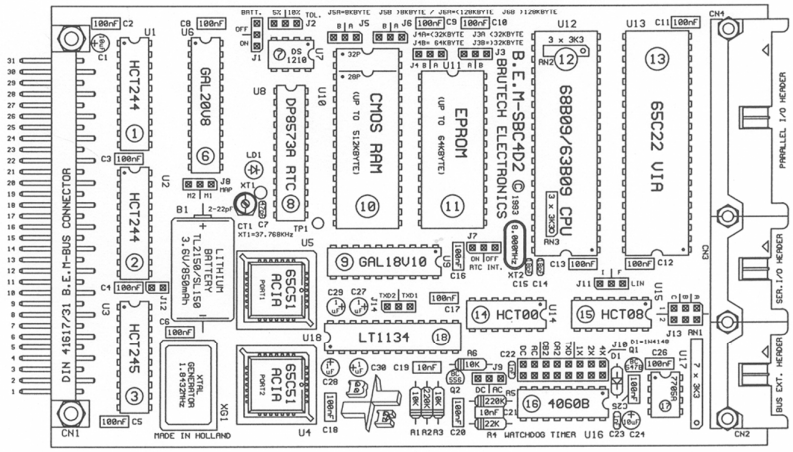
5 **MAXIMUM THICKNESS:**

Battery included: 17.5 mm.
Solder side: - 2.0 mm.
Component side: +13.7 mm.

MECHANICAL LAY - OUT B.E.M - SBC4D



MECHANICAL LAY - OUT B.E.M - SBC4D2



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