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D O U B L E D E N S I T Y D I S K C O N T R O L L E R

H A R D W A R E M A N U A L

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1. MTU-140 DISK SYSTEM OVERVIEW

The floppy disk controller in the MTU-140 computer is a separate board plugged into the motherboard and is located in the third slot from the bottom. The following MTU-140 system resources and functions are handled by this board:

A. 16K of read/write memory from address C000 through FEFF in bank 0.

B. Write protect circuitry for addresses E000-FEFF in bank 0.

C. 256 bytes of "bootstrap ROM" from address FF00 through FFFF (except FFE8-FFEF) which loads the CODOS operating system when the computer is turned on.

D. A double-density disk controller integrated circuit (NEC type uPD765).

E. Direct memory access circuitry to allow direct data transfers to and from the on-board memory without CPU interference.

F. Necessary Interfacing circuitry for up to four 8 inch disk drives terminating in a 50 pin ribbon cable header.

The disk drives are mounted in the computer enclosure and are connected to the disk controller with a 50 conductor ribbon cable. The cabinet may have either one or two double-sided, half-height 8 inch drives for a total of either 1M byte or 2M bytes of storage. Single drive systems may be later expanded two drives. DC power for the drives comes from a power supply mounted in the computer cabinet. AC power is not required by the drives normally used. For installations requiring 3 or 4 drives, an external drive cabinet may be "daisy chained" to the computer cabinet using a special cable.

2. DIRECT PROGRAMMING OF THE CONTROLLER

Thorough understanding of the following section is not necessary unless the customer wishes to write his own disk handling code. Normally the CODOS Disk Operating System supplied with the MTU-140 computer performs all of the disk handling functions required. However, special high speed data acquisition applications or utility programs for translating other diskette sector formats into CODOS standard format will require direct programming of the disk controller.

The following discussion is just a summary of the information needed for successful disk hardware programming. Its purpose is to establish an overview and point out the pitfalls discovered during development of the Disk Controller and CODOS. Answers to detailed programming questions can be found in the uPD765 Controller Chip Data Sheet in section 9 of this manual.

2.1 DISK CONTROLLER MEMORY MAP

The Disk Controller looks to the using system like two independent 8K blocks of memory. In the MTU-140, one block is addressed from C000-DFFF and the other is addressed from E000-FFFF, both in bank 0. Disk controller memory performs just like any other memory in the system but it does have two important features that other system memory does not. First, data transfers to and from the disk drives can use direct memory access with any of the Disk Controller memory but not with other system memory. Second, the higher 8K block (addresses E000-FFFF) can be write protected under software control. The most critical portions of CODOS reside in this block to minimize the possibility that errant user programs will "wipe out" the operating system.

The upper 8K block of Disk Controller RAM also includes the I/O registers for the uPD765 chip and the bootstrap ROM. The following chart gives a detailed memory map of the disk controller RAM (all addresses are in bank 0):

C000 to DFFF	Lower 8K of read/write memory.
E000 to FEFF	Upper 8K of read/write memory, can be software write protected.
FF00 to FFE7	Bootstrap loader PROM.
FFE8	Read - Hardware Status Read Write - Hardware Control Write
FFEA	Write-only, set DMA address register.
FFEE	Read-only, uPD765 Main Status Register
FFEF	Read/Write, uPD765 Data Register
FFF0 to FFFF	Remainder of bootstrap loader PROM.

2.1.1 Bootstrap Loader PROM

The Bootstrap Loader PROM is a 256 byte fusible link PROM selected for its small size and low cost compared with erasible PROM's. Eight of the 256 bytes are not available because they are overlayed by I/O register addresses. This PROM is supplied by MTU already programmed with a bootstrap loader that will read the CODOS Disk Operating System from disk and jump to it.

2.1.2 Hardware Status Read

Only two bits of the data read from this address are significant. Bit 7, which can be tested with the BMI and BPL 6502 instructions, is a zero if the uPD765 is requesting an interrupt and is a one if not. During DMA operations, this bit must be tested to determine when the operation is complete rather than reading the uPD765 main status register. Bit 6 is connected to the Option Jumper on the controller board and is a one if the jumper is installed. This is a read-only register.

2.1.3 Hardware Control Write

Only three bits of the data written to this register are significant. Bit 0 sets the DMA data transfer direction. When set to zero, data flows from the Disk Controller on-board memory to the disk and when set to one, data flows from the disk to the Disk Controller on-board memory. This bit must always agree with the read or write command given to the uPD765 for correct data transfer. System reset forces this bit to a zero.

Bit 1 controls write protect of the upper 8K block of Disk Controller RAM. When it is zero, normal write operation is allowed. When it is a one, writing into addresses E000-FEFF by the 6502 is prevented. The setting of this bit has no effect on DMA operations however. System reset forces this bit to a zero.

Bit 2 enables and disables interrupts from the uPD765 disk controller chip. When it is zero, actual 6502 IRQ interrupts from the Disk Controller are inhibited. When it is a one, an IRQ interrupt request to the MTU-140 6502 microprocessor will be generated whenever the uPD765 requests an interrupt. An interrupt service routine should test bit 7 of address FFE8 (the Hardware Status Read register) to determine if the Disk Controller is the source of the interrupt. The CODOS disk operating system does not normally use disk interrupts so it will keep this bit set to a zero. System reset forces this bit to a zero as well.

2.1.4 DMA Address Register

This is a write-only register used to specify where in Disk Controller memory a DMA transfer to or from the disk is to start. Only the upper 8 bits of the 14 bit DMA address counter may be set by writing to FFEA, the lower 6 bits will always be cleared to zero. The 8 bits of the DMA Address Register correspond exactly to bits 6-13 of the desired DMA address. Bits 14 and 15 of the desired DMA address must always be ones since only Disk Controller memory will support DMA. For convenience, one may write a subroutine to accept the desired DMA starting address and set the DMA Address Register accordingly.

Once set, the DMA address register will increment on every DMA cycle performed by the uPD765 disk controller. Thus if disk sectors are to be read into consecutive memory locations, the DMA Address Register need not be set at the beginning of every sector.

2.1.5 uPD765 Registers

The disk controller chip itself has only two registers. The Main Status Register is a read-only register that the uPD765 uses to tell the disk program what it is expecting and a little bit of information about the status of things. The uPD765 data register is used to send commands to the chip and receive detailed status from it. Operation in DMA mode is expected in which case the data register is not used for disk data. Please note that during a Read, Write, or Format command execution (which normally do DMA), that the program should not read or write any of the uPD765 registers. The reason is that the uPD765 cannot recover fast enough after a DMA cycle to do a CPU cycle correctly. During DMA, the Hardware Status Read register should be used to check on the busy status of the uPD765.

2.2 COMMUNICATING WITH THE uPD765

One of the problems in designing a floppy disk controller is the wide variety of data that must be exchanged with the using system. If a different address was used for each type of data, over a dozen addresses would be required. The uPD765 chip used by the MTU-140 Disk Controller approaches this problem by providing a single data "port" and then using an internal counter to direct the data to or from the correct internal register. With such a setup it is imperative that the internal counter be synchronized with the data so that it goes to or from the desired internal registers. The Main Status Register in the uPD765 is used to insure synchronization.

Actually the uPD765 tells the operating program what should be done next rather than vice-versa. This is accomplished with two bits in the Main Status Register at address FFEE. Bit 7 is called Request For Master (RQM) and when it is a one, the uPD765 wants the program to do something. If it is a zero, the uPD765 is busy and the program must not read or write the data register (unless the non-DMA mode is being used which is not considered here). Bit 6 indicates whether the uPD765 wishes to talk or listen. If it is a zero (and RQM is a one), the uPD765 is prepared to receive a command. If it is a one (and RQM is a one), the uPD765 has one or more status bytes available for reading.

2.2.1 Sending Commands to the uPD765

A command is sent to the uPD765 by first making sure that it is prepared to receive one (Main Status Register bit 7=1, bit 6=0). Then the first byte of the command is written into the data register. This action sets the internal address counter which distributes the remainder of the command bytes. It is important to test bit 7 of the Main Status Register for a one before each byte of the command is sent because of uncertain internal delays in disposing of command bytes. Note that the exact number of bytes defined for each command must be sent to the uPD765; no fewer and no more. The operating program must therefore be cognizant of the number of bytes the command requires because the uPD765 does not signal when the correct number has been received. When all of the command bytes have been received, the uPD765 starts executing the command and will be busy until the requested action is complete. (See the data sheet for details on simultaneous seek commands.)

2.2.2 Receiving Status from the uPD765

When the command is completed (except for Specify) the uPD765 will turn its Interrupt Request on which can be sensed by reading the Hardware Status Register bit 7. If the command was not a Specify, Seek, or Recalibrate, the uPD765 is now ready to send status bytes back to the using system. The program should test the Main Status Register for bit 7=1 and bit 6=1 before reading each status byte and status bytes must be read until bit 6 returns to a zero indicating readiness for the next command. Note that different commands give different numbers of status bytes and that their meaning depends on the command. The uPD765 will inform the using system when all status bytes have been read by setting Main Status Register bit 6 to a zero. Note that 12 microseconds should be allowed between reading a status byte and testing bit 6 of the Main Status Register to see if there are any others. The Specify command does not return any status bytes. The Seek and Recalibrate commands themselves do not return any status bytes either but must be followed by a Sense Interrupt Status command which will return status bytes.

2.3 COMMAND SEQUENCE DESCRIPTIONS

The following are very brief descriptions of the commands necessary for basic disk controller programming. Details on these and the very sophisticated search and scan commands may be found in the uPD765 data sheet.

2.3.1 Specify

The specify command is used to establish disk system operating parameters that remain constant. It must be executed first after every system reset. The first byte is the command code which is 03. The high nybble of the second byte is the two's complement of the stepping speed to be used on Seek and Recalibrate commands. Thus a value of A would be used for 6MS stepping (167 steps/second). The low nybble specifies how long the head should remain loaded to the disk after a read or write command completion in 16 MS increments. The maximum value (F or 240MS) is normally recommended. The most significant 7 bits of the third byte specifies the head load time allowed for the disk drive in 2 millisecond increments. 40MS should be adequate for any kind of drive. Note that this is also the time allowed for head settling after a seek before attempting to read or write data. The least significant bit of the third byte is normally a zero which specifies the DMA mode of data transfer. The Specify command is executed immediately, does not generate an interrupt, and returns no status bytes.

2.3.2 Recalibrate

The Recalibrate command is used to position the head on the selected disk drive to track 0 without making an assumption about where it is presently. This should be the second command executed after reset but can also be used as part of an error recovery procedure. The first byte of the Recalibrate command contains the command code of 07. The least significant two bits of the second byte specify the drive number in binary of the drive to be recalibrated. The reamining bits should be zero. After sending the Recalibrate command, the Disk Controller is able to accept additional Recalibrate or Seek commands for the other drives thus allowing simultaneous seek. For simplicity one may program just one recalibrate at a time if desired.

When the Recalibrate is complete, the Interrupt Request is raised by the uPD765 (Hardware Status Register bit 7=0). The program should respond by sending a Sense Interrupt Status command to the Disk Controller. This is a one byte command with a code of 04. The Disk Controller will then respond with 2 status bytes. The first byte tells how the Recalibrate command terminated. For normal termination, bits 6 and 7 will be zeroes. Otherwise an error condition occurred and the Status Register 0 table on the uPD765 data sheet should be consulted. Common errors during Recalibrate include failure to reach track 0 after 77 step pulses and the disk drive becoming not ready during its execution. The second status byte is always 0.

2.3.3 Seek

The Seek command is used to position the head to the desired track for reading or writing. The first byte is the command code which is 0F. The least significant bits of the second byte specify the drive number. Bit 2 specifies the head number for two-sided disk drives. The third byte gives the track number to seek to in normal binary code. Execution and completion of the Seek command are the same as with Recalibrate. The second status byte returned by the Sense Interrupt Status command however should be equal to the desired track number.

2.3.4 Read

The Read command is used to read data from the diskette into memory on-board the Disk Controller. If the final destination is elsewhere in memory, a move routine will have to move it there after it is read. Before executing the Read command, the disk head must be on the desired track, the DMA Address Register set to the desired memory address to receive the data, and the DMA direction bit set for write (Hardware Control Register bit 0=1).

Once a Read command is started, the disk controller will continuously read sectors in ascending order until it is stopped by the DMA controller or all of the sectors in the track have been read. Since the DMA controller used on the Disk Controller does not have a byte count register, the Read command will stop only after the last sector on the track has been read. Fortunately, the Read command itself can specify any number of sectors per track even if it is not the actual number. Thus single sector reads are accomplished by setting the final sector number (EOT) equal to the sector number to read. Although the disk controller will indicate an abnormal command termination, there are no ill effects.

The Read command requires 9 bytes. The first is the command code which also specifies the data density and other information. The normal code of 46 gives double-density, makes no distinction between normal and deleted data address marks, and does not automatically continue a read command from one side to the other on double-sided drives. The second byte specifies the drive number and diskette side in the same format as the Seek command. The third byte must be equal to the track number the head is currently at. The fourth byte is the side number (=0 for single sided drives, 0 or 1 for double-sided drives). The sector number to start reading at is the fifth byte. The sixth byte in conjunction with the ninth byte gives a code for the number of bytes in the sector. For the 256 byte sectors used by CODOS, the sixth byte should be set to 01 and the ninth set to FF. The seventh byte gives the last sector number to read. It should equal the fifth byte to specify a single sector read. The eighth byte gives the gap length between sectors and is normally set to $0E for 26 sectors, 256 bytes/sector, double density.

When the read operation is complete, the controller will request an interrupt and the program should respond by reading status bytes back. (Do <u>not</u> execute a Sense Interrupt Status to get the status.) The first three status bytes (from a total of 7) give an error code. Normal termination is for the first byte to read 40+4*(head number)+(drive number) which is hex 40 for a single-sided drive 0. The second status byte should read hex 80 and the third should be all zeroes. Anything else indicates some kind of read error and the data sheet should be consulted for the meaning.

2.3.5 Write

In most respects the Write command is identical to the read command. Before executing a write however the DMA direction bit should be set for read (Hardware Control Register bit 0=0). Once a Write command has been started, it will write continuously just like the read command. This is handled in the same way as with the Read command. The normal command code for write is 45 which gives double density and does not continue writing from one side to the other on double-sided disks. The remaining 8 bytes of the command are exactly the same as for the corresponding Read command. Also, execution and the 7 status bytes returned at completion are the same as for Read.

Following the write command a delay of at least 500uS <u>must</u> elapse before attempting to seek. If this delay is not allowed, either the drive will ignore the first step pulse or data on the adjacent track will be damaged by the tunnel erase head which remains energized for 500uS after the write current is turned off.

2.3.6 Format

The Format command is used to erase a disk and write the various address marks necessary to define the sector boundaries. The Format command applies to an entire track although all tracks on a disk need not be formatted the same way. The standard format for CODOS disks is similar to that used on IBM double density systems except that all tracks are double density. This format defines 26 sectors of 256 bytes on each of 77 tracks for a total of 512,512 bytes per diskette side. An alternate format useful for high speed data acqusition (e.g. digital audio) might use 8 sectors of 1024 bytes for a total of 630,784 bytes, a 23% increase.

The command code for Format is normally 4D which specifies double density. The second byte specifies the drive and head number as with read and write commands. The third byte is a code for the number of bytes per sector; 01 is used for 256 bytes and 03 is used for 1024 bytes. The fourth byte is the number of sectors per track and would normally be 1A hex for 26 decimal sectors per track. The fifth byte gives the gap length between sectors which is normally 36 for double density. The sixth byte is the filler value to which all of the data bytes will be set.

During execution of the Format command, additional formatting data is read from memory via direct memory access. Thus before executing the Format command the DMA direction must be set to read (Hardware Control Register bit 0=0), the DMA address register set, and the formatting data to be described prepared in memory. Each sector to be formatted reads 4 bytes from memory. The first byte must equal the track number that is being formatted. The second byte must equal the side number being formatted (set to 0 for single sided). The third byte gives the sector ID for the sector being formatted. The fourth byte is a code for the sector length and must be equal to the third byte of the command string described above. For formatting 26 sectors then, 4*26 or 104 bytes of formatting data will have to be set up in memory.

Note that the sectors need not be sequentially numbered around the track and each track can be different thus allowing optimized numbering for faster throughput when the disk is later read or written. CODOS format takes advantage of this and uses alternate numbering and staggering from track to track to attain an average throughput of about 20K bytes per second when reading sequential data from disk such as when loading a program. The exact format is described in the CODOS manual.

When the entire track has been formatted (as signalled by the second occurance of the index hole), an interrupt is generated and 7 status bytes may be read. Normal termination is for the first status byte to read 4*(side number)+(drive number) and the second and third status bytes to read zero. As with the Write command, a delay of at least 500uS must elapse before issuing a Seek to the next track so that tunnel erase is completed.

3. JUMPER OPTIONS

Since it was designed to accomodate a variety of system configurations, the Disk Controller board has a number of jumper options. These have already been set for proper operation in the MTU-140 computer. Therefore, any change by the user would be to accomodate special requirements. The effect of jumper settings is only summarized here. A full explanation may be found in the full K-1013 Disk Controller manual available separately at extra cost. In the listings below, the standard setting for the MTU-140 is designated with an *.

3.1 ADDRESS SELECTION JUMPERS

To the using system, the Disk Controller looks like 16K bytes of memory. This 16K is actually broken down into two completely independent 8K blocks. One of these blocks, which is called User RAM, is totally free for use as 8K of read/write memory. The other block, which is called System RAM, consists of 7.8K of read/write memory, 248 bytes of read-only memory, and the various I/O port registers associated with the disk controller chip (see the Programming section). Each block has its own set of address selection jumpers which are small staple- shaped pieces of wire which plug into standard IC sockets. The physical location of these sockets may be determined by looking at the Component Layout section. Note that when 18 bit addressing is used, the board must be addressed in the range of 8000 to FFFF within the selected bank.

BANK	JUMPER SETTING
0	U47-5 to U47-12*, U47-1 to U47-16*
1	U47-3 to U47-14, U47-1 to U47-16
16 bit addr.	U47-2 to U47-15

ADDRESS RANGE	SYSTEM RAM JUMPERS			U27	USER RAM JUMPERS			U27
0000 - 1FFF				8-9				4-13
1000 - 2FFF			7-10				3-14	
2000 - 3FFF			7-10	8-9			3-14	4-13
3000 - 4FFF		6-11				2-15		
4000 - 5FFF		6-11		8-9		2-15		4-13
5000 - 6FFF		6-11	7-10			2-15	3-14	
6000 - 7FFF		6-11	7-10	8-9		2-15	3-14	4-13
7000 - 8FFF	5-12				1-16			
8000 - 9FFF	5-12			8-9	1-16			4-13
9000 - AFFF	5-12		7-10		1-16		3-14	
A000 - BFFF	5-12		7-10	8-9	1-16		3-14	4-13
B000 - CFFF	5-12	6-11			1-16	2-15		
C000 - DFFF	5-12	6-11		8-9	1-16*	2-15*		4-13*
D000 - EFFF	5-12	6-11	7-10		1-16	2-15	3-14	
E000 - FFFF	5-12*	6-11*	7-10*	8-9*	1-16	2-15	3-14	4-13

3.2 SYSTEM CHARACTERISTICS JUMPERS

The IRQ Enable jumper is placed between U47 pins 8 and 9*. When installed and Disk Controller interrupts are enabled by Hardware Control Register bit 2 being set to 1, an interrupt request from the disk controller chip will cause an IRQ sequence in the 6502 to occur if the 6502 Interrupt Disable bit is turned off. The Disk Controller may be identified as the source of the interrupt by polling the Hardware Status Register (see Programming section). The CODOS Disk Operating System does not require interrupts to function, however, the jumper is normally installed so that user programs can use disk interrupts if desired.

The IPL Option jumper is placed between U47 pins 6 and 11. Its only function is to set bit 6 in the Hardware Status Register to a one if present. The interpretation of this bit is entirely up to the user; the bootstrap loader PROM and CODOS both ignore bit 6. This jumper is not normally installed in the MTU-130.

The Vector Fetch Enable jumper is placed between U47 pins 4 and 13. When installed, pin 19 of the MTU-130 bus will be pulled low whenever an address in the range of FF00 through FFFF (regardless of bank) is on the Address Bus. In the MTU-130, pin 19 of the bus does not connect to any system component but can be used by custom designed bus interface boards if desired. This jumper is normally removed.

3.3 DISK CHARACTERISTICS JUMPERS

The Write Precompensation jumpers are used to control the amount of write precompensation used in double-density operation. These jumpers have no effect on standard density operation but one must be present for the write circuitry to function. 125NS is normally chosen for 8 inch disks and 250NS for 5 inch disks. In some cases with older drives not rated for double density, better results are obtained with 250NS for 8 inch and 500NS for 5 inch.

*	U41-1 to U41-16	125NS
	U41-2 to U41-15	500NS
	U41-3 to U41-14	250NS

The Force 2-Sided jumper is used force the Two Side Sense input to the disk controller chip to a logic one. This in turn sets bit 3 of status register 3 to a one which indicates that a two-sided drive and diskette are present in the system. Its practical function is to allow the use of both sides of single-sided diskettes in two-sided drives (note however that single-sided diskettes are only certified on one side). True 2-sided diskettes have the aperture for the index sensor in a different location so that two-sided drives can sense when two-sided diskettes are being used. This jumper is normally removed.

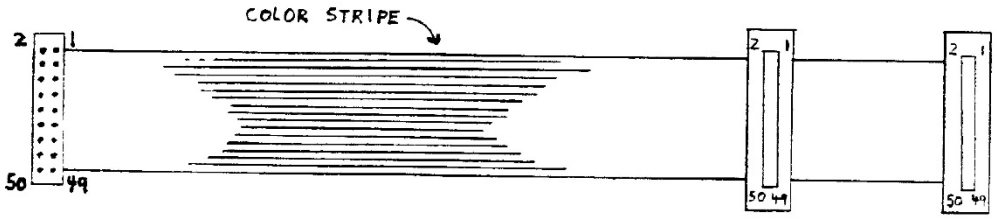
The Write Clock jumper selects between 8 inch and 5 inch drives. This is not a pluggable jumper; rather it is an etch cut and a soldered-in jumper. Since the MTU-130 and CODOS use only 8 inch drives, the write clock is set for 8 inch disks. To use 5 inch disks in a specialized application, the line between J1 and J2 must be cut and then a jumper placed between the two J1 points and another placed between the J2 points. Note also that for operation with 5 inch drives that 470pF 5% polystyrene capacitors must be installed at C90, C92, and C94, 1000pF 10% at C86 and .01uF 10% at C96. Also the data separator adjustments should be performed as described in the Adjustment Procedure section.

4. CONNECTION TO NON-MTU DISK DRIVES

While MTU disk drives and matching MTU cabinets and cables are preferable from the standpoint of performance and ease of setup and test, the MTU-140 Disk Controller is flexible enough to interface to a variety of disk drives. The primary requirement is that the disk drives must be standard size (8 inches).

Disk drives with a Shugart compatible connector are greatly preferred. These include but are not limited to: Shugart SA-800/801 and 850/851, Siemans FDD-100 and FDD-200, Control Data 9406, and Qume Datatrak 8. Either the single-sided or double-sided versions of the above drives may be used. If a non Shugart compatible drive is used, an adapter board or cable will have to be constructed. Refer to the Pin Connections section for pin numbers in the disk cable used by the controller.

Assuming that a Shugart compatible disk drive is used, the cable required is very simple. It should be a 50 wire ribbon cable with .050" between conductor centers (3M type number 3365-50) with a female ribbon cable connector on one end (mates with dual row .025" square posts on a .1" grid, 3M type number 3425-0000), and a female card edge connector on the other end (mates with 50 pin double-sided PC edge fingers on .1" spacing, 3M type number 3415-0001). If two or more drives are to be used in a system, additional female card edge connectors can be pressed onto the same cable with a spacing of 6" between centers (assuming upright mounting of the drives with not more than 1" spacing between drives) up to a total of 4 connectors. The total cable length should not exceed 10 feet and lengths of less than 5 feet are preferred. A drawing of the required cable configuration is shown below:



If more than one disk drive is used, the drive select jumpers in the drives will have to be re-configured. Following the instructions in the drive manual, set the jumpers in the first drive for 0, the next for 1, etc. The Disk Controller does NOT use binary select so ignore anything in the drive manual about binary select.

Most disk drives have additional jumpers to control other aspects of their operation. The list below shows what the controller expects of the drive and the jumpers should be configured accordingly.

1. The READY line should be daisy chained, not radial.

2. The stepper motor should either be energized continuously or when step pulses are present. Energizing only when the head is loaded or the drive is selected is NOT acceptable.

3. The Track 0 Sense should be daisy chained, not radial.

4. If an activity LED is on the drive front panel, it is of most value if it turns on when the drive's head is loaded.

5. The MTU Disk Controller board has its own data separator. Any separator in the drive should be disabled and the Raw Read Data should appear on pin 46.

6. The MTU Disk Controller board uses soft sectoring. Any sector separator circuitry on the drive should be disabled and the index sense signal should appear on pin 20.

7. If present, the Write Protect Sensor should be enabled.

8. If present on a double sided drive, the Double Sided Sensor should be enabled.

9. If a door lock solenoid is provided, it probably should not be used unless the disk is part of a turnkey system with unsophisticated operators. If it is used connect it to the Head Load signal so that the door is locked only when the head is loaded.

10. Any other radial-vs-daisy chain options should be set for daisy chain.

11. If in doubt about any other options, remember that the disk controller constantly scans the disk drive status at about a 1kHz rate (except when actually reading or writing) by selecting the drives one-at-a-time. Thus Drive Select alone should not initiate functions such as head load, stepper power, or light the front panel activity indicator.

MTU has application notes available that describe specifically how to jumper the more popular disk drives. If your drive is one of those covered, it is strongly suggested that the matching application note be obtained since drive manufacturer's instructions are typically very difficult to interpret.

AN-8 Covers the Shugart SA800/SA801
AN-9 Covers the Siemans FDD-100-8
AN-11 Covers the Siemans FDD-100-8D and FDD-100-8E
AN-12 Covers the the Shugart SA850/SA851
AN-13 Covers the Siemans FDD-200-8

5. PRINCIPLES OF OPERATION

The Disk Controller is basically a 16K memory board with a disk controller IC, direct memory access logic, TTL registers, and 256 bytes of PROM added. In operation it is synchronized to the 6502 bus cycle which is expected to be 1.0MHz to close tolerances.

Section 14 shows a block diagram of the Disk Controller board. Data are exchanged among the various elements of the board via a central bidirectional data bus. Because of the two-phase bus cycle of the 6502, this internal bus can be devoted to internal operations such as direct memory access and memory refreshing during Phase 1 and then turned over to the 6502 (if the board is addressed) during Phase 2. The memory IC's and the uPD765 disk controller IC are therefore operated at a 2mHz cycle rate which these modern devices handle quite well. The address bus is unidirectional being simply a buffered version of the 6502 address bus and two levels of multiplexors are used to select addresses from one of three sources for the RAM chips themselves.

5.1 ADDRESS RECOGNIZER

Because of the large number of different address ranges to be decoded and flexible address jumpering, a fairly large amount of logic located at the right side of page 1 of the schematics is devoted to address recognition. All 16 address lines are first buffered by U1 and U2 which are low power non-inverting octal buffers to produce LOC AB0 through LOC AB15. U29-6 in conjunction with inverters at its input produces KIM DEC ENAB which goes low when addresses in the range of 0000 through 1FFF are on the address bus. U8-8 detects addresses in the range of FF00 - FFFF and generates KIM VECT FETCH when they are seen. Neither KIM signal is of any significance in the MTU-140 computer but they are important in other applications of the Disk Controller.

Provisions for an 18 bit address bus were added after the board was designed. Nand gate U57 responds when a Bank 0 (or Bank 1 with a jumper change) address is on the bus and address bit 15 is high. The unused half of U58 is used as an inverter for the Board Selected signal and the result is sent to the remainder of the address decoder.

The first level of address decoding determines whether the User RAM block or the System RAM block is addressed, if either. This is accomplished with two completely separate circuits. A block recognizer operates by taking the 4 most significant address lines and then adding a 4 bit constant to them with a 4 bit adder. When the sum is either E or F, the recognizer is satisfied. The value of the constant is determined by 4 jumpers which in turn determine the 8K range on 4K boundaries that the recognizer will respond to. U28 in conjunction with U29-8 recognizes addresses intended for the User RAM block while U18 in conjunction with U29-12 recognizes System RAM addresses. Test points are provided for USRRAM ADRD and SYSRAM ADRD to facilitate troubleshooting. U39-8 logically OR's the two signals together to produce a board addressed signal.

U17-8 determines if the on-board PROM might be addressed by looking for an F from the System RAM adder (U18) and LOC AB8 through LOC AB11 to be all ones. U7-8 looks for addresses between xxE8 and xxEF which are candidates for the various I/O registers on the board. U38-12 makes the final decision about whether a System RAM address actually refers to RAM by requiring that SYSRAM ADRD be true and that the output from U17-8 be false. U38-6 makes the final decision about PROM addresses by requiring that SYSRAM ADRD be true, U17-8 be true, and U7-8 be false. U38-8 makes the final decision about I/O addresses by requiring SYSRAM ADRD be true, U17-8 be true, and U7-8 be true. When I/O addresses are detected by U38-8, U40, which is a 1-of-10 decoder, is enabled which looks at LOC AB0, LOC AB1, and the read/write line to determine exactly which device to activate.

5.2 DATA BUS BUFFERS

The data bus is buffered by two octal buffers, U3 and U9. If something on the board is addressed and the 6502 is performing a Read cycle (6502 R/$\overline{W}$ high), U9 is activated during PHASE 2 to drive the 6502 data bus with read data. If something on the board is addressed and the 6502 is performing a Write cycle (6502 R/$\overline{W}$ low), U3 is activated during PHASE 2 to drive the internal data bus (LOC DB0 - LOC DB7) with write data. Neither buffer is activated during PHASE 1 in order to reduce noise generation.

5.3 HARDWARE CONTROL REGISTER

The Hardware Control Register is in the middle of schematic page 2 and consists of a quad D-type latch with complementary outputs. It is clocked by the trailing edge of CNTL WRT which is activated when address 1FE8 in the System RAM (FFE8 in the MTU-140) is written to. When clocked, the least significant 4 data bus bits are latched. Bit 0 controls the direction of DMA data transfers, bit 1 allows or inhibits writing into the System RAM by the 6502, and bit 2 gates the interrupt request signal from the controller chip onto the system IRQ bus line. Bit 3 is unused. Reset from the bus is connected to reset all 4 bits in the register to put them into a known state (DMA mode=read, System RAM write enabled, interrupts disabled) at power-up.

5.4 HARDWARE STATUS REGISTER

The Hardware Status Register is at the top left corner of schematic page 3. It consists simply of two tri-state buffers which gate data onto LOC DB6 and LOC DB7 when activated by STATUS READ which in turn responds to read cycles from address 1FE8 in the System RAM. The Interrupt Request line from the uPD765 floppy chip is gated onto LOC DB7. A pluggable jumper determines the logic level gated onto LOC DB6.

5.5 DMA ADDRESS COUNTER

The DMA address counter is in the center of schematic page 4. It is a 14 bit counter with the least significant 6 bits being U22 which is an asynchronous clearable counter and the most significant 8 bits being U33 and U43 which are 4 bit synchronous loadable counters. Only 14 bits of counter are necessary because there is only 16K of on-board memory to address.

Normally the counters are set up to count pulses seen on the DMA CYC line. When the most significant bit of the asychronous counter makes a 1-to-0 transition, it is coupled through C77 and U62-6 to clock the synchronous counters which are set up for counting. However when the address decoder generates DMA CNT LD, the asynchronous counters are cleared and the synchronous counters are loaded from LOC DB0-LOC DB7. The delay network formed by R15 and C58 insures that the counters are kept in the Load Enable state long enough after clocking to load properly. U62-6 functions as an OR gate so that the synchronous counters are clocked either by DMA CNT LD or by a carry out from the asychronous counters.

5.6 IPL PROM

The IPL ROM is at the left center of schematic page 4. It is activated during read cycles when ROM CS1 is true by virtue of its two chip select inputs. Its 8 address inputs are connected directly to LOC AB0 - LOC AB7 for addressing of its 256 bytes. The 8 tri-state outputs are connected directly to the on-board LOC DB bus. A type 6309 (or equivalent) 256 word by 8 bit fusible link PROM is used. Note that locations E8-EF cannot be read from the PROM because the address decoder overlays them with I/O register addresses.

5.7 uPD765 FLOPPY DISK CHIP ADDRESSING

The uPD765 Floppy Disk Controller IC is located at the upper left corner of schematic page 3. It has only two internal registers that must be addressed. LOC ABO is used to distinguish between the Main Status Register and the Data Register. The uPD765 has separate $\overline{RD}$ and $\overline{WR}$ inputs which are used to strobe data from and into internal registers respectively. The driving signals, FDC $\overline{RD}$ and FDC $\overline{WRT}$ are generated by the DMA logic which simply OR's DMA access to the uPD765 with outputs from the address decoder for 6502 access. Its bidirectional data bus is simply tied to the on-board LOC DB bus.

5.8 TIMING GENERATOR

The timing generator is at the left side of schematic page 2. All timing is generated by counting down an 8mHz clock and then decoding the count in various ways to insure that accurate timing is always generated. The timing diagram in section 11 may be consulted for detailed timing relationships.

The timing generator is synchronized to the trailing edge of 6502 PHASE 2 by means of a phase-locked loop which is at the bottom left of the drawing. U57-8 is a simple Schmidt trigger oscillator with a nominal frequency (which can be adjusted with R27) of 8MHz. By connecting R30 to the R-C node, the frequency can be controlled by the application of a DC voltage to its free end. Although the linear control range is only 20% or so, it is ample for locking onto the crystal controlled system clock. The 8MHz output at U57-8 is normally asymetrical (35% high, 65% low) and goes to a number of places including the synchronous 4 bit counter, U21. U31-6 decodes the counter status to produce a low-going signal with duty cycle of 25% at a frequency of 1MHz. This is the comparison signal for the phase comparator. 6502 PHASE 2 is the reference signal and U50 is used as a phase comparator. The output of the phase comparator simply floats for 3/4 of each 1uS cycle since it is actually a tri-state gate. When it is enabled by U31-6, the output first goes high (since when locked 6502 PHASE 2 would be high), then goes low when 6502 PHASE 2 terminates, and then floats when disabled by U31-6. The ratio of high-to-low time of this signal is averaged by lowpass filter R31, C84, and R29 which is then the control voltage to the 8MHz oscillator.

Normally the trailing edge of 6502 PHASE 2 occurrs midway in the "window" defined by the output of U31-6. Locking action can be understood by considering what would happen if 6502 PHASE 2 terminated later in the window, i.e., slowed down slightly. The output of the phase comparator would then be high for a longer time and low for a shorter time thus raising the averaged control voltage. Since a higher control voltage slows down the oscillator, the window frequency would decrease to match the input. The converse would occur if 6502 PHASE 2 should speed up. R27 can be adjusted to center the trailing edge of 6502 PHASE 2 in the window for accurate timing. This circuit has been found to be highly reliable and is used in many MTU products to provide a phase locked high frequency clock for timing.

The most critical timing signals needed are those that operate the 16K dynamic RAM chips. U42-6 and both halves of U32 are set up as a 3 bit shift register delay line to generate the $\overline{RAS}$, address swap, and $\overline{CAS}$ sequence needed by the memories. A memory cycle is started if MEM CYC ENAB is true when bit 0 of the 4 bit timing counter is high, bit 1 is low, and a positive edge of 8 MHZ CLOCK is seen. U42-6 then goes low generating $\overline{RAS}$ which starts the timing chain for the memory cycle. The next negative edge of 8 MHZ CLOCK flips U32-6 which through the memory address multiplexor, switches from row address to column address. Finally, the next positive edge of 8 MHZ CLOCK after the address is switched generates $\overline{CAS}$ which latches the column address in the RAM chip and activates the RAM I/O circuitry. At the end of the memory cycle, U42-6 is set back high by the transition of counter bit 1 from 1 to 0. U32-6 and U31-10 then switch back high in preparation for another memory cycle.

The uPD765 Floppy Disk Controller IC requires a Write Clock signal that is exactly twice the bit rate to the floppy disk and is 250NS wide independent of its frequency. U5-10 acts as a fifth counter bit on the timing generator and in conjunction with U31-3 and U11-6 produce FDC WRT CLK at a frequency of 1.0MHz, .5MHz, or .25MHz depending on the disk type and recording density. With the J1 and J2 jumper set for standard 8" disks, FDC WRT CLK will be .5MHz if MFM MODE is a logic one and will be 1.0MHz if MFM MODE is a logic zero, With the J1 and J2 jumpers set for mini disk operation, both frequencies are divided by two for .25MHz and .5MHz respectively. The pulse width in all cases is 250NS.

Z11 produces a .5uS pulse every 4uS which triggers a refresh cycle for the memory chips. However, if a DMA cycle is in progress the refresh cycle is omitted until the next 4uS period. There is no chance that DMA will lock out refreshing however because the maximum data rate to or from the disk is every 16uS. Even if every DMA cycle preempted a refresh cycle, the refresh rate would only drop from 128 cycles per .5MS to 128 cycles per .62MS.

5.9 MEMORY CYCLE CONTROL

The Memory Cycle control circuitry is at the top right of schematic page 2. Its main function is to determine if a memory cycle is needed during PHASE 1 and if so, whether it is a DMA cycle involving the uPD765 chip or a refresh cycle. It also distinguishes between read and write cycles based on the setting of the DMA WRITE and WRITE PROT flip-flops. A DMA control chip, such as an 8257, was not used because it is too slow to control .5uS memory cycles.

U42-10 is used to synchronize DMA requests from the uPD765 to memory cycle oppertunities during PHASE 1. When U42-10 is set, it sends an acknowledge back to the uPD765 (FDC DACK) which then drops its request. The request is dropped soon enough so that two DMA cycles are not taken. U52-11 logically AND's the DMA flip-flop with CNTC (which is approximately the same as PHASE 1) and generates DMA CYC and DMA CYC through inverter U53-12. If the DMA mode is read, U52-3 will generate a write pulse coincident with DMA CYC for the uPD765 which is OR'ed with write pulses from the 6502 in U62-3. If the DMA mode is write, U52-6 will generate a read pulse which is OR'ed with reade pulses from the 6502 in U62-11. The delay network consisting of R52 and C98 prevents possible overlap of the uPD765 driving the LOC DB bus before the RAM chips have stopped driving it.

Considerable logic is required to generate RAM WE only when needed. U52-8 requests the generation of RAM WE during all DMA cycles when the DMA mode is write. U30-6 requests RAM WE when the System RAM is addressed by the 6502, a 6502 write cycle is in progress, and the Write Protect is off. CNTC is factored in to include only 6502 cycles during PHASE 2. U20-6 requests RAM WE when the User RAM is addressed by the 6502 and a 6502 write cycle is in progress. All of these requests are OR'ed together in U20-12. The result is AND'ed with RAS to produce a properly timed RAM WE pulse for the RAM chips.

The circuitry at the top right of schematic page 1 also controls memory cycles. U30-8 OR's cycle requests from 4 different sources to produce MEM CYC ENAB which then triggers the timing generator to execute a memory cycle. Two of the sources, DMA CYC and REF CYC have already been covered. The third source is User RAM Addressed and the fourth is System RAM Addressed AND'ed with PROM not addressed.

5.10 REFRESH ADDRESS COUNTER

The refresh address counter is at the bottom left corner of page 4. It is simply an 8 bit asynchronous counter that counts up on the trailing edge of REF CYC pulses. The eighth bit is not needed to refresh 16K RAM chips.

5.11 MEMORY ADDRESS MULTIPLEXOR

The Memory Address Multiplexor is at the bottom right of schematic page 4. It is actually a two-level multiplexor and simultaneously performs address selection from 3 different sources and row/column multiplexing for the RAM chips. U13 and U23 form the first multiplex level which selects between the refresh address and the low 7 bits of the DMA address. Note that the high 7 bits of the DMA address will actually be the high 7 bits of the refresh address but these address bits are ignored during refresh cycles.

The output of the first level multiplexor along with the upper 7 DMA address bits and all 14 of the 6502 address bits enters a 4 input 7 bit multiplexor made from U14, U24, U34, and U44. One of the select inputs to this multiplexor selects between 6502 address and DMA/refresh address under the control of CNTC. Thus the 6502 address is selected during PHASE 2 and the DMA/refresh address is selected during PHASE 1. (Actually there is some timing skew because CNTC is not the exact inverse of PHASE 2.) The other select input is connected to the MUX ROW/$\overline{\text{COL}}$ output of the timing generator which selects between the lower 7 address bits (row address) and upper 7 address bits (column address) at the proper point in the memory cycle. Since only 8 type 4116 RAM's are being driven, the bare outputs of the 74LS153's in the multiplexor are sufficient to drive the address inputs.

5.12 MEMORY ARRAY

The actual memory matrix is at the top of schematic page 4. All lines to the memory chips except data input and data output are simply wired in parallel. One .1uF capacitor per chip on both the +12 and -5 power supply busses and a gridded ground network on the board minimize noise generation. Since "early write" timing is used on the RAM's, their data input and data output lines can simply be connected to the on-board bidirectional LOC DB bus.

5.13 FLOPPY DISK INTERFACE

Unfortunately the inputs and outputs of the uPD765 Floppy Disk Controller IC cannot be simply connected to a floppy disk drive. Instead, most signals must be buffered and some must be multiplexed because of pin count limitations of the uPD765. In a system with several disk drives, all are parallel bussed and only one at a time is selected by the Disk Controller for operation. U61 is a decoder that accepts the two Unit Select outputs of the uPD765 and pulls one of the DRV SEL lines low in response. The drive responds by sending status back to the controller and accepting commands, if any, from the controllet. Except during read and write operations, all 4 drives (even if they are not installed) and being scanned at a 1KHz rate for status changes.

Four of the uPD765 pins are multiplexed to give the effect of 8 in two groups of 4. The signals that are multiplexed have been chosen so that 4 of them are significant only during read/write operations and the other 4 are significant only during seeking and idle periods. A signal from the uPD765 called RW/SEEK determines which group is active. The signals within a group are further divided into 2 input signals (drive to uPD765) and 2 output signals. Quad tri-state inverters U50 and U59 are appropriately wired to do the necessary multiplexing and demultiplexing with high output drive capability. The 4 input signals that are multiplexed are $\overline{\text{WRITE PROT}}$, $\overline{\text{TRACK 00}}$, $\overline{\text{2-SIDE SENSE}}$, and $\overline{\text{FAULT SENSE}}$. The latter signal is not normally present on Shugart compatible drives so it simply goes to a pad on the K-1013. The 4 output signals that are multiplexed are LOW CURRENT, $\overline{\text{STEP}}$, $\overline{\text{STEP IN}}$, and $\overline{\text{FAULT RESET}}$. Like $\overline{\text{FAULT SENSE}}$, $\overline{\text{FAULT RESET}}$ simply goes to a pad. The $\overline{\text{READY}}$ status from the disk drive is not multiplexed and is simply inverted by U51-8 before going to the uPD765. INDEX is likewise inverted by U51-10 and sent directly to the uPD765.

Three outputs from the uPD765 are buffered and sent to the disk drive. These are HDL (HeaD Load), HD (HeaD select for double-sided drives), and WE (Write Enable). The interrupt request output goes directly to the Hardware Status gate (U59). It is also gated by Interrupt Enable (U10-15) with a diode And gate and goes through open-collector inverter U60 to the 6502 IRQ bus line if the IRQ ENAB jumper is installed. The 8MHz clock input to the uPD765 is buffered and given an appropriate duty cycle by U51-6. Pullup resistor R52 gives the somewhat higher logic 1 level required by the uPD765.

5.14 WRITE PRECOMPENSATION

During readback of double-density data from diskette, the recorded pulses experience a predictable shift away from their ideal positions in time which make data decoding errors more likely. This tendency may be counteracted by shifting the pulses in the opposite direction when written which is called precompensation. The uPD765 internally computes whether a pulse should be written early, on-time, or late and supplies this information on the PS0 and PS1 lines to the write logic.

U48 is connected as a 3 bit shift register which shifts the FDC WRT DATA output of the uPD765 at a rate determined by the PRECOMP jumper currently in use. Thus the A, B, and C outputs of the register represent early, on-time, and late pulse timing respectively. Multiplexor U58 selects one of these pulses under control of PS0 and PS1 and sends the result through U60-12 for buffering to the disk drive.

5.15 DATA SEPARATOR

More than any other portion of a disk controller the data separator determines the overall reliability of the disk system. Not supprisingly, it is also the most difficult circuit to design. The data separator used is a true analog phase locked loop with none of the time quantization error found in digital phase locked loops.

Actually the uPD765 does the separation of data pulses from clock pulses internally but it must have a clock input (called FDC DATA WINDOW) synchronized to the pulse stream to function. This clock input is a square wave phased to the pulse stream such that pulses occur near the center of half-cycles of the clock. Internally the uPD765 simply registers whether a pulse occurred during a half-cycle or not and the data is separated based on the pattern of pulse-no pulse seen. If a pulse occurred for every half-cycle of the clock, then any of a variety of integrated circuit phase locked loops could be used. Unfortunately they all fail when presented with inputs having "missing" pulses.

Since the goal is to adjust the frequency of the clock so that pulses occur midway in its half-cycles, a phase comparator based on the difference between the actual position of the pulse and its ideal position can be constructed. If a pulse is missing during a half-cycle, the frequency of the clock should be left alone. In order to distinguish ahead of time the difference between a very late pulse and a missing one, the input pulses need to be delayed by 1/2 of the window width. This is accomplished by U64-13 which produces a 1.0uS output for single density tracking and U64-5 which produces a .5uS output for double density frequency tracking. Both pulse widths may be doubled for mini floppy applications by adding C90 and C92.

The timing diagram in section 11 tells better than words how the phase comparator works. Basically, flip-flop U55-7 is turned on by the data pulse if it is early and turned off at the center point of the window. Thus its on-time is proportional to how early the pulse is. If the pulse is late instead, U55-10 instead turns on at the center point and turns off when the pulse actually appears giving a pulse width proportional to how late the pulse was. If there was no pulse at all (single-shot not triggered), then neither flip-flop is turned on and no frequency adjustment is made.

C97 acts as an integrator (type of low-pass filter) for the early and late pulses from the U55 flip-flops. R26 and C87 "shapes" the response of the filter to prevent excessive overshoot when the loop is locking up. When not disturbed (no pulses within the window), it will retain its charge and thus specify a constant frequency from the voltage controlled oscillator. R51 and R25 do however very gradually pull C97 to +2.5 volts and the oscillator to a "center frequency" value when pulses are absent for long periods. If U55-7 momentarily goes low because a pulse arrived early, D6 becomes reverse biased which allows some of the charge on C97 to go to ground through D7 and R23. This causes a slight reduction in voltage on C97 which will speed up the oscillator to counteract the early pulse. Conversely, if U55-10 goes high because of a late pulse, some charge is added to C97 through D8 and R24 which slows down the oscillator.

Q1, R50, Q2, and R48 form a simple unity gain buffer amplifier to match the high impedance level at the base of Q1 to the low impedance level at the control voltage input to the oscillator. The complementary NPN and PNP transistors reduce the input-to-output offset voltage of the amplifier to about 100MV. U56-8, R49, R46, and C95 form a Schmidt trigger oscillator which is made voltage-controlled by the addition of R47. The nominal frequency of the oscillator is 2MHz which can be adjusted with R49. It is important that the other half of U56 only be used in circuitry that is synchronous to the oscillator.

U54 is used as a 1 bit counter followed by a two bit counter. The single/double density signal from the uPD765 selects either the 1MHz output of the first counter for single density or the 2MHz output of the oscillator for double density. This is accomplished with AND-OR-INVERT gate U63-6 which is wired up as a simple 2 input multiplexor. The output of the 2 bit counter is the actual window signal to the disk controller while the B output is used to establish the center point of the window for use by the phase comparator. U63-8 selects either the 1.0uS single-shot output for single-density or the .5uS single shot for double-density. C66, R16, and R17 convert the wide data pulses from the disk drive into very narrow pulses for the disk controller and phase comparator. Since the entire pulse must be within the data window, narrow pulses are preferred for maximum tolerance of pulse position deviation without error.

5.16 POWER SUPPLY

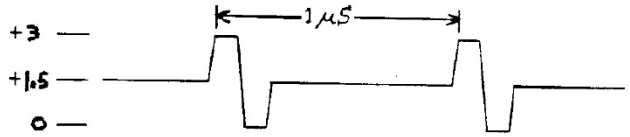
The on-board power supply is at the bottom right corner of schematic page 2. Positive 5 volts for the board logic is derived from the unregulated +8 input by VR2 which is a 1 amp 5 volt IC regulator. C11 prevents oscillation and numerous .05uF bypass capacitors maintain regulation during transient current drains. Positive 12 volts for the memory IC's is provided by VR1. C7 suppresses oscillation and provides additional ripple filtering of the unregulated 16 volt input. C10 absorbs the large current transients typical of dynamic memories. Negative 5 volts for the memory chips is provided by a charge pump circuit consisting of C9, D2, D3, and C8. The circuit is driven from a 12 volt amplitude 1MHz square wave provided by open-collector inverter U60-8 and R6. Shunt regulator D1 limits the negative voltage to -5 volts and in so doing limits the swing at U60-4 to about 6 volts. D1 also prevents the -5 bus from becoming substantially positive during component failure and thus prevents possible damage to the memory chips.

6. ADJUSTMENT PROCEDURE

Four adjustments are provided on the Disk Controller to optimize performance. All are normally made at the factory and the trim pots are sealed with black adhesive tape. If after troubleshooting or replacing components readjustment is required, please read the appropriate sections. An oscilloscope is required to make the adjustments accurately. A 10MHz DC coupled triggered sweep scope is adequate.

6.1 8 MHZ CLOCK (BUS SYNC)

All timing is derived from the 1.0MHz system PHASE 2 clock via a times 8 phase locked frequency multiplier. With the Disk Controller in the system receiving PHASE 2 and powered up, connect the scope to TP13 at the top left corner of the board. One should see a doublet pulse as pictured below with a repetition rate of 1MHz. If an unsynchronized mess is seen or the positive and negative portions of the pulse are not of equal width, rotate R27 until the proper waveform is seen. Double-check the frequency to be certain that the loop has not locked on a subharmonic.



6.2 DATA SEPARATOR SINGLE-SHOTS

To adjust the single-shots, first disconnect the disk drives and jumper U5-10 to pin 46 on the disk cable connector (J1). This is a .25MHz square wave that simulates data pulses from the disk. Next connect the scope to TP16 which should display positive-going pulses approximately 1uS wide and exactly 4uS apart (you may calibrate the scope sweep to the 4uS if needed for maximum accuracy in the pulse width adjustment). Adjust R42 (which has a fairly limited range) until the pulse width is exactly 1.0uS. If capacitors have been added for minifloppy operation, adjust for exactly 2.0uS. To adjust the double-density single-shot, connect the scope to TP12 and adjust R45 for exactly .5uS (1.0uS for minifloppy).

6.3 DATA SEPARATOR VCO ADJUSTMENT

The center frequency of the VCO in the data separator needs to be adjusted to 2MHz for best data recovery reliability. When making this adjustment, there should be no read data pulses coming into the K-1013. If necessary the disk drives should be disconnected. With power on and the scope connected to U54-12, adjust R49 until a 1MHz square wave is seen. The VCO output itself should not be probed during adjustment since the added load capacitance will shift its frequency slightly. If C94 has been added for minifloppy operation, adjust R49 for a .5MHz square wave. After adjustment, double check the DC error voltage at TP17 which should be 2.5 volts. If it is not 2.5 volts or it is varying, verify that pulses are not being received on the $\overline{\text{READ DATA}}$ line.

7. TROUBLESHOOTING

Since all of the MTU-140 system software is loaded from disk when power is applied, disk subsystem faults often result in a system that is not functional. Following are some suggestions of what to look for and try when the CODOS operating system cannot be loaded from disk. These assume that the power-up procedure outlined in the Setup and Installation section of the MTU-140 User Manual has been carefully followed.

7.1 NARROWING TO THE DISK SUBSYSTEM

The first step to take when the system will not load CODOS is to narrow the problem down to the disk subsystem. A good indication that the MTU-140 CPU is working is the appearance of a stable, if somewhat random, image on the video display. If the display fails to show a stable image or any image at all, then the problem is likely to be in the CPU board or power supply. Please refer to the Monomeg CPU Board manual for relevant troubleshooting suggestions.

7.2 DISK DRIVE READY PROBLEMS

If the CPU seems to be coming up but the disk drive select light does not come on and the head does not load, then the Disk Controller is not receiving ready status from the disk drive. Make sure the diskette is inserted properly and that you are not trying to read a double-sided disk in a single-sided drive. Verify that the disk is rotating by removing the disk, manually rotating the disk so that the index hole lines up with the jacket hole, reinserting in the drive momentarily, and checking if the index hole has moved. If the disk is not rotating, make sure the disk drives are receiving power. If you are familiar with disk drive jumpering, you might try swapping the drive select jumpers so that what has been drive 1 is now drive 0. As a final check, obtain an oscilloscope and look at the signal on pin 26 of the disk drive signal cable connector. There should be a pair of negative-going pulses that recur at a 1KHz rate whenever the system is powered up. If they are not seen, the problem is definitely in the disk signal cable or is a Disk Controller board failure.

7.3 DISK READ PROBLEMS

If the activity light comes on and the disk head loads and stays loaded, then the Bootstrap Loader program is unable to read the CODOS operating system from the disk. First try resetting the system several times (be sure to hold the MOD key down until after the disk head loads). If this fails, remove the disk from the drive, reinsert it, and try the reset several more times. Next, try another diskette (you might want to remove the write-permit sticker). If the system has been shipped or subjected to other mechanical shock and vibration since it was used last, then the alignment might have been disturbed which will require an oscilloscope and a special alignment disk to correct. If there are two drives in the cabinet, you can try swapping drive assignments by disassembling the cabinet and swapping the drive select jumpers. If the other drive shows the same symptoms, there could be a problem in the signal cable or the Disk Controller board. With an oscilloscope, look at the signal on pin 46 of the signal cable while the loader is trying to read in CODOS. There should be negative-going pulses approximately 200NS wide and spaced (somewhat erratically) by 2, 3, and 4 microseconds.

PROCESSOR INTERFACE

During Command or Result Phases the Main Status Register (described earlier) must be read by the processor before each byte of information is written into or read from the Data Register. Bits D6 and D7 in the Main Status Register must be in a 0 and 1 state, respectively, before each byte of the command word may be written into the μPD765. Many of the commands require multiple bytes, and as a result the Main Status Register must be read prior to each byte transfer to the μPD765. On the other hand, during the Result Phase, D6 and D7 in the Main Status Register must both be 1's (D6 = 1 and D7 = 1) before reading each byte from the Data Register. Note, this reading of the Main Status Register before each byte transfer to the μPD765 is required in only the Command and Result Phases, and NOT during the Execution Phase.

During the Execution Phase, the Main Status Register need not be read. If the μPD765 is in the NON-DMA Mode, then the receipt of each data byte (if μPD765 is reading data from FDD) is indicated by an Interrupt signal on pin 18 (INT = 1). The generation of a Read signal ($\overline{RD}$ = 0) will reset the Interrupt as well as output the Data onto the Data Bus. If the processor cannot handle Interrupts fast enough (every 13 μs) then it may poll the Main Status Register and then bit D7 (RQM) functions just like the Interrupt signal. If a Write Command is in process then the $\overline{WR}$ signal performs the reset to the Interrupt signal.

If the μPD765 is in the DMA Mode, no Interrupts are generated during the Execution Phase. The μPD765 generates DRQ's (DMA Requests) when each byte of data is available. The DMA Controller responds to this request with both a $\overline{DACK}$ = 0 (DMA Acknowledge) and a $\overline{RD}$ = 0 (Read signal). When the DMA Acknowledge signal goes low ($\overline{DACK}$ = 0) then the DMA Request is reset (DRQ = 0). If a Write Command has been programmed then a $\overline{WR}$ signal will appear instead of $\overline{RD}$. After the Execution Phase has been completed (Terminal Count has occurred) then an Interrupt will occur (INT = 1). This signifies the beginning of the Result Phase. When the first byte of data is read during the Result Phase, the Interrupt is automatically reset (INT = 0).

It is important to note that during the Result Phase all bytes shown in the Command Table must be read. The Read Data Command, for example has seven bytes of data in the Result Phase. All seven bytes must be read in order to successfully complete the Read Data Command. The μPD765 will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the Result Phase.

The μPD765 contains five Status Registers. The Main Status Register mentioned above may be read by the processor at any time. The other four Status Registers (ST0, ST1, ST2, and ST3) are only available during the Result Phase, and may be read only after successfully completing a command. The particular command which has been executed determines how many of the Status Registers will be read.

The bytes of data which are sent to the μPD765 to form the Command Phase, and are read out of the μPD765 in the Result Phase, must occur in the order shown in the Command Table. That is, the Command Code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the Command or Result Phases are allowed. After the last byte of data in the Command Phase is sent to the μPD765, the Execution Phase automatically starts. In a similar fashion, when the last byte of data is read out in the Result Phase, the command is automatically ended and the μPD765 is ready for a new command.

PHASE	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
READ DATA										
Command	W	MT	MF	SK	0	0	1	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and main system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
READ DELETED DATA										
Command	W	MT	MF	SK	0	1	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
WRITE DATA										
Command	W	MT	MF	0	0	0	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the main-system and FDD
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
WRITE DELETED DATA										
Command	W	MT	MF	0	0	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								

PHASE	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
READ A TRACK										
Command	W	0	MF	SK	0	0	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the FDD and main-system. FDC reads all of cylinders contents from index hole to EOT
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
READ ID										
Command	W	0	MF	0	0	1	0	1	0	Commands
	W	X	X	X	X	X	HD	US1	US0	
Execution										The first correct ID information on the Cylinder is stored in Data Register
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information during Execution Phase
	R	H								
	R	R								
	R	N								
FORMAT A TRACK										
Command	W	0	MF	0	0	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	N								Bytes/Sector
	W	SC								Sectors/Track
	W	GPL								Gap 3
	W	D								Filler Byte
Execution										FDC formats an entire cylinder
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								In this case, the ID information has no meaning
	R	H								
	R	R								
	R	N								
SCAN EQUAL										
Command	W	MT	MF	SK	1	0	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data-compared between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								

Note ① Symbols used in this table are described at the end of this section.

② A_0 should equal binary 1 for all operations.

③ X = Don't care, usually made to equal binary 0.

PHASE	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
SCAN LOW OR EQUAL										
Command	W	MT	MF	SK	1	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data-compared between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
SCAN HIGH OR EQUAL										
Command	W	MT	MF	SK	1	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data-compared between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								

PHASE	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
RECALIBRATE										
Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	X	X	X	X	X	0	US1	US0	
Execution										Head retracted to Track 0
SENSE INTERRUPT STATUS										
Command	W	0	0	0	0	1	0	0	0	Command Codes
Result	R	STO								Status information at the end of seek-operation about the FDC
	R	PCN								
SPECIFY										
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W	SRT						HUT		
	W	HLT						ND		
SENSE DRIVE STATUS										
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
Result	R	ST 3								Status information about FDD
SEEK										
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	NCN								
Execution										Head is positioned over proper Cylinder on Diskette
INVALID										
Command	W	Invalid Codes								Invalid Command Codes (NoOp – FDC goes into Standby State)
Result	R	ST 0								ST 0 = 80 (16)

COMMAND SYMBOL DESCRIPTION

SYMBOL	NAME	DESCRIPTION
A_0	Address Line 0	A_0 controls selection of Main Status Register (A_0 = 0) or Data Register (A_0 = 1)
C	Cylinder Number	C stands for the current-selected Cylinder (track) number 0 through 76 of the medium
D	Data	D stands for the data pattern which is going to be written into a Sector
D_7 D_0	Data Bus	8 bit Data Bus, where D_7 stands for a most significant bit, and D_0 stands for a least significant bit
DTL	Data Length	When N is defined as 00, DTL stands for the data length which users are going to read out or write into the Sector
EOT	End of Track	EOT stands for the final Sector number on a Cylinder
GPL	Gap Length	GPL stands for the length of Gap 3 (spacing between Sectors excluding VCO Sync. Field)
H	Head Address	H stands for head number 0 or 1, as specified in ID field
HD	Head	HD stands for a selected head number 0 or 1. (H = HD in all command words.)
HLT	Head Load Time	HLT stands for the head load time in the FDD (2 to 256 ms in 2 ms increments)
HUT	Head Unload Time	HUT stands for the head unload time after a read or write operation has occurred (0 to 240 ms in 16 ms increments)
MF	FM or MFM Mode	If MF is low, FM mode is selected, and if it is high, MFM mode is selected.
MT	Multi-Track	If MT is high, a multi-track operation is to be performed. (A cylinder under both HD0 and HD1 will be read or written.)

COMMAND SYMBOL DESCRIPTION (CONT.)

SYMBOL	NAME	DESCRIPTION
N	Number	N stands for the number of data bytes written in a Sector.
NCN	New Cylinder Number	NCN stands for a new Cylinder number, which is going to be reached as a result of the Seek operation. Desired position of Head.
ND	Non-DMA Mode	ND stands for operation in the Non-DMA Mode.
PCN	Present Cylinder Number	PCN stands for the Cylinder number at the completion of SENSE INTERRUPT STATUS Command. Position of Head at present time.
R	Record	R stands for the Sector number, which will be read or written.
R/W	Read/Write	R/W stands for either Read (R) or Write (W) signal.
SC	Sector	SC indicates the number of Sectors per Cylinder.
SK	Skip	SK stands for Skip Deleted Data Address Mark.
SRT	Step Rate Time	SRT stands for the Stepping Rate for the FDD. (1 to 16 ms in 1 ms increments.) Must be defined for each of the four drives.
ST 0 ST 1 ST 2 ST 3	Status 0 Status 1 Status 2 Status 3	ST 0-3 stand for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by A_0 = 0). ST 0-3 may be read only after a command has been executed and contain information relevant to that particular command.
STP		During a Scan operation, if STP = 1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA), and if STP = 2, then alternate sectors are read and compared.
US0, US1	Unit Select	US stands for a selected drive number 0 or 1.

The bits in the Main Status Register are defined as follows:

BIT NUMBER	NAME	SYMBOL	DESCRIPTION
DB_0	FDD 0 Busy	D_0B	FDD number 0 is in the Seek mode.
DB_1	FDD 1 Busy	D_1B	FDD number 1 is in the Seek mode.
DB_2	FDD 2 Busy	D_2B	FDD number 2 is in the Seek mode.
DB_3	FDD 3 Busy	D_3B	FDD number 3 is in the Seek mode.
DB_4	FDC Busy	CB	A read or write command is in process.
DB_5	Non-DMA mode	NDM	The FDC is in the non-DMA mode.
DB_6	Data Input/Output	DIO	Indicates direction of data transfer between FDC and Data Register. If DIO = "1" then transfer is from Data Register to the Processor. If DIO = "0", then transfer is from the Processor to Data Register.
DB_7	Request for Master	RQM	Indicates Data Register is ready to send or receive data to or from the Processor. Both bits DIO and RQM should be used to perform the hand-shaking functions of "ready" and "direction" to the processor.

The DIO and RQM bits in the Status Register indicate when Data is ready and in which direction data will be transferred on the Data Bus.

STATUS REGISTER IDENTIFICATION

BIT NO.	BIT NAME	BIT SYMBOL	DESCRIPTION
STATUS REGISTER 0			
D_7	Interrupt Code	IC	$D_7 = 0$ and $D_6 = 0$ Normal Termination of Command, (NT). Command was completed and properly executed.
D_6			$D_7 = 0$ and $D_6 = 1$ Abnormal Termination of Command, (AT). Execution of Command was started, but was not successfully completed.
			$D_7 = 1$ and $D_6 = 0$ Invalid Command issue, (IC). Command which was issued was never started.
			$D_7 = 1$ and $D_6 = 1$ Abnormal Termination because during command execution the ready signal from FDD changed state.
D_5	Seek End	SE	When the FDC completes the SEEK Command, this flag is set to 1 (high).
D_4	Equipment Check	EC	If a fault Signal is received from the FDD, or if the Track 0 Signal fails to occur after 77 Step Pulses (Recalibrate Command) then this flag is set.
D_3	Not Ready	NR	When the FDD is in the not-ready state and a read or write command is issued, this flag is set. If a read or write command is issued to Side 1 of a single sided drive, then this flag is set.
D_2	Head Address	HD	This flag is used to indicate the state of the head at Interrupt.
D_1	Unit Select 1	US 1	These flags are used to indicate a Drive Unit Number at Interrupt
D_0	Unit Select 0	US 0	
STATUS REGISTER 1			
D_7	End of Cylinder	EN	When the FDC tries to access a Sector beyond the final Sector of a Cylinder, this flag is set.
D_6			Not used. This bit is always 0 (low).
D_5	Data Error	DE	When the FDC detects a CRC error in either the ID field or the data field, this flag is set.
D_4	Over Run	OR	If the FDC is not serviced by the main-systems during data transfers, within a certain time interval, this flag is set.
D_3			Not used. This bit always 0 (low).
D_2	No Data	ND	During execution of READ DATA, WRITE DELETED DATA or SCAN Command, if the FDC cannot find the Sector specified in the IDR Register, this flag is set.
			During executing the READ ID Command, if the FDC cannot read the ID field without an error, then this flag is set.
			During the execution of the READ A Cylinder Command, if the starting sector cannot be found, then this flag is set.

STATUS REGISTER IDENTIFICATION (CONT.)

BIT NO.	BIT NAME	BIT SYMBOL	DESCRIPTION
STATUS REGISTER 1 (CONT.)			
D_1	Not Writable	NW	During execution of WRITE DATA, WRITE DELETED DATA or Format A Cylinder Command, if the FDC detects a write protect signal from the FDD, then this flag is set.
D_0	Missing Address Mark	MA	If the FDC cannot detect the ID Address Mark after encountering the index hole twice, then this flag is set.
			If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. Also at the same time, the MD (Missing Address Mark in Data Field) of Status Register 2 is set.
STATUS REGISTER 2			
D_7			Not used. This bit is always 0 (low).
D_6	Control Mark	CM	During executing the READ DATA or SCAN Command, if the FDC encounters a Sector which contains a Deleted Data Address-Mark, this flag is set.
D_5	Data Error in Data Field	DD	If the FDC detects a CRC error in the data field then this flag is set.
D_4	Wrong Cylinder	WC	This bit is related with the ND bit, and when the contents of C on the medium is different from that stored in the IDR, this flag is set.
D_3	Scan Equal Hit	SH	During execution, the SCAN Command, if the condition of "equal" is satisfied, this flag is set.
D_2	Scan Not Satisfied	SN	During executing the SCAN Command, if the FDC cannot find a Sector on the cylinder which meets the condition, then this flag is set.
D_1	Bad Cylinder	BC	This bit is related with the ND bit, and when the content of C on the medium is different from that stored in the IDR and the content of C is FF, then this flag is set.
D_0	Missing Address Mark in Data Field	MD	When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set.
STATUS REGISTER 3			
D_7	Fault	FT	This bit is used to indicate the status of the Fault signal from the FDD.
D_6	Write Protected	WP	This bit is used to indicate the status of the Write Protected signal from the FDD.
D_5	Ready	RY	This bit is used to indicate the status of the Ready signal from the FDD.
D_4	Track 0	T0	This bit is used to indicate the status of the Track 0 signal from the FDD.
D_3	Two Side	TS	This bit is used to indicate the status of the Two Side signal from the FDD.
D_2	Head Address	HD	This bit is used to indicate the status of Side Select signal to the FDD.
D_1	Unit Select 1	US 1	This bit is used to indicate the status of the Unit Select 1 signal to the FDD.
D_0	Unit Select 0	US 0	This bit is used to indicate the status of the Unit Select 0 signal to the FDD.

READ DATA

A set of nine (9) byte words are required to place the FDC into the Read Data Mode. After the Read Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify Command), and begins reading ID Address Marks and ID fields. When the current sector number ("R") stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC outputs data (from the data field) byte-to-byte to the main system via the data bus.

After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a "Multi-Sector Read Operation." The Read Data Command may be terminated by the receipt of a Terminal Count signal. Upon receipt of this signal, the FDC stops outputting data to the processor, but will continue to read data from the current sector, check CRC (Cyclic Redundancy Count) bytes, and then at the end of the sector terminate the Read Data Command.

The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track), MF (MFM/FM), and N (Number of Bytes/Sector). Table 1 below shows the Transfer Capacity.

Multi-Track MT	MFM/FM MF	Bytes/Sector N	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Diskette
0	0	00	(128) (26) = 3,328	26 at Side 0
0	1	01	(256) (26) = 6,656	or 26 at Side 1
1	0	00	(128) (52) = 6,656	26 at Side 1
1	1	01	(256) (52) = 13,312	
0	0	01	(256) (15) = 3,840	15 at Side 0
0	1	02	(512) (15) = 7,680	or 15 at Side 1
1	0	01	(256) (30) = 7,680	15 at Side 1
1	1	02	(512) (30) = 15,360	
0	0	02	(512) (8) = 4,096	8 at Side 0
0	1	03	(1024) (8) = 8,192	or 8 at Side 1
1	0	02	(512) (16) = 8,192	8 at Side 1
1	1	03	(1024) (16) = 16,384	

Table 1. Transfer Capacity

The "multi-track" function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 0, Side 0 and completing at Sector L, Side 1 (Sector L = last sector on the side). Note, this function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, then DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a Sector, the data beyond DTL in the Sector, is not sent to the Data Bus. The FDC reads (internally) the complete Sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read Operation. When N is non-zero, then DTL has no meaning and should be set to FF Hexidecimal.

At the completion of the Read Data Command, the head is not unloaded until after Head Unload Time Interval (specified in the Specify Command) has elapsed. If the processor issues another command before the head unloads then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another.

If the FDC detects the Index Hole twice without finding the right sector, (indicated in "R"), then the FDC sets the ND (No Data) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC sets the DE (Data Error) flag in Status Register 1 to a 1 (high), and if a CRC error occurs in the Data Field the FDC also sets the DD (Data Error in Data Field) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

Status Register 2 to a 1 (high), and terminates the Read Data Command.

If the FDC reads a Deleted Data Address Mark off the diskette, and the SK bit (bit D5 in the first Command Word) is not set (SK = 0), then the FDC sets the DM (Control Mark) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command, after reading all the data in the Sector. If SK = 1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector.

During disk data transfers between the FDC and the processor, via the data bus, the FDC must be serviced by the processor every 27 μs in the FM Mode, and every 13 μs in the MFM Mode, or the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command.

If the processor terminates a read (or write) operation in the FDC, then the ID Information in the Result Phase is dependent upon the state of the MT bit and EOT byte. Table 2 shows the values for C, H, R, and N, when the processor terminates the Command.

FUNCTIONAL DESCRIPTION OF COMMANDS (CONT.)

MT	EOT	Final Sector Transferred to Processor	ID Information at Result Phase			
			C	H	R	N
0	1A	Sector 1 to 25 at Side 0	NC	NC	R + 1	NC
	0F	Sector 1 to 14 at Side 0				
	08	Sector 1 to 7 at Side 0				
	1A	Sector 26 at Side 0	C + 1	NC	R = 01	NC
	0F	Sector 15 at Side 0				
	08	Sector 8 at Side 0				
	1A	Sector 1 to 25 at Side 1	NC	NC	R + 1	NC
	0F	Sector 1 to 14 at Side 1				
	08	Sector 1 to 7 at Side 1				
	1A	Sector 26 at Side 1	C + 1	NC	R = 01	NC
	0F	Sector 15 at Side 1				
	08	Sector 8 at Side 1				
1	1A	Sector 1 to 25 at Side 0	NC	NC	R + 1	NC
	0F	Sector 1 to 14 at Side 0				
	08	Sector 1 to 7 at Side 0				
	1A	Sector 26 at Side 0	NC	LSB	R = 01	NC
	0F	Sector 15 at Side 0				
	08	Sector 8 at Side 0				
	1A	Sector 1 to 25 at Side 1	NC	NC	R + 1	NC
	0F	Sector 1 to 14 at Side 1				
	08	Sector 1 to 7 at Side 1				
	1A	Sector 26 at Side 1	C + 1	LSB	R = 01	NC
	0F	Sector 15 at Side 1				
	08	Sector 8 at Side 1				

Notes: 1 NC (No Change): The same value as the one at the beginning of command execution.

2 LSB (Least Significant Bit): The least significant bit of H is complemented.

Table 2: ID Information When Processor Terminates Command

WRITE DATA

A set of nine (9) bytes are required to set the FDC into the Write Data mode. After the Write Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify Command), and begins reading ID Fields. When the current sector number ("R"), stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC takes data from the processor byte-by-byte via the data bus, and outputs it to the FDD.

After writing data into the current sector, the Sector Number stored in "R" is incremented by one, and the next data field is written into. The FDC continues this "Multi-Sector Write Operation" until the issuance of a Terminal Count signal. If a Terminal Count signal is sent to the FDC it continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written then the remainder of the data field is filled with 00 (zeros).

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (incorrect CRC) in one of the ID Fields, it sets the DE (Data Error) flag of Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

The Write Command operates in much the same manner as the Read Command. The following items are the same, and one should refer to the Read Data Command for details:

- Transfer Capacity
- EN (End of Cylinder) Flag
- ND (No Data) Flag
- Head Unload Time Interval
- ID Information when the processor terminates command (see Table 2)
- Definition of DTL when N = 0 and when N ≠ 0

In the Write Data mode, data transfers between the processor and FDC, via the Data Bus, must occur every 31 μs in the FM mode, and every 15 μs in the MFM mode. If the time interval between data transfers is longer than this then the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 0 also has bit 7 and 6 set to 0 and 1 respectively.)

WRITE DELETED DATA

This command is the same as the Write Data Command except a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark.

READ DELETED DATA

This command is the same as the Read Data Command except that when the FDC detects a Data Address Mark at the beginning of a Data Field (and SK = 0 (low), it will read all the data in the sector and set the MD flag in Status Register 2 to a 1 (high), and then terminate the command. If SK = 1, then the FDC skips the sector with the Data Address Mark and reads the next sector.

READ A TRACK

This command is similar to READ DATA Command except that this is a continuous READ operation where the entire contents of the track are read. Immediately after encountering the INDEX HOLE, the FDC starts reading all data on the track, Gap bytes, Address Marks and Data are all read as a continuous data stream. If the FDC finds an error in the ID or DATA CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR, and sets the ND flag of Status Register 1 to a 1 (high) if there is no comparison. Multi-track or skip operations are not allowed with this command.

This command terminates when EOT number of sectors have been read ($EOT_{max} = FF_{hex} = 255_{dec}$). If the FDC does not find an ID Address Mark on the diskette after it encounters the INDEX HOLE for the second time, then it sets the MA (missing address mask) flag in Status Register 1 to a 1 (high), and terminates the command. (Status Register 0 has bits 7 and 6 set to 0 and 1 respectively).

READ ID

The READ ID Command is used to give the present position of the recording head. The FDC stores the values from the first ID Field it is able to read. If no proper ID Address Mark is found on the diskette, before the INDEX HOLE is encountered for the second time then the MA (Missing Address Mark) flag in Status Register 1 is set to a 1 (high), and if no data is found then the ND (No Data) flag is also set in Status Register 1 to a 1 (high). The command is then terminated with Bits 7 and 6 in Status Register 0 set to 0 and 1 respectively.

FORMAT A TRACK

The Format Command allows an entire track to be formatted. After the INDEX HOLE is detected, Data is written on the Diskette; Gaps, Address Marks, ID Fields and Data Fields, all per the IBM System 34 (Double Density) or System 3740 (Single Density) Format are recorded. The particular format which will be written is controlled by the values programmed into N (number of bytes/sector), SC (sectors/cylinder), GPL (Gap Length), and D (Data Pattern) which are supplied by the processor during the Command Phase. The Data Field is filled with the Byte of data stored in D. The ID Field for each sector is supplied by the processor; that is, four data requests per sector are made by the FDC for C (Cylinder Number), H (Head Number), R (Sector Number) and N (Number of Bytes/Sector). This allows the diskette to be formatted with non-sequential sector numbers, if desired.

After formatting each sector, the processor must send new values for C, H, R, and N to the μPD765 for each sector on the track. The contents of the R register is incremented by one after each sector is formatted, thus, the R register contains a value of R + 1 when it is read during the Result Phase. This incrementing and formatting continues for the whole cylinder until the FDC encounters the INDEX HOLE for the second time, whereupon it terminates the command.

If a FAULT signal is received from the FDD at the end of a write operation, then the FDC sets the EC flag of Status Register 0 to a 1 (high), and terminates the command after setting bits 7 and 6 of Status Register 0 to 0 and 1 respectively. Also the loss of a READY signal at the beginning of a command execution phase causes bits 7 and 6 of Status Register 0 to be set to 0 and 1 respecitvely.

Table 3 shows the relationship between N, SC, and GPL for various sector sizes:

FORMAT	SECTOR SIZE	N	SC	GPL ①	GPL ②	REMARKS
FM Mode	128 bytes/Sector	00	$1A_{(16)}$	$07_{(16)}$	$1B_{(16)}$	IBM Diskette 1
	256	01	$0F_{(16)}$	$0E_{(16)}$	$2A_{(16)}$	IBM Diskette 2
	512	02	08	$1B_{(16)}$	$3A_{(16)}$	
FM Mode	1024 bytes/Sector	03	04	–	–	
	2048	04	02	–	–	
	4096	05	01	–	–	
MFM Mode	256	01	$1A_{(16)}$	$0E_{(16)}$	$36_{(16)}$	IBM Diskette 2D
	512	02	$0F_{(16)}$	$1B_{(16)}$	$54_{(16)}$	
	1024	03	08	$35_{(16)}$	$74_{(16)}$	IBM Diskette 2D
	2048	04	04	–	–	
	4096	05	02	–	–	
	8192	06	01	–	–	

Table 3

Note: ① Suggested values of GPL in Read or Write Commands to avoid splice point between data field and ID field of contiguous sections.

② Suggested values of GPL in format command.

FUNCTIONAL DESCRIPTION OF COMMANDS (CONT.)

SCAN COMMANDS

The SCAN Commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system (Processor in NON-DMA mode, and DMA Controller in DMA mode). The FDC compares the data on a byte-by-byte basis, and looks for a sector of data which meets the conditions of $D_{FDD} = D_{Processor}$, $D_{FDD} \leq D_{Processor}$, or $D_{FDD} \geq D_{Processor}$. Ones complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremented (R + STP → R), and the scan operation is continued. The scan operation continues until one of the following conditions occur, the conditions for scan are met (equal, low, or high), the last sector on the track is reached (EOT), or the terminal count signal is received.

If the conditions for scan are met then the FDC sets the SH (Scan Hit) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (Scan Not Satisfied) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. The receipt of a TERMINAL COUNT signal from the Processor or DMA Controller during the scan operation will cause the FDC to complete the comparison of the particular byte which is in process, and then to terminate the command. Table 4 shows the status of bits SH and SN under various conditions of SCAN.

COMMAND	STATUS REGISTER 2		COMMENTS
	BIT 2 = SN	BIT 3 = SH	
Scan Equal	0	1	$D_{FDD} = D_{Processor}$
	1	0	$D_{FDD} \neq D_{Processor}$
Scan Low or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} < D_{Processor}$
	1	0	$D_{FDD} \neq D_{Processor}$
Scan High or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} < D_{Processor}$
	1	0	$D_{FDD} \geq D_{Processor}$

Table 4

If the FDC encounters a Deleted Data Address Mark on one of the sectors (and SK = 0), then it regards the sector as the last sector on the cylinder, sets CM (Control Mark) flag of Status Register 2 to a 1 (high) and terminates the command. If SK = 1, the FDC skips the sector with the Deleted Address Mark, and reads the next sector. In the second case (SK = 1), the FDC sets the CM (Control Mark) flag of Status Register 2 to a 1 (high) in order to show that a Deleted Sector had been encountered.

When either the STP (contiguous sectors = 01, or alternate sectors = 02 sectors are read) or the MT (Multi-Track) are programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26, and we start the Scan Command at sector 21; the following will happen. Sectors 21, 23, and 25 will be read, then the next sector (26) will be skipped and the Index Hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the Scan Command would be completed in a normal manner.

During the Scan Command data is supplied by either the processor or DMA Controller for comparison against the data read from the diskette. In order to avoid having the OR (Over Run) flag set in Status Register 1, it is necessary to have the data available in less than 27 μs (FM Mode) or 13 μs (MFM Mode). If an Overrun occurs the FDC ends the command with bits 7 and 6 of Status Register 0 set to 0 and 1, respectively.

SEEK

The read/write head within the FDD is moved from cylinder to cylinder under control of the Seek Command. The FDC compares the PCN (Present Cylinder Number) which is the current head position with the NCN (New Cylinder Number), and if there is a difference performs the following operation:

PCN < NCN: Direction signal to FDD set to a 1 (high), and Step Pulses are issued. (Step In.)
PCN > NCN: Direction signal to FDD set to a 0 (low), and Step Pulses are issued. (Step Out.)

The rate at which Step Pulses are issued is controlled by SRT (Stepping Rate Time) in the SPECIFY Command. After each Step Pulse is issued NCN is compared against PCN, and when NCN = PCN, then the SE (Seek End) flag is set in Status Register 0 to a 1 (high), and the command is terminated.

During the Command Phase of the Seek operation the FDC is in the FDC BUSY state, but during the Execution Phase it is in the NON BUSY state. While the FDC is in the NON BUSY state, another Seek Command may be issued, and in this manner parallel seek operations may be done on up to 4 Drives at once.

If an FDD is in a NOT READY state at the beginning of the command execution phase or during the seek operation, then the NR (NOT READY) flag is set in Status Register 0 to a 1 (high), and the command is terminated after bits 7 and 6 of Status Register 0 are set to 0 and 1 respectively.

RECALIBRATE

The function of this command is to retract the read/write head within the FDD to the Track 0 position. The FDC clears the contents of the PCN counter, and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal is low, the Direction signal remains 1 (high) and Step Pulses are issued. When the Track 0 signal goes high, the SE (SEEK END) flag in Status Register 0 is set to a 1 (high) and the command is terminated. If the Track 0 signal is still low after 77 Step Pulse have been issued, the FDC sets the SE (SEEK END) and EC (EQUIPMENT CHECK) flags of Status Register 0 to both 1s (highs), and terminates the command after bits 7 and 6 of Status Register 0 is set to 0 and 1 respectively.

The ability to do overlap RECALIBRATE Commands to multiple FDDs and the loss of the READY signal, as described in the SEEK Command, also applies to the RECALIBRATE Command.

SENSE INTERRUPT STATUS

An Interrupt signal is generated by the FDC for one of the following reasons:

1. Upon entering the Result Phase of:
   a. Read Data Command
   b. Read a Track Command
   c. Read ID Command
   d. Read Deleted Data Command
   e. Write Data Command
   f. Format a Cylinder Command
   g. Write Deleted Data Command
   h. Scan Commands
2. Ready Line of FDD changes state
3. End of Seek or Recalibrate Command
4. During Execution Phase in the NON-DMA Mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. However, interrupts caused by reasons 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt Status Command. This command when issued resets the interrupt signal and via bits 5, 6, and 7 of Status Register 0 identifies the cause of the interrupt.

SEEK END	INTERRUPT CODE		CAUSE
BIT 5	BIT 6	BIT 7	
0	1	1	Ready Line changed state, either polarity
1	0	0	Normal Termination of Seek or Recalibrate Command
1	1	0	Abnormal Termination of Seek or Recalibrate Command

Table 5

Neither the Seek or Recalibrate Command have a Result Phase. Therefore, it is mandatory to use the Sense Interrupt Status Command after these commands to effectively terminate them and to provide verification of where the head is positioned (PCN).

SPECIFY

The Specify Command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the Execution Phase of one of the Read/Write Commands to the head unload state. This timer is programmable from 0 to 240 ms in increments of 16 ms (00 = 0 ms, 01 = 16 ms, 02 = 32 ms, etc.). The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms, etc.). The HLT (Head Load Time) defines the time between when the Head Load signal goes high and when the Read/Write operation starts. This timer is programmable from 2 to 256 ms in increments of 2 ms (00 = 2 ms, 01 = 4 ms, 02 = 6 ms, etc.).

The time intervals mentioned above are a direct function of the clock (CLK on pin 19). Times indicated above are for an 8 MHz clock, if the clock was reduced to 4 MHz (mini-floppy application) then all time intervals are increased by a factor of 2.

The choice of DMA or NON-DMA operation is made by the ND (NON-DMA) bit. When this bit is high (ND = 1) the NON-DMA mode is selected, and when ND = 0 the DMA mode is selected.

SENSE DRIVE STATUS

This command may be used by the processor whenever it wishes to obtain the status of the FDDs. Status Register 3 contains the Drive Status information.

INVALID

If an invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command after bits 7 and 6 of Status Register 0 are set to 1 and 0 respectively. A Sense Interrupt Status Command must be sent after a Seek or Recalibrate Interrupt, otherwise the FDC will consider the next command to be an Invalid Command.

In some applications the user may wish to use this command as a No-Op command, to place the FDC in a standby or no operation state.

9. SPECIFICATIONS

PHYSICAL: 7 1/2" high by 11" wide exclusive of edge fingers; fits the K-1005 series of card files.

POWER REQUIREMENT: +8 volts unregulated 600MA, +16 volts unregulated 125MA.

BUFFERING: Maximum of 1 LS TTL load on address and data bus lines.

LSI CHIPS USED: uPD765 disk controller, 4116 dynamic RAM 200NS access time.

SYSTEM CLOCK FREQUENCY: Phase 2 clock frequency must be 1.0MHz crystal controlled as provided by the MTU-130 Computer.

DISK DRIVE INTERFACE: Shugart 8 inch SA800 compatible drives may be used directly. Others accomodated by adapter board and cable change.

ON BOARD MEMORY: 2 independent 8K blocks of RAM, 256 bytes bipolar PROM.

DATA TRANSFER METHOD: Direct access into on-board memory.

WAIT STATES: None under any condition. DMA transfers and memory refresh performed during phase 1 of the system clock. (6502 accesses only during phase 2.

ADDRESSING: Each 8K block of memory may be independently addressed on any 4K boundary. PROM and I/O registers are part of one 8K block.

DATA SEPARATOR: True analog phase-locked loop, no quantizing error.

ADJUSTMENTS: 4, Master clock sync, data separator oscillator, standard density pulse width, double density pulse width.

10. PIN CONNECTIONS

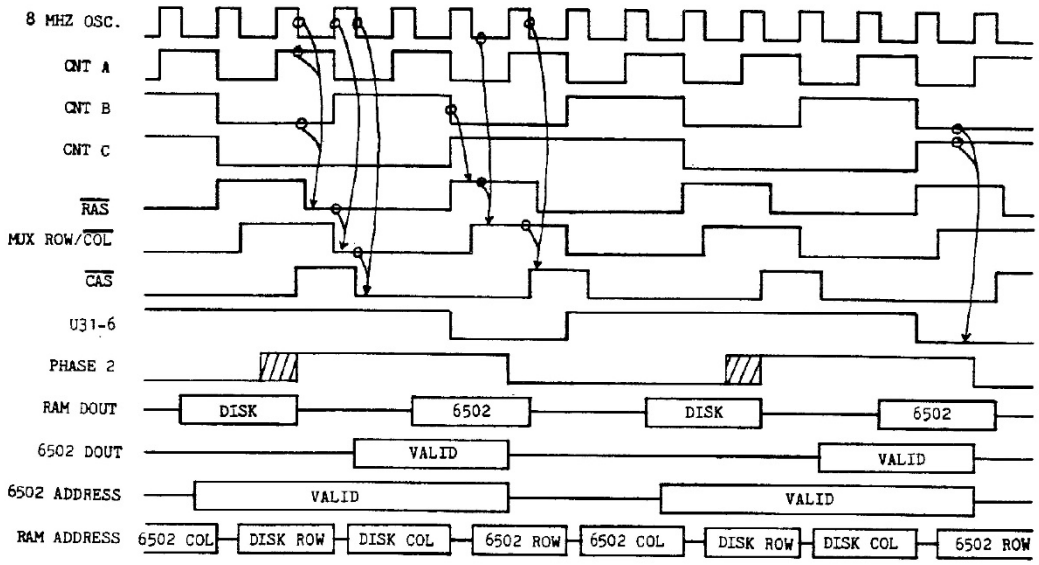
MTU-140 BUS CONNECTOR	SIGNAL
1	N. C.
2	ADDRESS BUS 16
3	ADDRESS BUS 17
4	IRQ
5	N. C.
6	N. C.
7	RESET
8	DATA BUS BIT 7
9	DATA BUS BIT 6
10	DATA BUS BIT 5
11	DATA BUS BIT 4
12	DATA BUS BIT 3
13	DATA BUS BIT 2
14	DATA BUS BIT 1
15	DATA BUS BIT 0
16	N. C.
17	N. C.
18	+8 VOLTS UNREG
19	VECTOR FETCH
20	DECODE ENABLE
21	N. C.
22	GROUND

MTU-140 BUS CONNECTOR	SIGNAL
A	ADDRESS BUS 0
B	ADDRESS BUS 1
C	ADDRESS BUS 2
D	ADDRESS BUS 3
E	ADDRESS BUS 4
F	ADDRESS BUS 5
H	ADDRESS BUS 6
J	ADDRESS BUS 7
K	ADDRESS BUS 8
L	ADDRESS BUS 9
M	ADDRESS BUS 10
N	ADDRESS BUS 11
P	ADDRESS BUS 12
R	ADDRESS BUS 13
S	ADDRESS BUS 14
T	ADDRESS BUS 15
U	PHASE 2
V	READ/WRITE
W	N. C.
X	+16 VOLTS UNREG
Y	N. C.
Z	N. C.

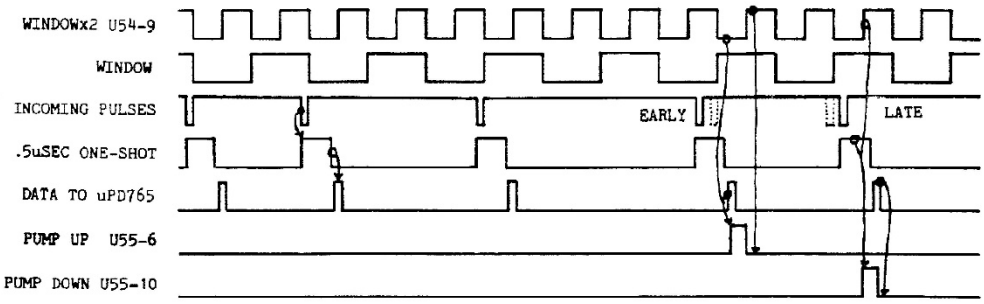
DISK DRIVE CONNECTOR	SIGNAL
1	GROUND
2	LOW WRITE CURRENT
3	GROUND
4	N. C.
5	GROUND
6	N. C.
7	GROUND
8	N. C.
9	GROUND
10	2-SIDED SENSE (2-side only)
11	GROUND
12	N. C.
13	GROUND
14	HEAD SELECT (2-side only)
15	GROUND
16	N. C.
17	GROUND
18	HEAD LOAD
19	GROUND
20	INDEX
21	GROUND
22	READY
23	GROUND
24	N. C.
25	GROUND

DISK DRIVE CONNECTOR	SIGNAL
26	DRIVE SELECT 0
27	GROUND
28	DRIVE SELECT 1
29	GROUND
30	DRIVE SELECT 2
31	GROUND
32	DRIVE SELECT 3
33	GROUND
34	STEP DIRECTION=IN
35	GROUND
36	STEP
37	GROUND
38	WRITE DATA
39	GROUND
40	WRITE ENABLE
41	GROUND
42	TRACK 0
43	GROUND
44	WRITE PROTECT
45	GROUND
46	RAW READ DATA
47	GROUND
48	N. C.
49	GROUND
50	N. C.

11. TIMING DIAGRAMS



MEMORY CYCLE TIMING DIAGRAM



DATA SEPARATOR TIMING DIAGRAM

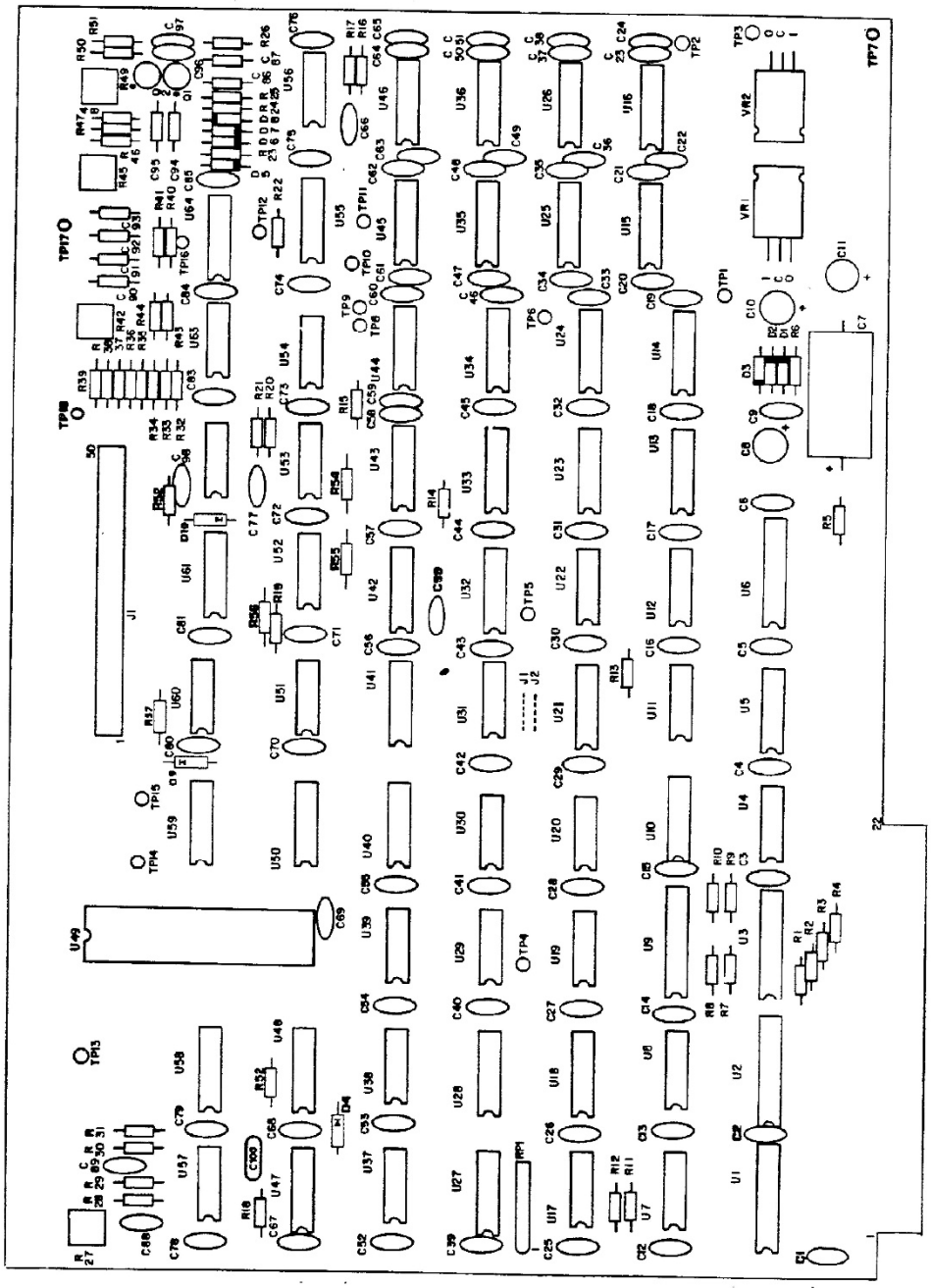
12. PARTS LIST

QTY	PART TYPE	DESIGNATION
3	LOGIC, 74LS00	U31,39,52
5	LOGIC, 74LS04	U4,19,37,51,53
1	LOGIC, 7406	U60
1	LOGIC, 74LS08	U62
3	LOGIC, 74LS10	U20,29,38
2	LOGIC, 74LS13	U56,57
2	LOGIC, 74LS20	U11,30
3	LOGIC, 74LS30	U7,8,17
1	LOGIC, 74LS42	U40
1	LOGIC, 74LS51	U63
1	LOGIC, 74LS93	U54
4	LOGIC, 74LS109	U5,32,42,55
1	LOGIC, 74145	U61
5	LOGIC, 74LS153	U14,24,34,44,58
2	LOGIC, 74LS157	U13,23
3	LOGIC, 74LS161	U21,33,43
1	LOGIC, 74LS173	U48
1	LOGIC, 74LS175	U10
1	LOGIC, 74LS221	U64
2	LOGIC, 74LS283	U18,28
2	LOGIC, 74LS368	U50,59
2	LOGIC, 74LS393	U12,22
4	LOGIC, 81LS95	U1-3,9
8	MEMORY, 4116 TYPE 200ns	U15,16,25,26,35,36,45,46
1	MEMORY, 256X8 PROM	U6
1	LSI FD CONTR UPD765	U49
24	SOCKET, PC 14 PIN	U4,7,8,11,12,17,19,20,22,29-31, 37-39,51-54,56,57,60,62,63
35	SOCKET, PC 16 PIN	U5,10,13-16,18,21,23-28,32-36, 40-48,50,55,58,59,61,64
5	SOCKET, PC 20 PIN	U1-3,6,9
1	SOCKET, PC 40 PIN	U49
1	DIODE, GERMANIUM 1N270	D4
8	DIODE, SILICON 1N4148	D2,3,5-10
1	DIODE, ZENER 5.1V .4W	D1
1	TRANSISTOR, NPN PN2222	Q2
1	TRANSISTOR, PNP PN2907	Q1
1	VOLT REG. +5V LM340T-5	VR2
1	VOLT REG. +12V LM341P-12	VR1

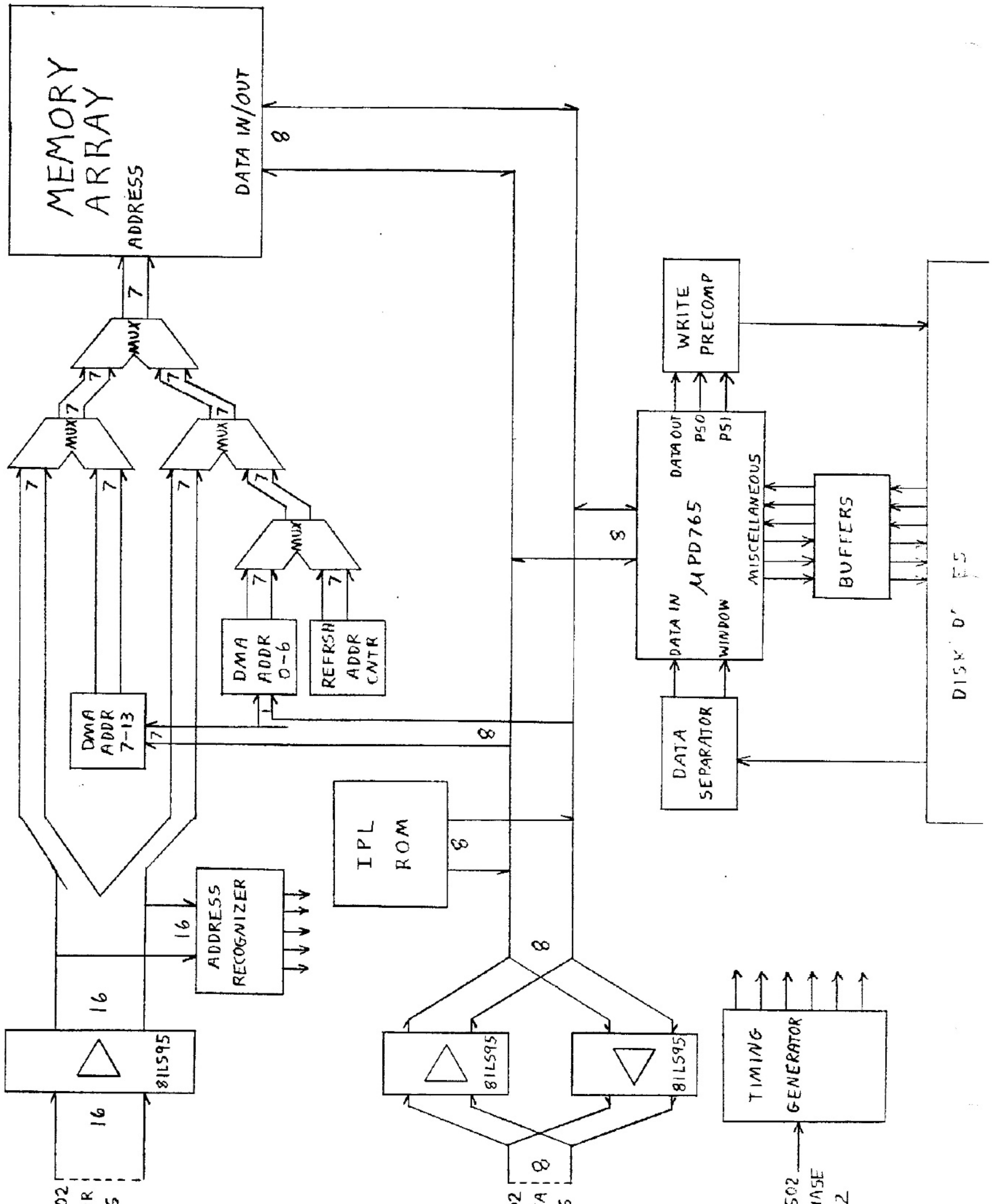
QTY	PART TYPE	DESIGNATION
1	RES, 1/4W 5% 10 OHM	R29
5	RES, 1/4W 5% 220 OHM	R32,34,36,38,41
9	RES, 1/4W 5% 270 OHM	R1-4,7-10,46
6	RES, 1/4W 5% 330 OHM	R33,35,37,39,40,52
4	RES, 1/4W 5% 470 OHM	R15,28,31,53
4	RES, 1/4W 5% 1K	R6,19,26,56
1	RES, 1/4W 5% 1.5K	R44
7	RES, 1/4W 5% 2.2K	R16,17,20,30,47,48,54
1	RES, 1/4W 5% 3K	R43
2	RES, 1/4W 5% 3.3K	R21,55
2	RES, 1/4W 5% 4.7K	R23,24
8	RES, 1/4W 5% 10K	R5,11-14,18,22,57
1	RES, 1/4W 5% 51K	R50
2	RES, 1/4W 5% 820K	R25,51
1	RES, PACK 5% 10K 8	RP1
4	TRIMPOT, 500 OHM SQ	R27,42,45,49
3	CAP,ELECT 100UF 16V RA	C8,10,11
1	CAP,ELECT 1000UF 25V AX	C7
3	CAP,POLY,470PF 12V	C91,93,95
1	CAP,POLY,1000PF 12V	C87
4	CAP,DISK,NPO 68PF 12V	C66,88,98,99
3	CAP,DISK,Y5F 100PF 12V	C58,77,100
3	CAP,DISK,Z5U .01UF 12V	C9,89,97
56	CAP,DISK,Z5U .047UF 12V	C1-6,12-19,25-33,39-46,52-57, 59,60,67-76,78-82,83-85
20	CAP, DISK, Z5U .1UF 12V	C20-24,34-38,47-51,61-65
6	TEST POINTS	TP4,8,9,12,13,16
1	CONN, 50 PIN HEADER	J1
1	HTSNK 1" SQ AAVID 5072B	H1
2	SCREW,#4-40 X 3/8	
2	NUT, #4-40 HEX	
1	BOARD, PC K-1013-1 REV D	

13.

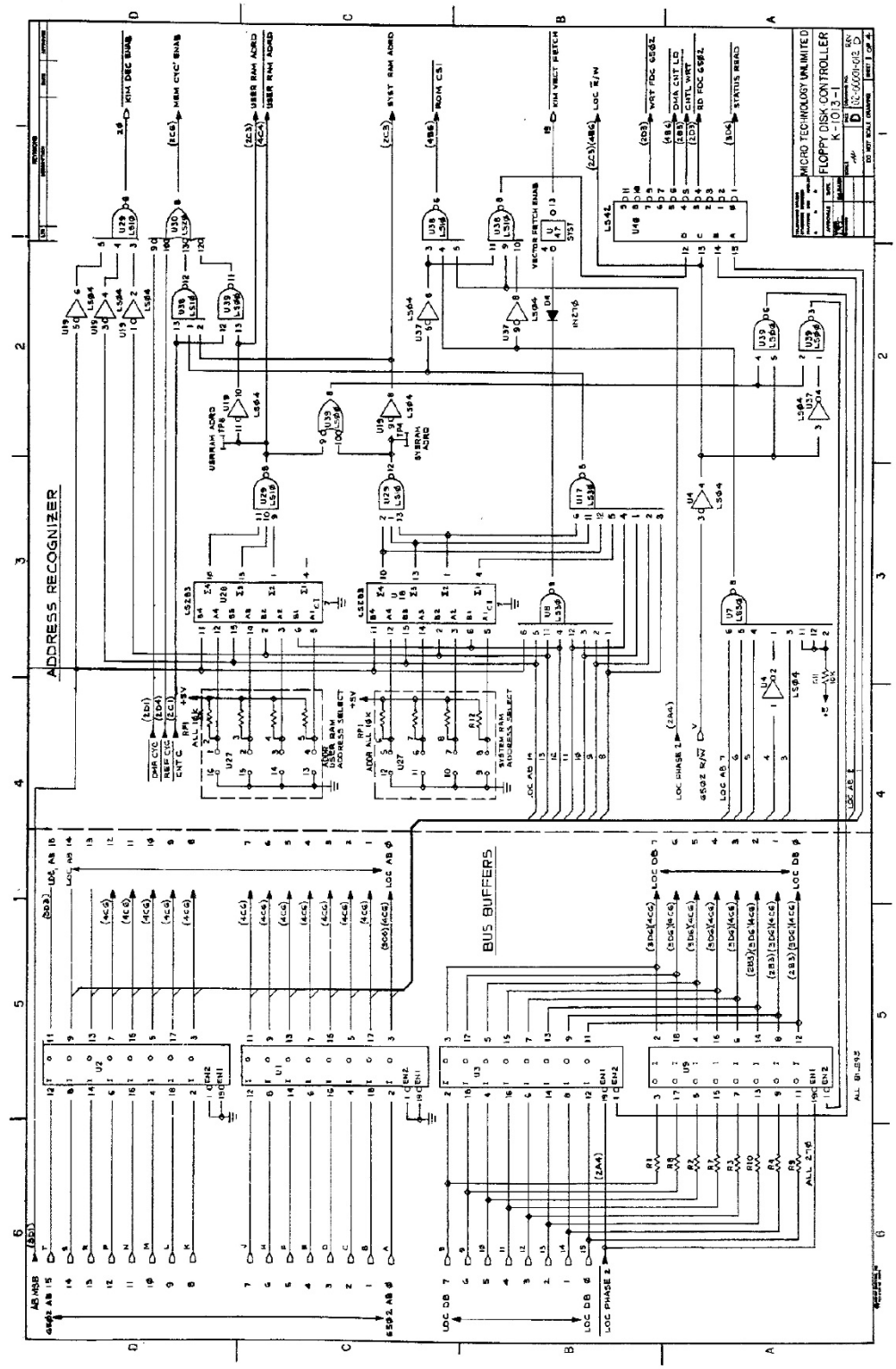
PARTS LAYOUT



14. BLOCK DIAGRAM



15. SCHEMATIC DIAGRAMS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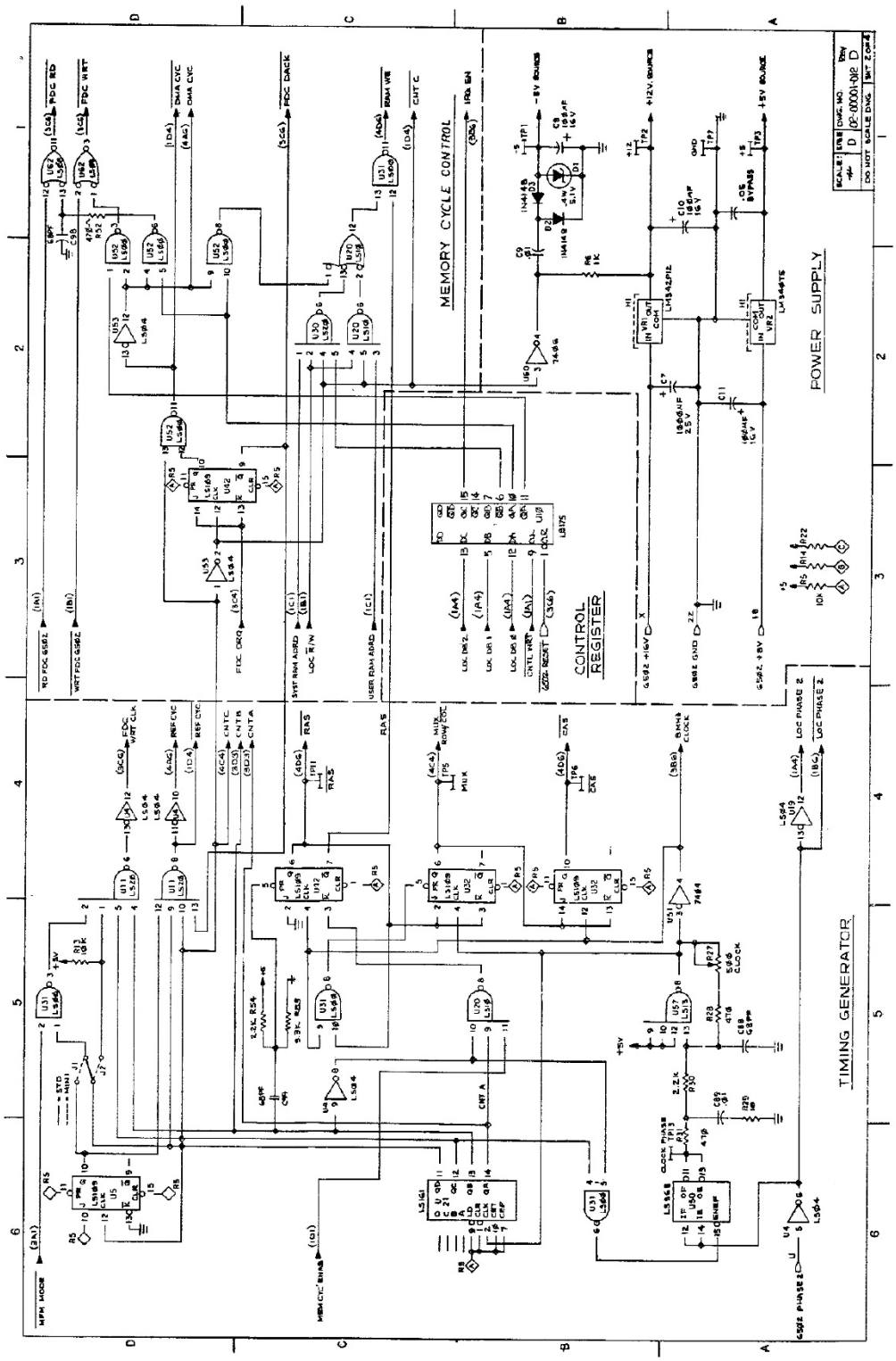
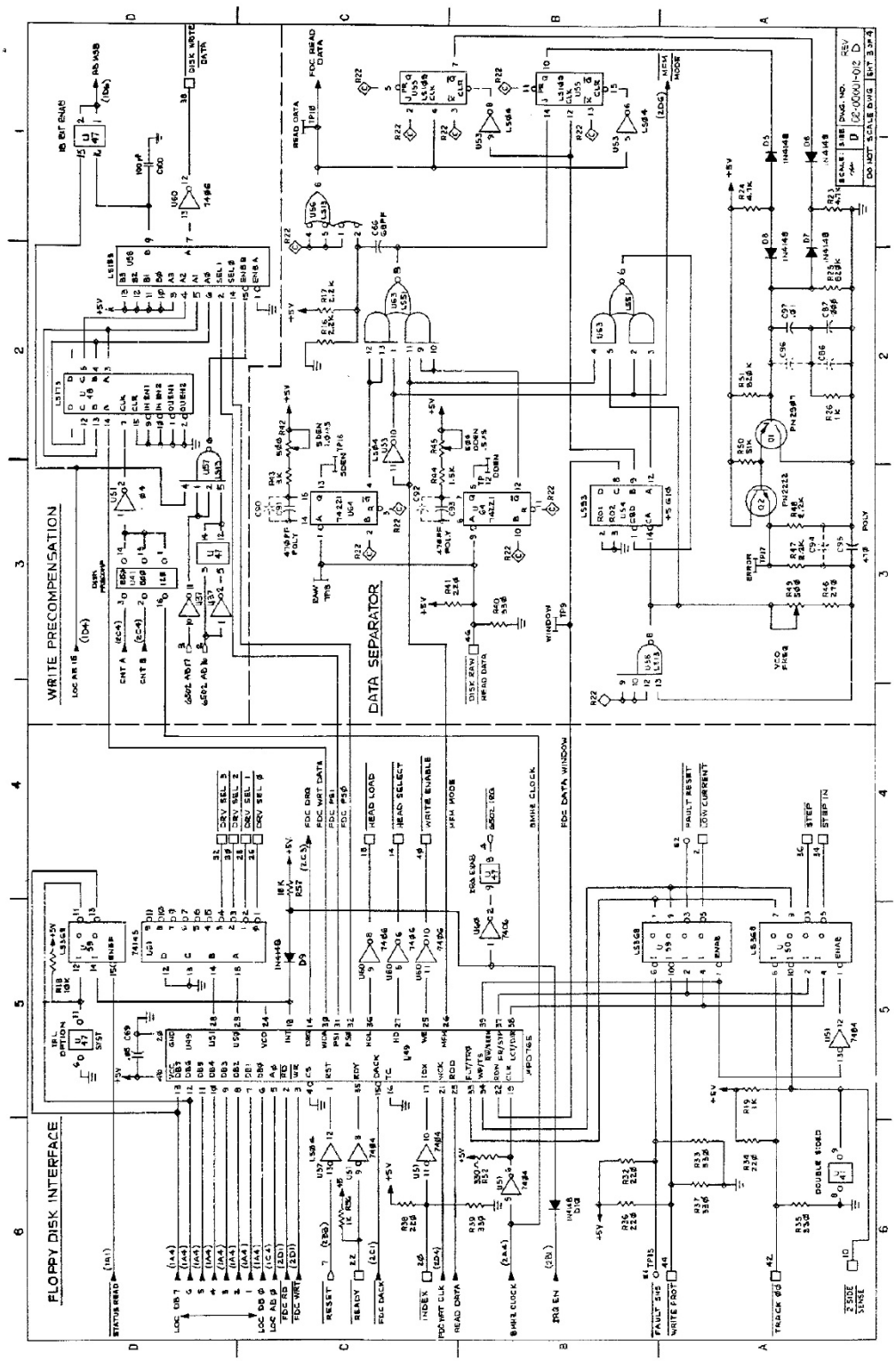
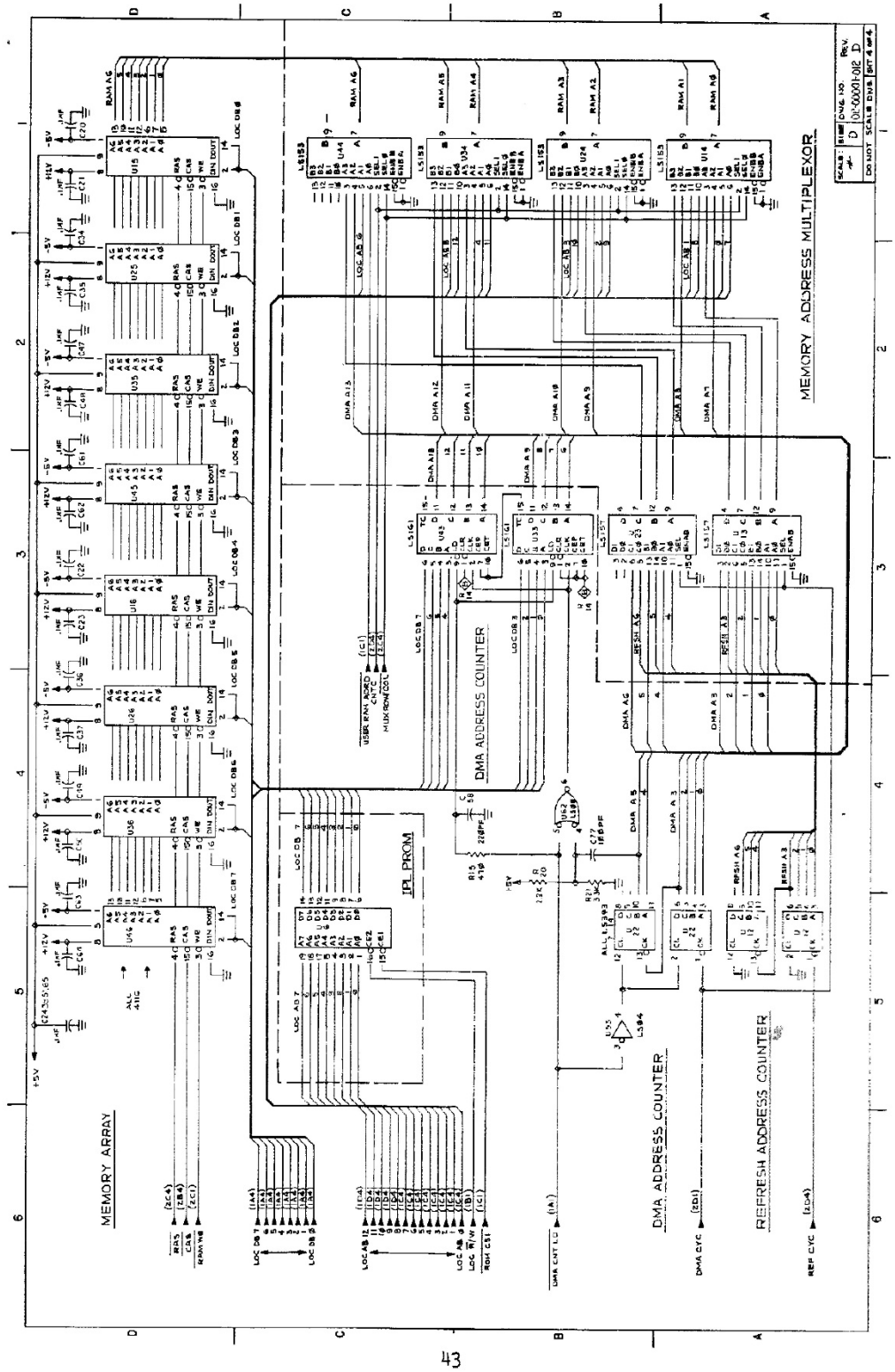
BUS BUFFERS
MICRO TECHNOLOGY UNLIMITED
FLOPPY DISK CONTROLLER
K-1013-1


MEMORY CYCLE CONTROL
POWER SUPPLY
CONTROL REGISTER
TIMING GENERATOR


WRITE PRECOMPENSATION
DATA SEPARATOR
FLOPPY DISK INTERFACE


MEMORY ADDRESS MULTIPLEXOR
DMA ADDRESS COUNTER
IPL PROM
MEMORY ARRAY
DMA ADDRESS COUNTER
REFRESH ADDRESS COUNTER