Micro Technology Unlimited

K-1007-1-PET INTERFACE

BETWEEN
COMMODORE PET-2001 4/8K. P.E.T. COMPUTER
AND
MICRO TECHNOLOGY UNLIMITED BUS DRIVEN PRODUCTS

JULY, 1979

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SPECIFICATIONS

MECHANICAL: The smaller K-1007-2 board is 1.6" long by 4.25" wide exclusive of edge connector. The larger K-1007-1 board is 6" by 6" exclusive of edge fingers. The K-1007-1 board can plug into one half of a K-1005 motherboard/card file.

CABLES The large ribbon cable is 50 conductors and is 12" long, connecting the small board to the large board. The small ribbon cable is 22" long, connecting the large board to the PET monitor. All of the PET expansion signals are available from a separate set of edge fingers on the small board. Three descrete wires are available for attaching the small board to the PET transformer.

POWER SUPPLY: Utilizes PET AC via the included wires to provide +8 volts regulated and +16 volts unregulated to the MTU bus and expansion boards. Maximum current available is .75 amps on the +8 volt output and .35 amps on the +16 volt output.

VIDEO CIRCUITS: Sync processor controls include horizontal position, vertical position, and height for centering the Visible Memory image on the PET screen. The video switch selects PET video after reset, power up or if memory location BFFE is accessed, and selects the Visible Memory image if location BFFF is accessed. Access to PET video and video monitor inputs is via connectors and cables provided.

ADDRESS ENCODER: Encodes PET addresses from 2000 through 7FFF and 9000 through AFFF into a contiguous range from 2000 through 9FFF. PET addresses from B000 through BFFF are translated to F000 through FFFF to take care of the MTU standard I/O page at FE.

SOFTWARE PROVIDED: The manual contains a diagnostic program and a Visible Memory demonstration program listing, both written entirely in BASIC. A high speed machine language graphics software package that is callable from BASIC is available and is called the K-1008-3C.

PET CONNECTOR PIN CONNECTIONS
(odd/even numbering convention)

All Even Numbers GROUND

1	ADDR 0	53	$\overline{\text{RESET}}$
3	ADDR 1	55	$\overline{\text{IRQ}}$
5	ADDR 2	57	PHASE 2
7	ADDR 3	59	READ/WRITE
9	ADDR 4	65	DATA 0
11	ADDR 5	67	DATA 1
13	ADDR 6	69	DATA 2
15	ADDR 7	71	DATA 3
17	ADDR 8	73	DATA 4
19	ADDR 9	75	DATA 5
21	ADDR 10	77	DATA 6
23	ADDR 11	79	DATA 7
31	$\overline{\text{SEL 1}}$		
33	$\overline{\text{SEL 2}}$		
35	$\overline{\text{SEL 3}}$		
37	$\overline{\text{SEL 4}}$		
39	$\overline{\text{SEL 5}}$		
41	$\overline{\text{SEL 6}}$		
43	$\overline{\text{SEL 7}}$		
45	$\overline{\text{SEL 9}}$		
47	$\overline{\text{SEL 10}}$		
49	$\overline{\text{SEL 11}}$		

MTU BUS CONNECTOR PIN CONNECTIONS
(industry standard numbering)

A	ADDR 0	1	N.C.
B	ADDR 1	2	VM VIDEO
C	ADDR 2	3	N.C.
D	ADDR 3	4	$\overline{\text{IRQ}}$
E	ADDR 4	5	N.C.
F	ADDR 5	6	N.C.
H	ADDR 6	7	RESET
J	ADDR 7	8	DATA 7
K	ADDR 8	9	DATA 6
L	ADDR 9	10	DATA 5
M	ADDR 10	11	DATA 4
N	ADDR 11	12	DATA 3
P	ADDR 12	13	DATA 2
R	ADDR 13	14	DATA 1
S	ADDR 14	15	DATA 0
T	ADDR 15	16	VM HORIZONTAL
U	PHASE 2	17	VM VERTICAL
V	READ/WRITE	18	+8 VOLTS
W	$\overline{\text{READ/WRITE}}$	19	VECTOR FETCH
X	+16 VOLTS	20	N.C.
Y	$\overline{\text{PHASE 2}}$	21	N.C.
Z	$\overline{\text{RAM R/W}}$	22	GROUND

MICRO TECHNOLOGY UNLIMITED PHILOSOPHY

The K-1007-1 system provides the PET user with an electrical and mechanical interface to all Micro Technology Unlimited (MTU) boards. MTU does not presently design major function boards specifically for a particular computer system. All our boards are compatible with the K-1005 card file system, with seperate processors interfaced to our card file structure and electrical connections. This means that once you have started using our hardware system, you will be able to use any of the boards we introduce in the future.

BOARD DESCRIPTION AND WARNINGS

The K-1007-1 interface is a carefully engineered, manufactured, and tested product that should operate perfectly when handled and installed according to the following instructions. Since sensitive semiconductor components are used on the board, damage is possible if the interface is installed or removed while the PET power is on. TURN THE POWER OFF AND WAIT AT LEAST 15 SECONDS before installing or removing it or any of the boards it is connected to.

In the succeeding discussion it is assumed that a K-1008 Visible Memory has also been purchased for use with the K-1007-1 interface. If the interface was purchased instead to make use of our 16K memory or PROM/IO boards most comments still apply although those regarding the display do not. Note that the K-1007-1 interface works with the OLD style PET's with the calculator type keyboard. The version for new PET's is the K-1007-3.

INSTALLATION AND INITIAL CHECKOUT

1. Remove the 4 screws on the underside of the PET to allow the top half of the system to be tilted up.

2. Plug the small printed circuit board marked K-1007-2 onto the PET memory expansion edge fingers (as shown on the installation drawing, section B-B).

3. Take the 3 separate wires and solder them to the indicated large power diodes on the PET main logic board.

4. Leave the narrow ribbon cable disconnected until later

5. Turn the PET power on. Operation should be completely normal and not impaired in any way. The interface must pass this test before continuing with the next step. If the normal READY message does not appear, immediately turn power off and check the installation. Check to see if the small board is plugged onto the PET memory expansion port straight and is fully seated. Recheck the three power wires to be sure they were installed properly and try again. If still no luck, completely remove the interface and verify that normal PET operation is restored. Then make a careful visual inspection of the two boards for shipping damage. If no specific problem can be found, return the interface along with a problem description to the factory for warranty repair.

6. Lay the K-1007-1 logic board at the other end of the ribbon cables flat on a non-metallic surface and plug the K-1008-PET Visible Memory into it as shown in the second diagram.

7. The visible memory has been jumpered for addressing in the second 8K block (2000-3FFF hex) which is appropriate for 8K PET's. Please test the board jumpered this way if possible.

8. Turn the PET power on. Operation should again be normal but the PET should now say that 15,359 bytes are available rather than the normal 7,167 bytes (if you have an 8K PET). The interface/Visible Memory combination must pass this test before continuing.

9. Turn the PET power off and remove the 7 position (6 wires and 1 polarizing pin) video connector which connects the PET main logic board to the display monitor.

10. Plug the 14 wire cable from the K-1007-1 printed circuit board onto the pins which are now exposed because the video cable was removed. The 14 pin socket on the MTU cable should be plugged in such that the unconnected row of 7 pins is on the right side of the PET connector which is plugged into the left row of 7 pins (see the assembly diagram, section A-A).

11. Plug the PET video cable connector from the display onto the 6 posts pointing up on the 14 pin socket used in D above. These posts are the long ones, not the short ones above the PET connector below. Polarizing pins in the connectors should prevent incorrect installation in steps 10 and 11.

12. Be sure that the slide switch handle between the two ribbon cables on the large interface board is moved away from the edge of the board as far as possible (it is a three position switch).

13. Turn the PET on again. Operation should still be normal except for the increased amount of user memory available. If the monitor screen should fail to light up, immediately turn power off and check installation of the small ribbon cable and video socket.

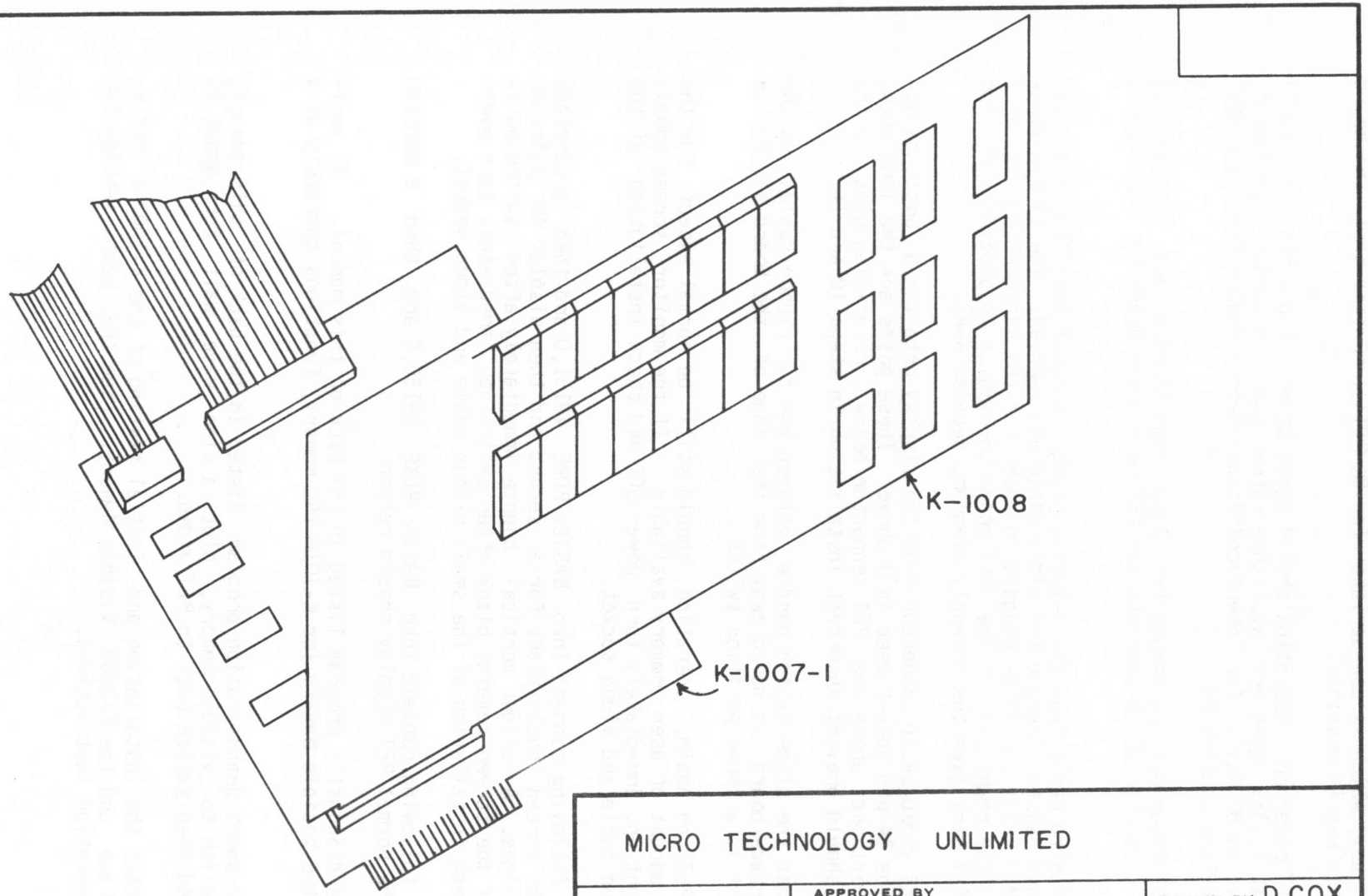
14. Type the following command into BASIC: POKE 49151,0 and then a carriage return. The screen should blank for a second and then display 40 pairs of vertical lines. A slight vertical bounce immediately after switching is normal. If the screen remains blank after switching, immediately turn power off and check installation of the small ribbon cable and video socket.

15. Type the following command into BASIC: POKE 49150,0 and then a carrige return. The normal PET display should return.

16. Type in the diagnostic program listed in the back of this manual. It verifies that the Visible Memory (or K-1016 16K memory) functions correctly as a memory.

17. Type in the short demonstration program listed in the back of this manual. It will switch to visible memory, plot a sine wave, wait for about 10 seconds, and then switch back to PET video.

18. This completes the installation and initial testing of the K-1007-1 PET to MTU interface and the K-1008 Visible Memory. See the next section for detailed operation instructions.

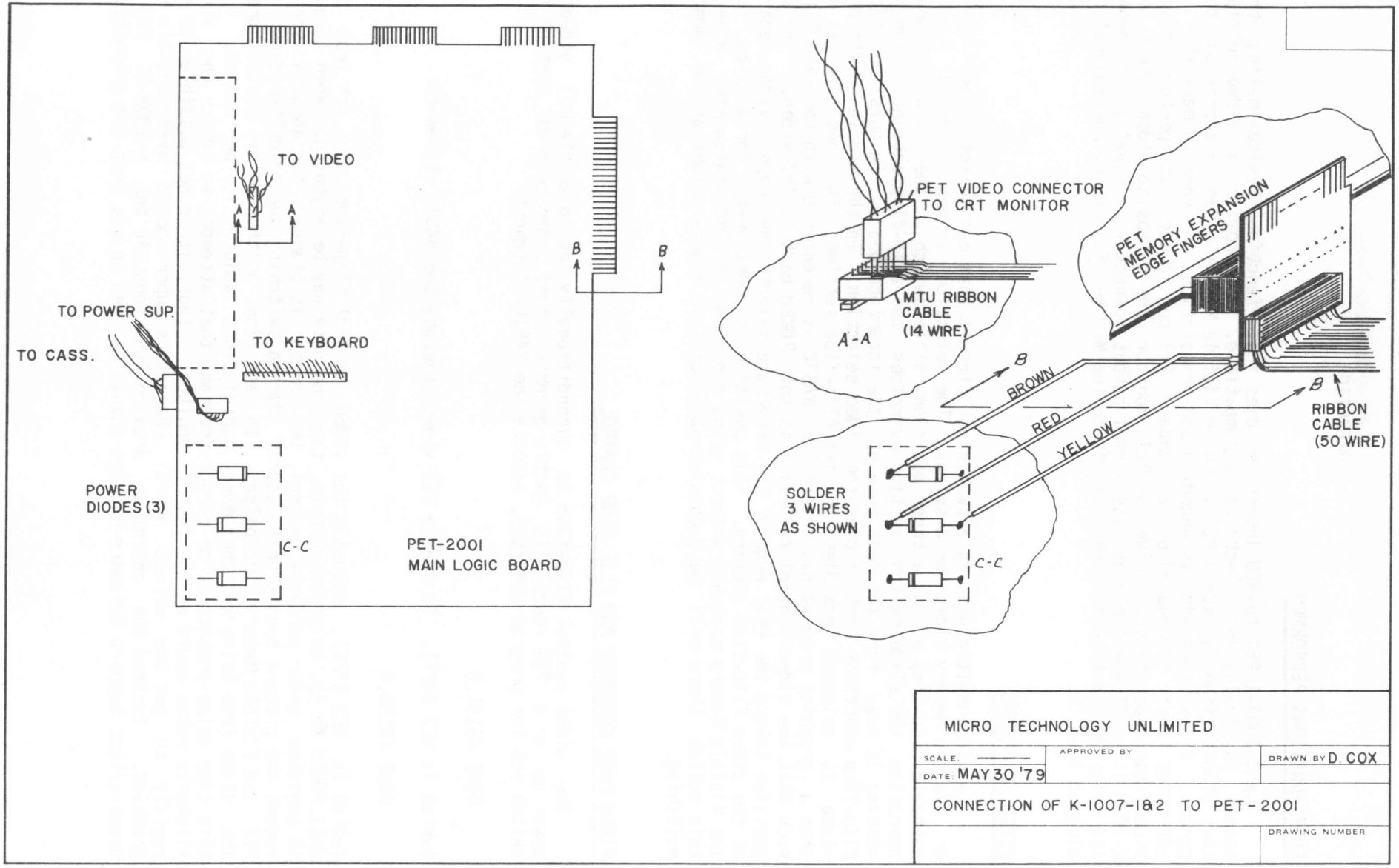


MICRO TECHNOLOGY UNLIMITED

SCALE:	APPROVED BY	DRAWN BY D.COX
DATE: MAY 30 '79		

ASSEMBLY OF K-1008 TO K-1007-1 PET INTERFACE

DRAWING NUMBER



MICRO TECHNOLOGY UNLIMITED		
SCALE:	APPROVED BY	DRAWN BY D. COX
DATE: MAY 30 '79		
CONNECTION OF K-1007-182 TO PET-2001		
		DRAWING NUMBER

OPERATION

FOUR FUNCTIONS PERFORMED

The K-1007-1 PET-to-MTU interface does four functions besides making the two busses physically and electrically compatible. It provides a video multiplexor that allows either standard PET video or Visible Memory video to appear on the PET screen. It performs address encoding and translation in order to make the 36K of addresses that are unused on a standard PET contiguous. It performs composite video/sync separation to drive the PET monitor (the composite video output of the K-1008 is still available at its normal output connector). Finally, it generates +16 volts DC and transfers +8 volts DC to the MTU bus for use by peripheral boards plugged into it.

VIDEO SWITCHING

The video multiplexor is a switching circuit that can select either PET video or Visible Memory video for display. The selection is controlled by a software settable flip-flop and by a three position slide switch on the K-1007-1 board. In operation the slide switch setting overrides the flip-flop setting. The normal setting is away from the rear edge of the interface board. In this position the flip-flop exercises control over the video selection. In the middle position, PET video is selected regardless of the flip-flop setting. This position is useful when a graphics program has crashed or BASIC is re-entered with the RUN/STOP key such that the video control flip-flop is not POKEd back to PET video. The switch position toward the rear edge of the interface selects the graphic video regardless of the video flip-flop setting. This position is most useful for a quick look at the Visible Memory contents without using a program or POKE statements. When using this switch there will be a considerable picture bounce right at the momont of switching.

VIDEO POKE COMMANDS AND FLIP-FLOP CONTROL

The video control flip-flop is unconditionally set to enable PET video after power up or a PET reset. To enable graphic video under program control (slide switch set for program control), execute the BASIC statement:

```
POKE 49151,0
```

(which is HEX BFFF). To enable PET video, execute the BASIC statement:

```
POKE 49150,0
```

(which is HEX BFFE). Actually the video control flip-flop does not look at the data POKEd to it, only the address, thus the data may be anything. When the video is switched under software control, the screen is blanked for about a second to reduce the picture bounce that occurrs during switching due to differences in the PET and Visible Memory sync pulses. In addition, another delay circuit prevents the video from being switched more rapidly than about twice per second. Without this time delay protection an errant program that attempts to switch the video at kilohertz rates could damage the PET monitor. Thus, it is not possible to switch rapidly to get the effect of PET characters superimposed over Visible Memory graphics. Instead the character drawing functions in the K-1008-3C PET BASIC Graphic/Text Support Software Package should be used to mix text and graphics.

HARDWARE ADDRESS TRANSLATION

Although the address encoding and translation performed by the K-1007-1 may appear to be confusing, it has been set up to provide the greatest flexibility possible in configuring our MTU bus expansion boards. The table below relates the addresses generated by the PET with the addresses that appear on the MTU bus on the other side of the interface:

PET ADDRESSES	MTU ADDRESSES	USE	PET ADDRESSES	MTU ADDRESSES	USE
0000 - 0FFF	0000 - 0FFF	PET RAM	8000 - 8FFF	0000 - 0FFF	PET SCREEN
1000 - 1FFF	1000 - 1FFF	PET RAM[1]	9000 - 9FFF	8000 - 8FFF	FREE[3]
2000 - 2FFF	2000 - 2FFF	FREE[2]	A000 - AFFF	9000 - 9FFF	FREE[3]
3000 - 3FFF	3000 - 3FFF	FREE[2]	B000 - BFFF	F000 - FFFF	FREE[3]
4000 - 4FFF	4000 - 4FFF	FREE[2]	C000 - CFFF	0000 - 0FFF	PET ROM
5000 - 5FFF	5000 - 5FFF	FREE[2]	D000 - DFFF	0000 - 0FFF	PET ROM
6000 - 6FFF	6000 - 6FFF	FREE[2]	E000 - EFFF	0000 - 0FFF	PET ROM
7000 - 7FFF	7000 - 7FFF	FREE[2]	F000 - FFFF	0000 - 0FFF	PET ROM

1. In 8K PET's 2. Can be used by BASIC 3. Protected from BASIC

Examination of the table will reveal several properties. First, addresses that belong exclusively to the PET such as its own ROM, its screen memory, and its first 4K are all translated to 0000 - 0FFF on the MTU side. When doing this it is required that no boards on the MTU bus respond to addresses from 0000 to 0FFF. The next property is that starting from 2000, 32K of unassigned PET addresses are contiguous in the KIM address space. Thus the "hole" from 8000 to 8FFF which contains the pet screen memory is "filled" on the MTU side of the interface. (For 4K PET owners, 36K of unassigned addresses are available.) The last property is that PET addresses from B000 to BFFF are translated to F000 to FFFF on the MTU bus. These addresses have been reserved for use as I/O addresses and any PROM that might be installed on the MTU bus.

SOFTWARE ADDRESSING

It is important not to become confused by the address translation that is being performed since it is transparent to the PET. For example, if one wishes the Visible Memory to be addressed above the PET screen from PET address 9000 to AFFF, the Visible Memory board itself would be jumpered for operation from 8000 to 9FFF since these are the addresses that would appear on the MTU bus. The PET program still uses addresses between 9000 and AFFF; it doesn't know that the addresses are translated and it doesn't care! Another example would be putting the VM Graphics routines into two 2708 PROM's on a K-1012 PROM/IO board so they do not have to be loaded before use and do not take space in the 32K of memory that PET BASIC can address. As will be recommended in the next section, they should reside from B000 to B7FF in the PET. Now on the MTU bus these addresses will be translated to F000 to F7FF but the program stored in the PROM's must still be assembled for addresses from B000 to B7FF since the computer that will be executing the program (the PET) will be generating these addresses during execution. The only effect of address translation is the way that a MTU bus board is jumpered, it has no effect on the PET or software addresses.

COMPOSITE SYNC AND VIDEO SEPERATION

Video processing circuitry is present on the K-1007-1 which serves to convert signals from the Visible Memory, which were designed for standard CCTV monitors, into the form required by the PET monitor. Three controls are associated with this circuitry. Although they have been adjusted at the factory, there is a possibility that differences between PET systems may necessitate readjustment. Note that these controls should be adjusted with a small jeweler's screwdriver.

R9, which is the one closest to 22/44 pin socket, is the horizontal centering control and is the one most likely to require adjustment. R13, which is closest to the large ribbon cable, is vertical centering. The middle control, which is R11, is the height control which has a narrow adjustment effect on height. It is adjusted at the factory for a vertical drive pulse width of 1.3 milliseconds, which is the same as the PET logic board puts out. It should not require adjustment to produce the same height as the PET's own video signals.

POWER SUPPLY

The last function of the K-1007-1 PET to MTU Interface is to condition and provide power to the MTU bus boards. The amount of power available is sufficient to power any mix of up to 4 MTU boards without significant additional strain on the PET power supply. Two voltages are distributed on the MTU bus. The first is +8 volts of unregulated DC which is simply transferred from the PET rectifiers to the MTU bus. Operating power for the K-1007-1 itself is drawn from this voltage and regulated to +5 volts. The other voltage required is +16 volts unregulated. Raw AC from the PET transformer is voltage doubled and rectified to provide this voltage to the MTU boards where they transform it to +12 and -5 volts regualted.

------WARNING------

The present power connector from the PET transformer to the PET main logic board is not sufficient to handle even the PET main logic board current. This means that failure of this connector can occur WITH NO ADDITIONAL CURRENT LOAD THROUGH IT. The connector is designed by its manufacturer to handle 3 amps of current maximum. The power supply current passing through it in the PET can have peak current spikes up to 10 amps. MTU recommends that this connector be replaced by a more sufficient one OR the power wires in the white nylon connector housing (female portion) be soldered to the male pins on the PET main logic board. Otherwise deterioration of the connector will continue to occur until it fails at some point in the future, possibly causing loss of data or programs.

CONNECTION TO MTU BOARDS/SYSTEM

SINGLE BOARD OPERATION

The K-1007-1 has both edge fingers and an edge socket for connecting to MTU bus boards providing the least cost and greatest expansion flexibility. The socket is provided for those who wish only to use a single MTU bus board such as the K-1008 Visible Memory.

EXPANSION TO MULTI-BOARD SYSTEM

For applications using two or more MTU bus boards, the edge fingers can be plugged into a K-1005-PET motherboard/card file which will then hold up to 4 boards in addition to the K-1007-1 interface board. On other MTU K-1005 card file models (non -PET), the top slot which is normally used by the processor is not usable for the K-1007-1 board as received. The following jumper wires must be added to the motherboard from the top connector pins to the second down connector pins:

1. Pin X to supply +16V DC to the MTU boards.
2. Pin 2 to connect video to the K-1007-1
3. Pin 16 to connect horizontal drive to the K-1007-1
3. Pin 17 to connect vertical drive to the K-1007-1

AFTER MODIFICATION ONLY THE K-1007 MAY BE USED IN THE CARD FILE; A KIM, SYM, OR AIM WILL BE DAMAGED IF IT IS PLUGGED IN WITH THESE JUMPER WIRES IN PLACE!

Note that there is no obsoleted equipment in expanding from a single board to multiple boards.

WARNING

Ribbon cables are used with the K-1007-1 PET interface in order to provide a high degree of reliability at low cost. Unfortunately they are less rugged than might be desired. For trouble-free operation never subject the connector/cable joining point to heavy stress. In particular, never let the K-1007-1 dangle by the ribbon cables. Also, it is a good idea to disconnect the interface or securely tape it to the PET when the PET is moved.

Most people have their own ideas about how a computer system should be configured. The following are merely suggestions as to the most effective ways to configure a PET, K-1007-1 interface, and various K series MTU boards. Note that all MTU boards are address selectable by jumpers.

USE OF THE K-1008 VISIBLE MEMORY

The Visible Memory board and our support software packages are configured for Visible Memory addressing from 2000 to 3FFF hexadecimal. These locations are just above the PET's own memory and therefore have the advantage that PET BASIC can use the Visible memory for program and data storage when it is not being used for graphics. Note that when using the Visible Memory for graphics without benefit of the K-1008-3C software package, it is necessary to protect it from BASIC. This is accomplished by typing:

1.On PET's with old ROM's - POKE 135,32 and then a carriage return.
2.On PET's with new ROM's - POKE 53,32 and then a carriage return.

If you never intend to use the Visible Memory as memory and desire that it be automatically protected, it should be jumpered for addressing from 8000 to 9FFF which are PET addresses 9000 to AFFF. This places it just above the PET's own display memory, a fairly logical location that cannot be reached by BASIC (except through PEEK's and POKE's of course). Also users who anticipate upgrading their PET's memory later might want to consider placing the Visible Memory here so that old programs will not have to be modified when the Visible Memory is moved to make space for the new memory. When using the K-1008-3C software package, the relocation program will have to be run (see instructions in the software manual).

USE OF THE K-1016 16K MEMORY BOARD

The K-1016 16K memory is an ideal method of expanding the PET to 24K. In conjunction with a Visible Memory, up to 32K will be available when graphics is not being used. It is always desirable to place the Visible Memory highest in address order so that BASIC can use all of the non-visible memory (BASIC requires that its memory be contiguous). Therefore the K-1016 would be jumpered for addresses from 2000 to 5FFF and the Visible Memory would be jumpered for 6000 to 7FFF.

The maximum RAM configuration would be a K-1016 16K memory and two K-1008 Visible Memories which would provide 32K of memory for BASIC as well as Visible Memory graphics. The first Visible Memory (the one used for graphics) would be reconfigured for addressing from 8000 to 9FFF and the second would be jumpered for 6000 to 7FFF. Note that the second Visible Memory must NOT have the PET suffix on its part number. This means that the video signals are not hand wired to the edge fingers where they would interfere with the first board. If desired however video from the second board (as well as the first) is still available from the jack at the edge of the board and can be used to drive a standard CCTV monitor.

USE OF THE K-1012 PROM/IO/COMM/PROGRAMMER BOARD

The K-1012 PROM/IO board is also useable with the PET and K-1007-1 interface. If 3K or less of the PROM on the K-1012 is needed (such as to permantly hold the graphics support package), it should be auxiliary PROM. Three auxiliary PROM sockets should be enabled and the addressing jumpers should be set for F000, F400, and F800. The main PROM should be disabled. The I/O page should be set for FE and the I/O base can be set for anything. Because of K-1007-1 address translation, the PROM will be from B000 through BBFF and the I/O page will be BE from the PET's point of view. If more PROM is needed, the main array can be enabled and jumpered for addressing from 8000 to 9FFF. Note that this action will force the Visible Memory to be placed in the BASIC area below 8000.

COMPATIBILITY WITH OTHER INTERFACES

Some PET owners will have already purchased a memory expansion interface from another vendor and wish to utilize the high resolution graphics that the K-1007-1 and Visible Memory combination offers. We have not tested all of the various expansions on the market along with our unit but, we can point out some considerations and offer suggestions. In the following discussion it is assumed that only the Visible Memory is used with the K-1007-1 interface.

The most important level of compatibility is mechanical compatibility. Examination of the small K-1007-2 board that plugs onto the PET reveals that another set of edge fingers identical to those on the PET memory expansion port are present. These fingers are oriented such that if the PET expansion edge fingers were rotated 90 degrees up, they would be identical. Note that all of the PET component side contacts are gound and are connected together. In order to use a competitive interface along with the K-1007-1, first plug the K-1007-1 into the PET and then plug the competitive interface into the K-1007-1. Although the edge fingers are oriented differently from those on the PET it should be possible in most cases to completely close the pet cover.

The most important electrical compatibility consideration is where the Visible Memory will be addressed. The locations chosen must not interfere with active locations in the competitive expansion interface if memory is present on it. Due to the design of the K-1007-1 and Visible memory, the only addressing possibilities are 2000-3FFF, 4000-5FFF, 6000-7FFF, and 9000-AFFF (PET addresses). Since the goal of most competitive interfaces is to provide up to 32K of memory for PET BASIC, in all likelihood the only addressing possibility will be the 9000-AFFF slot.

Some interfaces may offer ROM and I/O functions as well as memory, probably addressed above the PET screen. Hopefully they will be addressed in the range of B000-BFFF and leave 9000-AFFF free for the Visible Memory. Note however that BFFE and BFFF are used to control the video switcher flip-flop on the K-1007-1. If these addresses refer to an I/O port on the competitive interface there could be a conflict. On the other hand, if they refer to ROM there is no problem since ROM cannot be written to and the video switch does not respond to read cycles at these locations. In summary, if there is no place to put the Visible Memory in address space when used in addition to expansion products other than MTU, there will be a problem unless something is modified. The Principles of Operation section in this manual should provide the information needed to modify the K-1007-1 if that seems necessary. Note that such modification might void the warranty if it is extensive or done sloppily.

There is one last compatibility consideration that might cause a serious contention problem. This problem can only occur if the competitive interface is buffered. Small interfaces may not be buffered since the PET bus itself is buffered and therefore will not suffer from this problem. S-100 conversion interfaces on the other hand are likely to be buffered if they will hold a large number of boards.

The cause of the problem with other buffered systems is the data bus buffers in the interface. These buffers have no way of knowing whether a board plugged into the converted bus is responding to an address or not. Therefore they are usually designed so that all addresses that do not belong to the PET will activate the buffer. Obviously this ignores the presence of any other product connected to the PET in parallel with these buffers (such as MTU products on the K-1007-1) which is unbuffered and so it will fight the data bus buffers on the competitive interface. Usually this contention problem only shows up when trying to read the Visible Memory. The only solution to this problem if it exists is to change the buffer activation logic on the competitive interface to open up a hole for the Visible Memory.

PRINCIPLES OF OPERATION

The K-1007-1 PET to MTU bus interface consists of four major circuit blocks. The first is the video multiplexor which chooses the PET video signals or the Visible Memory graphic video signals. The second is the bus translation logic itself which converts PET addresses and timing signals into MTU format. The third is the video processor which converts video signals from the Visible Memory into the form required by the PET monitor. The last section is the power supply circuitry.

VIDEO MULTIPLEXOR CIRCUITRY

The majority of the circuitry on the board is devoted to handling video functions. U6-6 and U6-12 form a cross-coupled flip-flop which is the video switching control flip-flop. A momentary low into U6-4 will set the flip-flop while a momentary low into U6-1 or 13 will reset the flip-flop. Reset from the PET is connected to U6-13 so that the flop will always be off following power up or a PET reset. U1 and U2 together detect the two addresses that are used to control the flip-flop under software control. U2 looks for A1-A7 to be ONEs which gives a lower address byte of either FE or FF. U1 is activated only if U2 is satisfied and VECTOR FETCH is present. The latter signal is generated by all MTU bus interface boards when the upper address byte is FF. Thus U1 is activated by MTU bus addresses FFFE and FFFF. Since PET addresses have been translated by the preceeding circuitry, U1 will be activated by PET addresses BFFE and BFFF. Note that an MTU board must be plugged into the K-1007-1 for the video flip-flop address decoder to function. Once activated, U1 then looks at A0 and RAM R/W and pulses pin 2 low if a write cycle to FFFE is performed or pulses pin 1 low on write cycles to FFFF. Read cycles to these addresses or write cycles to any other address will leave both of these outputs high. When U1-2 pulses low, the video control flip-flop is set and when U1-1 pulses low, the flop is reset.

The state of the control flip-flop passes through U3-8 before reaching the actual video switch. The R-C network at the input of this gate restricts the maximum frequency that can pass to a few Hertz. Any higher frequency will leave U3-8 in a fixed state since the voltage swing at its input will be insufficient to cross both switching thresholds of the schmidt trigger gate.

U3-6 and U11-6 form a single-shot that is triggered whenever U1-1 or U1-2 is pulsed. Normally U11-6 is high at +3.5 volts and the other end of C1 is also at about 3.5 volts. When U3-1 or 5 pulses low, U11-3 also pulses low which feeds a low back to U3-2 since C1 cannot charge instantly. This latches U11-6 low until the capacitor can recharge to the threshold voltage of U3. When this occurs, U11-6 snaps back high and remains until triggered again. While U11-6 is low, video to the PET monitor is blanked so that switching interference is not seen.

U12 is the actual video multiplexor. When its SEL line is low, PET horizontal, vertical, and video signals pass right through and are sent to the monitor. When SEL is high, processed Visible Memory signals are sent to the monitor. The three position slide switch can force SEL low for PET video, force it high for Visible Memory video, or connect it to U3-8 for video flip-flop control of video selection. U11-11 and U11-8 form a blanking gate for blanking the video during switching.

The bounce that occurs during switching is due to a phase discontinuity that occurrs in the horizontal and vertical sync signals when they are switched. Although the PET and VM sync signals are of exactly the same frequency, their relative phase is randomly determined at power up. The bounce is simply the PET monitor sweep circuits readjusting to the new phase. Excessively rapid switching (which is prevented by R6, C5, and U3-8) might cause overheating of the monitor due to constant readjustment activity.

BUS ADDRESS TRANSLATION LOGIC

The bus translation logic is in the left half of the schematic and is actually quite straightforward since both the source and destination buses are optimized for the 6502 microprocessor. The 8 data lines are simply passed through the interface with no connection whatever to anything on the board. The lower 12 address lines from the PET are also passed through the interface to the MTU bus with no processing required. The upper 4 address lines however are decoded by the PET internally and are available on the PET's expansion connector only in their decoded form. Thus some logic is necessary to re-encode them into the 4 address bits required by MTU bus peripherals. This encoding is performed by U6-8, U7, U9, and U10. Each gate output is associated with an address bit. For encoding, a decoded line from the PET (called SEL lines in PET literature) is simply OR-ed into those gates corresponding to ONE's in the desired binary encoding of the 4K block. Thus SEL5, which is activated by the PET when an address in the range of 5000-5FFF is accessed, would be connected to U7 and U9 which correspond to the ONE's in the binary 0101 representation of 5. This arrangement makes it easy to encode addresses by 4K blocks in any way desired. The encoding actually performed by this circuitry is given in the Operation section of this manual. Note that when no SEL lines are activated none of the encoding gates will be activated either so 0000 will be placed onto the most significant 4 MTU bus address lines.

The remaining conversion logic is in the extreme lower left corner of the schematic. Here both true and false PHASE 2 and READ/WRITE signals are generated for the MTU bus. Also PHASE 2 and READ/WRITE are ANDed together in order to generate a memory write strobe which is a standard MTU bus signal. Note that a READY signal is simply not available from the PET so any memory or peripheral connected to the bus must be fast enough to function without wait states. (Actually wait states went out with 1702 EPROM's since all modern memory IC's are more than fast enough to run with the processor at full speed.)

SYNC SEPERATION FROM VIDEO

Unlike most standard monitors, the PET monitor requires separate horizontal sync, vertical sync, and video signals. The most straightforward way of providing these from the Visible Memory is to bring out the appropriate signals to the edge fingers and arrange for them to be available to the K-1007-1. These signals must then be converted into the proper waveform for the monitor. In addition, by changing the phase of the sync signals with respect to the video data, limited adjustment of image centering and size is possible.

U5 is the horizontal sync processor. The leftmost section is used to adjust the time delay between the positive edge of the VM horizontal sync signal and the beginning of the horizontal retrace pulse to the PET. Fixed resistor R5 and variable resistor R9 determine this delay which serves to HORIZONTALLY CENTER the VM image. The rightmost section generates the proper width (24 microseconds) horizontal retrace pulse after the delay period. R9 has been adjusted at the factory for good horizontal centering but there is expected to be some variation among PET monitors that would require readjustment.

U8 likewise is the vertical sync processor. The leftmost section controls vertical centering in the same way as horizontal centering discussed above. Variable resistor R13 is the VERTICAL CENTERING control and is factory adjusted. The rightmost section generates the vertical retrace pulse. The pulse width has a slight effect on image height. Variable resistor R11 is adjusted at the factory for a 1.3MS pulse width which is what the PET itself provides.

POWER SUPPLY

The power supply is in the upper right corner of the drawing. Unregulated 8 volts from the PET is simply decoupled and pass through to the MTU bus. Regulator Q1 provides sufficient 5 volts to power the logic on the K-1007-1 board. Unregulated 16 volts DC is produced by half-wave voltage doubler D1, D2, C18, and C15. R15 and R16 discharge the two filter capacitors when power is turned off to prevent damage when the board is installed or removed. This power supply circuit has a capacity of 300 to 500MA when C15 is supplemented by the additional filtering capacitance found on all MTU bus interface boards that use 16 volts. Otherwise a 1000uF 25 volt capacitor must be connected accross C15 if more than about 50MA is drawn from +16 volts.

------WARNING------

The present power connector from the PET transformer to the PET main logic board is not sufficient to handle even the PET main logic board current. This means that failure of this connector can occur WITH NO ADDITIONAL CURRENT LOAD THROUGH IT. The connector is designed by its manufacturer to handle 3 amps of current maximum. The power supply current passing through it in the PET can have peak current spikes up to 10 amps. MTU recommends that this connector be replaced by a more sufficient one OR the power wires in the white nylon connector housing (female portion) be soldered to the male pins on the PET main logic board. Otherwise deterioration of the connector will continue to occur until it fails at some point in the future, possibly causing loss of data or programs.

TROUBLESHOOTING

Before a K-1007-1 interface leaves the factory it is actually connected to a standard 8K PET, a Visible Memory is plugged into it, and the diagnostic program listed in the back of this manual is run with no errors allowed. Once you have received this product, in the event that a problem is uncovered during the installation and checkout procedure listed in the front of this manual, the first step is to make a careful visual inspection of both boards for shipping or mishandling damage. Check for evidence of damage to the ribbon cable terminations, particularly insulation pulled away from the connector. Verify that the Visible Memory is fully seated in its socket and plugged in the right direction. Ditto for the small board that plugs into the PET expansion connector. Recheck all connections to the PET for proper installation.

If the interface interferes with the PET without the Visible Memory plugged in, the most likely source of trouble is the large flat cable or the 80 pin socket that plugs onto the PET. Use a continuity tester (ohmmeter on RX1 range or a single 1.5 volt battery and 1.5 volt flashlight bulb is safe) and check for shorts and opens in the large ribbon cable. Also check for shorts between signals and ground (signals are all on the bottom side and ground is on the top side) on the K-1007-2 board that plugs onto the PET memory expansion port edge fingers. Do this testing with the interface disconnected from the PET. With the interface re-installed on the PET, check for the presence of 5 volts on the various IC's with a voltmeter.

If the interface is OK but the PET won't run with the Visible Memory, carefully inspect the Visible Memory for shipping problems. Verify that three white jumpers are installed in the IC socket near the heatsink and that they bridge pins 1-16, 3-14, and 6-11 (addresses 2000-3FFF selected). They should be flat against the socket when they are fully seated. If a voltmeter is available check if +5 volts and +12 volts is being generated by the regulators on the Visible Memory.

If the PET runs OK with the Visible Memory but does not recognize the additional memory available, perform all of the checks in the previous paragraph. Then, using POKE and PEEK statements in BASIC examine some locations in the VM. For example, try a POKE 10000,255 then a PRINT PEEK(10000). The number 255 should be printed, Try again at location 10001 (to address the other row of memory chips). Then try POKEing zeroes. If data retention is not accurate, examination of the data read back may indicate where to look for a bad memory chip. If 255 is consistently read back, the Visible Memory is not responding to its address. Check the jumpers on the VM and also the large ribbon cable as described in the second paragraph above.

If everything is OK but the PET screen is blank when the video cable is installed, perform the small ribbon cable checks described in the second paragraph above. Try moving the slide switch to see if video appears in any of its three positions.

If the PET video works OK but the screen is blank when the Visible Memory is selected, check to see if the Visible Memory has had the three PET video wire modifications installed. There should be three small guage blue wires running from circuitry on the right half of the board to edge fingers on the left of the board. If these are absent either return the VM for modification or add the following wires: U13-1 to I/O 16; U15-1 to I/O 15; U44-1 to I/O 2.

If the interface and/or the Visible Memory cannot be made operational with the PET, return both of them postpaid along with a description of the problem to the factory for prompt repair.

Diagnostic Program

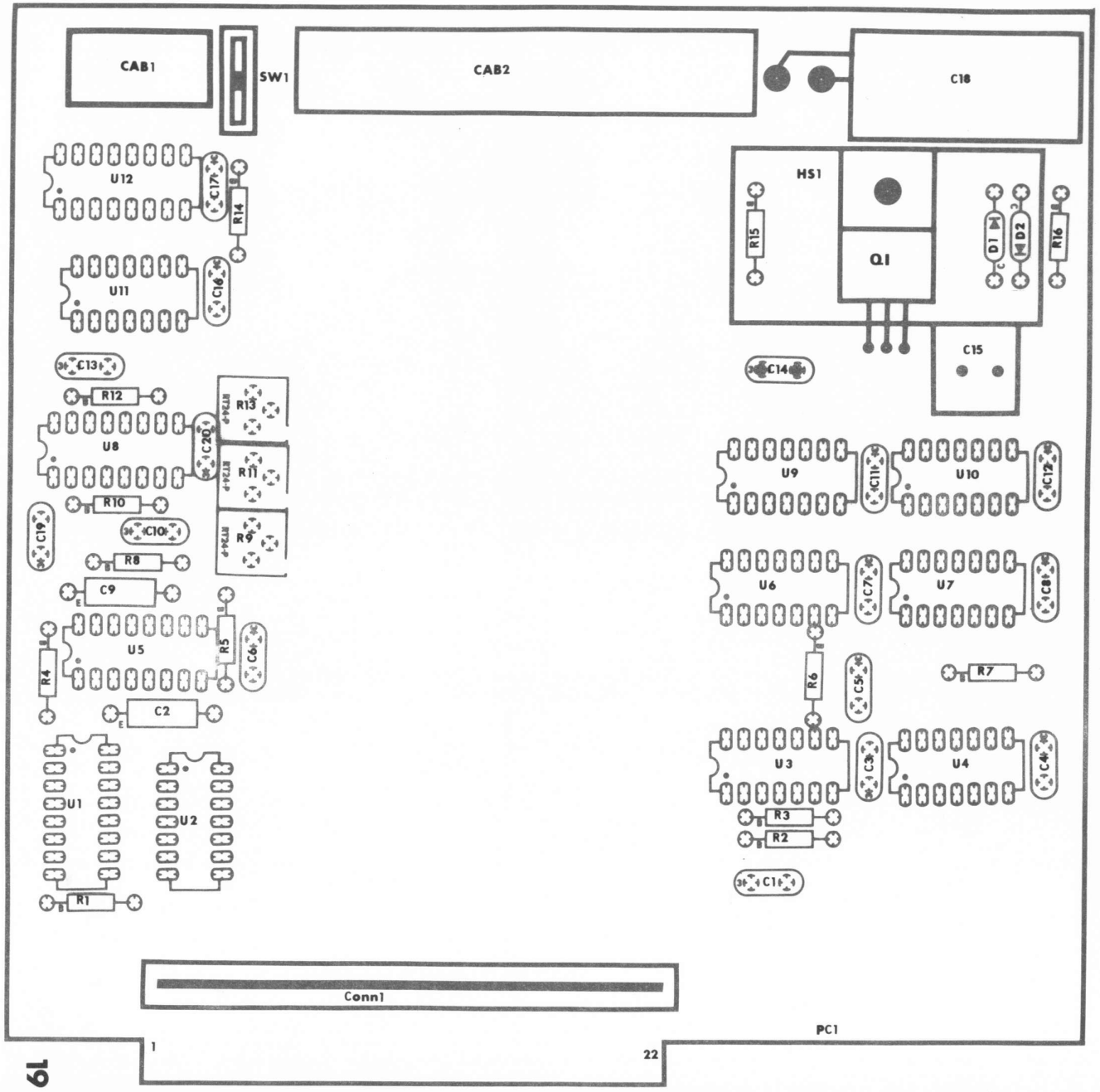
```
10 REM  VISIBLE MEMORY OR 16K MEMORY DIAGNOSTIC PROGRAM
20 REM  TYPE RUN FOR A VISIBLE MEMORY ADDRESSED AT 2000
30 REM  CHANGE LINE 110 TO 16384 FOR A 16K MEMORY
40 REM  ADDRESSED AT 2000
50 REM  CHANGE LINE 100 TO DECIMAL STARTING ADDRESS
60 REM  IF OTHER THAN 2000 HEX (8192 DECIMAL)
100 SA=8192
110 NL=8192
200 FOR I=1 TO 10: REM 10 PASSES THROUGH DIAGNOSTIC
210 SD=RND(1): REM GET RANDOM SEED
220 Z9=RND(-SD)
300 FOR J=SA TO SA+NL-1: REM STORE RANDOM PATTERN IN MEMORY
310 POKE J,RND(1)*256
320 NEXT J
390 Z9=RND(-SD): REM RESTART RANDOM SEQUENCE
400 FOR J=SA TO SA+NL-1: VERIFY MEMORY CONTENTS
410 CT=PEEK(J)
420 RN=INT(256*RND(1))
430 IF CT=RN GOTO 450
440 PRINT 'ERR ADDR';J,'READ';CT,'WRIT';RN
450 NEXT J
500 PRINT 'PASS';I;'COMPLETED'
510 NEXT I
520 STOP
```

Point Plot Demonstration Program

```
10 REM VISIBLE MEMORY POINT PLOT DEMONSTRATION PROGRAM
20 REM TYPE RUN TO GET A PLOT OF A SINE WAVE
30 REM CHANGE LINE 100 TO DECIMAL STARTING ADDRESS
40 REM IF OTHER THAN 2000 HEX (8192 DECIMAL)
100 SA=8192
110 POKE 49151,0: REM SWITCH TO VISIBLE MEMORY
120 GOSUB 1000: REM CLEAR VISIBLE MEMORY
200 FOR X1=0 TO 319
210 Y1=99*SIN(6.28318*X1/320)+100
220 GOSUB 2000: REM PLOT POINT AT X1,Y1
230 NEXT X1
240 FOR I=1 TO 10000: NEXT I
250 POKE 49150,0
260 STOP
1000 REM CLEAR VISIBLE MEMORY AS FAST AS POSSIBLE WITH BASIC
1010 ZR=0
1020 TM=SA+8191
1030 FOR I=SA TO TM: POKE I,ZR: NEXT
1040 RETURN
2000 REM PLOT POINT AT X1,Y1  0 =X1 320  0 =Y1 200
2010 AD=40*INT(199-Y1)+INT(X1/8)+SA
2020 BT=2 (7-(X1 AND 7))
2030 POKE AD,(PEEK(AD) OR BT)
2040 RETURN
```

K-1007-1 PARTS LIST

2	74LS00	U4,11
1	74LS10	U6
1	74LS13	U3
4	74LS30	U2,7,9,10
1	74LS42	U1
1	74LS157	U12
2	74LS221	U5
1	LM340T-5	Q1
2	DIODE SIL SIGNAL 1N4001	D1,2
1	CAP ELECT 25V 1000UF RADIAL	C18
2	CAP ELECT 16V 100UF RADIAL	C1,5
1	CAP ELECT 35V 220UF AXIAL	C15
2	CAP POLY 12V 2000PF AXIAL	C2,9
1	CAP TANT 25V 10UF RADIAL	C14
10	CAP Z5U 12V 0.047UF	C3,4,6,7,8,11,12,16,17,20
2	CAP Z5U 12V 0.1UF	C10,13
1	RES 1/4W 5% 47O	R6
1	RES 1/4W 5% 2.2K	R5
2	RES 1/4W 5% 4.7K	R15,16
3	RES 1/4W 5% 10K	R1,4,7
2	RES 1/4W 5% 13K	R10,12
1	RES 1/4W 5% 18K	R8
1	RES 1/4W 5% 22K	R2
1	RES 1/4W 5% 39K	R3
3	TRIMPOT VERTICAL 10K	R9,11,13
1	CONN PC 22/44 .156 SPACING	
1	CONN PC 40/80 .100 SPACING	
1	MTU CABLE, RIBBON 12" 50 WIRE	
1	MTU CABLE, RIBBON 22" 14 WIRE	
1	WIRE #18 AWG STRANDED BROWN	
1	WIRE #20 AWG STRANDED RED	
1	WIRE #20 AWG STRANDED YELLOW	
1	SWITCH SLIDE PC 3 POSITION	S1
1	HEAT SINK 1W TO-220	HQ1
1	PC BOARD K-1007-1	
1	PC BOARD K-1007-2	
1	SCREW STEEL RH 4-40X1/2	
1	NUT STEEL 4-40X1/4	


CAB1
SW1
CAB2
C18
HS1
Q1
R15
D1
D2
R16
U12
C17
R14
U11
C16
C15
C14
C13
R12
U8
C20
R13
R11
R10
C19
C10
R9
R8
C9
U5
R5
C6
R4
C2
U1
U2
R1
U9
C11
U10
C12
U6
C7
U7
C8
R6
C5
R7
U3
C3
U4
C4
R3
R2
C1
Conn1
PC1
1
22