

ZX65: Simulating a Micro

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ABSTRACT

This article gives complete details, including source code, of an assembly language program which functionally simulates the operation of a 6502 microprocessor device using a Z80 based host computer system. Under control of ZX65, a wide variety of 6502 software may be directly executed in any of several modes. Useful for 6502 software development as well as for its tutorial value, ZX65 should prove to be a significant addition to the Z80 user's software library. Occupying only 4K Bytes of system memory, ZX65 is sufficiently flexible to be readily adapted to system environments other than the one described.

Having logged many hours of software development work on my Z80-based system, I recently decided that I was up to a particular challenge: using my system as a development tool for a totally different microprocessor; specifically, the 6502. This decision, I must confess, was not altogether based on a burning lust for knowledge, but rather on a more practical requirement: I had become involved in the development of a 6502-based device, and had no ready access to a 6502 development system. I decided that a simple cross-assembler wasn't good enough, and set out to write a 6502-to-Z80 object code translator/simulator/interpreter.

The program described here, which I have dubbed ZX65, is the result of my efforts to generate a software package to perform this task. It is useful not only for the intended purpose of software development, but also for the rewarding experience of exploring a whole new field of good software written for a processor other than one's own.

ZX65 operates as an interpretive simulator; that is, a simulated 6502 CPU is maintained in system memory, and each encountered 6502 instruction is

decoded and processed interpreter-fashion to properly act upon the simulated CPU registers. The entire package resides in just over 4K Bytes of high system memory, leaving the remaining portion, including the all-important (for 6502) base page, free for program and data storage. Note that CP/M serves only as a loader and is not used thereafter. In fact, while the program loads normally into CP/M's Transient Program Area, it immediately relocates itself into high memory, overlaying both the CCP and the BDOS portions of CP/M. The user I/O linkages (CBIOS), however, remain intact and are used by the package to perform disk and console functions. The functions which must be provided by the system are a subset of those required by CP/M and should thus be readily available. These functions are all accessed via a jump table within the interpreter and thus can be readily changed to accommodate different system requirements (See Table 1). Parameters must be passed to the drivers in register "C" (register pair "BC" for item six) and data, if any, is returned in the accumulator.

ZX65 is referred to as a package since it includes three distinct function groups. The first and largest is the interpreter/simulator itself. The second group is an elementary monitor providing the functions of memory examine and modify. The third group consists of a self-contained, elementary disk operating system (DOS) (Note: ZX65 files are not CP/M compatible). The normal configuration assumes a two-drive system, with the system diskette on drive A, and all internal disk access routed to drive B (Modification for a single drive system could easily be done, requiring the user to switch diskettes after the package is loaded). The package is written in standard Zilog/Mostek source code and is quite heavily commented. Much use is made of the Z80's special instructions and index registers, and operation on an 8080 is definitely not possible without extensive modification. Although the commented listing should guide you through the program's operation without too much trouble, a brief description of the interpreter portion is in order. A study of the small but powerful instruction set of the 6502 will reveal certain

patterns in the op codes, as also occurs with most other processors. The eight "BRANCH ON CONDITION" codes, for example, all have zero as a low-order nybble, while the high-order portion is always an odd value.

Another pattern, not so obvious, is that every instruction having an odd-valued op code uses multiple addressing modes. These and other such patterns are exploited by the program. Even so, much of the code is devoted solely to decoding the op code and transferring control to the proper instruction processor. The code beginning at "STEP" (line 241) performs the initial decoding, and fully decodes certain instructions such as "RTI", "JMP", and a few others. In most cases, decoding proceeds to a point where the instruction is known to be part of a group, such as the branch group described above. In these cases, look-up tables are used, but not always in the same way. The branch group and the flag set/reset group, for example, derive mask patterns from the tables which are used for testing, setting, or resetting the condition flags.

In the case of multiple addressing mode instructions, however, the tables serve an entirely different purpose. The table contents are, in these instances, decoded into addresses for indirect jumps; first to the addressing mode processors, and then to the actual instruction processors. Each processor performs its instruction as required. The "ADC" instruction, as an example, causes a byte of data to be fetched from memory or from the object code, depending on the addressing mode. After setting the Z80 carry flag to match the simulated 6502 carry flag, this data byte is added to the value currently in the simulated accumulator, and the result is stored there. The simulated carry flag is then updated to again match the Z80 carry, and the simulated sign, overflow, and zero flags are set or reset according to the results in the accumulator (In this case, the overflow flag is set or reset according to a logical exclusive "OR" of bits six and seven). Considerable care has been given to treatment of the flags, since Z80 flags and their 6502 namesakes do not always have the same meaning (Case in point: the 6502 carry flag assumes a logical

"NOT" BORROW meaning during subtract and compare operations, while the Z80 and most other common processors invert the carry flag internally during these operations so that it represents a "TRUE" BORROW; other flag differences, for the most part, are more subtle).

Finally, each individual processor is responsible for exiting with codes for the mnemonic, the addressing mode, and the number of bytes occupied by the instruction available for use by the "DISPLAY" routine (line 173) to index into yet another set of tables and retrieve the ASCII messages for mnemonic and addressing modes. Upon exiting the instruction processors, the value stored in "NEXT PROGRAM COUNTER" is updated, and control is passed back to the COMMAND section where the operating mode in effect determines whether to display the updated CPU contents, and whether or not to continue execution with the next instruction.

Several distinct operating modes are available, defined briefly as follows:

Single-Step Mode: One instruction is decoded and executed. The console then displays the address of the instruction just executed (Current Program Counter), the decoded instruction (Mnemonic and Operand), the state of all CPU registers, and the address of the next instruction to be executed (Next Program Counter). Control is then returned to the user.

Multi-Step Trace Mode: The user specifies up to 255 instructions to be executed with the results displayed as above following each step. This occurs at the rate of approximately two instructions per second. Control is returned to the user after the required number of steps have been executed and displayed.

Run-to-Breakpoint Mode: Instructions are executed without display up to and including the user-specified breakpoint. CPU registers are then displayed as above and control is returned to the user.

Free-Run Mode: Instructions are executed with no display and no breakpoints. The console keyboard, however, is monitored, and CPU contents are displayed as above and control is returned to the user at any point upon console input.

The user may examine and modify any or all CPU registers, including the program counter, at any time that he

has control, without otherwise disturbing any operation in progress.

The 6502 "BRK" instruction (software interrupt) is handled through a vector location, just as in a normal system. Optionally, however, the BRK instruction may be used (and is initialized) to return control to the user in the same manner as the breakpoint mode described above. The BRK instruction and breakpoint mode operate independently, and both may be used in the same program. Additionally, up to five different "user" subroutines may be called for transfer of control to Z80 routines (such as console I/O). These are invoked by executing either a "JMP" or "JSR" instruction to addresses 0000, 0001, 0002, 0003, and 0004 (HEX). Control is passed via a jump table located within the interpreter, which the user may load with Z80 "JP" instructions to the desired subroutines. The subroutines must be terminated in the normal Z80 fashion by one of the "RET" instructions. Note that the first two entries in the table (JMP or JSR 0000, 0001 HEX) are initialized as console input and output via the 6502 accumulator. Three parameters may be passed to and from all user subroutines, as outlined in Table 2. Table 3 lists the locations of the BRK vector and the user subroutine jump table.

Although the interpreter is quite versatile and all 6502 instructions are handled properly, there are some limitations to its use. Perhaps the most important of these is that, even in the "free-run" mode, execution is quite slow compared to an actual 6502 running at normal clock speeds. No attempt has been made to correlate execution times with normal 6502 clock periods (this may, in fact, be impossible due to the way in which the system handles multiple addressing modes). Therefore, programs incorporating software timing loops will not execute properly. Also, since the package was intended for software development, hardware interrupts are not supported, and only a limited amount of hardware interfacing can be performed through the "user" subroutine calls.

Two program listings are included here. One, "ZXLD" is located at the end of this article. Its function is to boot the main program from the CP/M Transient Program Area to high memory. The other listing is the interpreter itself, assembled to reside from 6F00 to 7DFF (HEX) in a 32K system.

Note that this leaves 512 bytes, normally containing CBIOS, unaffected. The program is not relocatable, so that in order to run in a different memory configuration, it will be necessary to reassemble the source with a new value in the "SIZE EQU XX" statement. All other addresses are derived from this value. If the object code is to be manually loaded for the 32K system then "ZXLD" must be loaded first, starting at 0100 (HEX). Then start loading ZX65 at 0110 (HEX), continuing until the end. Finally, use the CP/M "SAVE" command (SAVE 15 ZX65.COM) to write the object code to disk. The package can now be invoked by answering "ZX65" to the CP/M prompt. If you are reassembling the package, then you should also reassemble the ZXLD routine (modified for your system) so that you have a .HEX file for each module. Then load the package using DDT as follows:

```
DDT ZXLD.HEX
  IZX65.HEX
  Rdisp
```

Where "disp" is the load offset value required to load the object code from the .HEX file at a different address than that specified. (DDT will calculate "disp" if you type "H1 10, ssss", where "ssss" is the actual starting address of your program. DDT will respond with the sum and difference of the two values, and the difference will be the required value "disp".) Finally, save the object code as directed above for manual loading.

To run the program, place the disk with ZX65.COM on drive A (this disk should also have a copy of CP/M so that the system can be restarted, if necessary, without changing disks). Place the ZX65 data disk on drive B. Start CP/M and invoke ZX65 by answering "ZX65" to the CP/M input prompt. The system will prompt you with a header and a ">" symbol. You are now in the command mode, and typing one of the command codes (see Table 4) will cause the appropriate action to occur. Note that if you are using a disk not previously used for ZX65 on the drive B, you will be unable to use the ZX65 DOS functions until you have initialized the disk. This is done simply by typing "I", at which point the system will ask you to verify this request with a "Y" or "N". The reason for this

(note this well) is that the "I" command clears and initializes the directory on disk B. This is the equivalent of the CP/M command "ERA *.*" and must be used with caution.

For those unwilling to type in a 4K Byte program by hand, I will make the package available on a standard 8 inch IBM format, single side, single density diskette (Sorry, I can't handle any other format!) at a nominal charge of \$15 to cover time and material. Write to me and specify your system memory size. I will send a diskette containing both source and object files assembled to reside in high memory as described above, as well as a copy of ZXLD. A command summary, operating hints, and other general information will be included on the disk.

Finally, although this program has been rather exhaustively tested with a variety of 6502 software (both simple and sophisticated) I cannot guarantee it bug-free. I have included no copyright notices of any kind, and I hope users will feel free to copy, add, delete, and improve at will. (I would like to hear of any major modifications... I may want to include them myself!) As stated at the outset, the package was developed as a side benefit of another project, not as a money maker, and if anyone else finds it useful, so much the better.

Acknowledgments:

CP/M is a registered trademark of Digital Research, Pacific Grove, CA.

While not specifically mentioned in the text, I have relied heavily on the information contained in the book "6502 Assembly Language Programming" by Lance A. Leventhal (Osborne/McGraw-Hill Inc., 1979).

Function	Address
1. Test console input status	7A2EH
2. Get single character from console	7A2BH
3. Send single character to console	7A28H
4. Select disk drive (A or B)	7A34H
5. Home R/W head of selected drive	7A31H
6. Set disk transfer buffer address	7A3DH
7. Set sector number for disk access	7A37H
8. Set track number for disk access	7A3AH
9. Read one sector from selected drive	7A40H
10. Write one sector to selected drive	7A43H

Table 1: Functions which ZX65 requires of the host system, and their locations within the interpreter.

6502 Register Accumulator X Index Y Index	Passed as Z80 Register Accumulator B Register C Register	G I K L M R S T SPACE	Go to 6502 program per Current Program Counter and execute without display (free-run). Initialize a fresh disk on drive B. (Must be formatted.) System will prompt for verification. Kill a ZX65 file on drive B. Similar to CP/M ERA. System will prompt for file name. Load a ZX65 file from disk B. System will prompt for file name. Memory substitution. View sequential memory locations and update if desired. System will prompt for address. Mode will continue in effect until a '.' (period) is typed. Load and run a ZX65 file from disk B, starting at the address specified in the directory. (Must be an executable 6502 program.) System will prompt for file name. Save a ZX65 file on disk B. System will prompt for file name, starting address, and number of bytes. Trace several 6502 instructions with display following each step. System will prompt for desired number of steps. Single-step command. System will execute one 6502 instruction, display the results, and stop.
Table 2: 6502/Z80 Parameter passing for user subroutines.			
Description	Address of vector or jump instruction		
BRK Vector	7A55H		
User 0	7A46H		
User 1	7A49H		
User 2	7A4CH		
User 3	7A4FH		
User 4	7A52H		
Table 3: Locations for 'BRK' vector and user jump table.			
Command	Function		
C	CPU register display and modify.		
D	Directory display of ZX65 files on disk B. Format: FILNAM.TYP LOAD ADDRESS #RECORDS		
E	Examine a block of memory. System will prompt for starting address and number of bytes.		

Table 4: A command summary for ZX65 (in alphabetical order).

LISTING

0001 ; ZX65: SIMULATING A MICRO	1/80 R M KRUSE
0002 ; FOR Z80-BASED SYSTEMS USING THE CP/M DOS	
0003 ; DESIGNED TO REPLACE ALL OF CP/M EXCEPT FOR USERS CBIOS	
0004 ; THRU WHICH DISK AND I/O CALLS ARE MADE	
0005 ; THIS VERSION IS ASSEMBLED FOR A 32K SYSTEM TO CHANGE	
0006 ; TO ANOTHER SIZE. INSERT APPROPRIATE VALUE FOR 'SIZE'	
0007 ; AND RE-ASSEMBLE. SOURCE CODE IS IN PROPER FORMAT FOR	
0008 ; THE S. D. SALES Z80 ASSEMBLER V1.0	
0009 ; PROGRAM MAY BE LOADED BY THE FOLLOWING PROCEDURE.	
0010 ; DDT SYLD HEX	
0011 ; ZX65 HEX	
0012 ; RZ210	
0013 ; GO	
0014 ; SAVE 15 ZX65 COM	
0015 ; THE RES. OPERATOR CAUSES THIS ASSEMBLER TO CLEAR ANY	
0016 ; OVERFLOW IN THE OPERAND FIELD.	
0017 ;	
0018 ;	
0019 ;	
0020 ;	
0021 ;	
0022 ;	
0023 ;	
0024 ;	
0025 ;	
0026 ;	
0027 ;	
0028 ;	
0029 ;	
0030 ;	
0031 ;	
0032 ;	
0033 ;	
0034 ;	
0035 ;	
0036 ;	
0037 ;	
0038 ;	
0039 ;	
0040 ;	
0041 ;	

700E C9	700E C9	POP C9	IX	INSTRUCTION, AND ALL REGISTERS	POP C9	RET	IX
0148	0148	0148	IX	INSTRUCTION, AND ALL REGISTERS	0148	0148	IX
0149	0149	0149	RET	INSTRUCTION, AND ALL REGISTERS	0149	0149	RET
0170	0170	0170	IX	INSTRUCTION, AND ALL REGISTERS	0170	0170	IX
0171	0171	0171	IX	INSTRUCTION, AND ALL REGISTERS	0171	0171	IX
0172	0172	0172	IX	INSTRUCTION, AND ALL REGISTERS	0172	0172	IX
0173	0173	0173	IX	INSTRUCTION, AND ALL REGISTERS	0173	0173	IX
0174	0174	0174	IX	INSTRUCTION, AND ALL REGISTERS	0174	0174	IX
0175	0175	0175	IX	INSTRUCTION, AND ALL REGISTERS	0175	0175	IX
0176	0176	0176	IX	INSTRUCTION, AND ALL REGISTERS	0176	0176	IX
0177	0177	0177	IX	INSTRUCTION, AND ALL REGISTERS	0177	0177	IX
0178	0178	0178	IX	INSTRUCTION, AND ALL REGISTERS	0178	0178	IX
0179	0179	0179	IX	INSTRUCTION, AND ALL REGISTERS	0179	0179	IX
0180	0180	0180	IX	INSTRUCTION, AND ALL REGISTERS	0180	0180	IX
0181	0181	0181	IX	INSTRUCTION, AND ALL REGISTERS	0181	0181	IX
0182	0182	0182	IX	INSTRUCTION, AND ALL REGISTERS	0182	0182	IX
0183	0183	0183	IX	INSTRUCTION, AND ALL REGISTERS	0183	0183	IX
0184	0184	0184	IX	INSTRUCTION, AND ALL REGISTERS	0184	0184	IX
0185	0185	0185	IX	INSTRUCTION, AND ALL REGISTERS	0185	0185	IX
0186	0186	0186	IX	INSTRUCTION, AND ALL REGISTERS	0186	0186	IX
0187	0187	0187	IX	INSTRUCTION, AND ALL REGISTERS	0187	0187	IX
0188	0188	0188	IX	INSTRUCTION, AND ALL REGISTERS	0188	0188	IX
0189	0189	0189	IX	INSTRUCTION, AND ALL REGISTERS	0189	0189	IX
0190	0190	0190	IX	INSTRUCTION, AND ALL REGISTERS	0190	0190	IX
0191	0191	0191	IX	INSTRUCTION, AND ALL REGISTERS	0191	0191	IX
0192	0192	0192	IX	INSTRUCTION, AND ALL REGISTERS	0192	0192	IX
0193	0193	0193	IX	INSTRUCTION, AND ALL REGISTERS	0193	0193	IX
0194	0194	0194	IX	INSTRUCTION, AND ALL REGISTERS	0194	0194	IX
0195	0195	0195	IX	INSTRUCTION, AND ALL REGISTERS	0195	0195	IX
0196	0196	0196	IX	INSTRUCTION, AND ALL REGISTERS	0196	0196	IX
0197	0197	0197	IX	INSTRUCTION, AND ALL REGISTERS	0197	0197	IX
0198	0198	0198	IX	INSTRUCTION, AND ALL REGISTERS	0198	0198	IX
0199	0199	0199	IX	INSTRUCTION, AND ALL REGISTERS	0199	0199	IX
0200	0200	0200	IX	INSTRUCTION, AND ALL REGISTERS	0200	0200	IX
0201	0201	0201	IX	INSTRUCTION, AND ALL REGISTERS	0201	0201	IX
0202	0202	0202	IX	INSTRUCTION, AND ALL REGISTERS	0202	0202	IX
0203	0203	0203	IX	INSTRUCTION, AND ALL REGISTERS	0203	0203	IX
0204	0204	0204	IX	INSTRUCTION, AND ALL REGISTERS	0204	0204	IX
0205	0205	0205	IX	INSTRUCTION, AND ALL REGISTERS	0205	0205	IX
0206	0206	0206	IX	INSTRUCTION, AND ALL REGISTERS	0206	0206	IX
0207	0207	0207	IX	INSTRUCTION, AND ALL REGISTERS	0207	0207	IX
0208	0208	0208	IX	INSTRUCTION, AND ALL REGISTERS	0208	0208	IX
0209	0209	0209	IX	INSTRUCTION, AND ALL REGISTERS	0209	0209	IX
0210	0210	0210	IX	INSTRUCTION, AND ALL REGISTERS	0210	0210	IX
0211	0211	0211	IX	INSTRUCTION, AND ALL REGISTERS	0211	0211	IX
0212	0212	0212	IX	INSTRUCTION, AND ALL REGISTERS	0212	0212	IX
0213	0213	0213	IX	INSTRUCTION, AND ALL REGISTERS	0213	0213	IX
0214	0214	0214	IX	INSTRUCTION, AND ALL REGISTERS	0214	0214	IX</

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70FE B5      0292      OR      L      NZ,BRK1-$
70FF 2007    0293      JR      BC      RET TO CHND
7101 C1      0294      POP      LD      BC,429H
7102 012904  0295      LD      DPLY
7105 C31170  0296      INC      TSPY
7108 23      0297 BRK1  CALL      (1Y+0),L
7109 C00475  0298      LD      INC      SP TO IY
710F FD2B    0299      DEC      (1Y+0),H
7111 FD7500  0300      LD      IV      'PUSH' PC
7114 FD2B    0301      LD      (1Y+0),L
7116 D07E01  0302      DEC      IV      'PUSH' P
7119 FD7700  0303      LD      A,(1X+1)
711C D00D75  0304      DEC      LD      (1Y+0),A
711E C00D75  0305      DEC      IV      'PUSH' P
7121 24557A  0306      TSPY      IY TO SP
7124 012904  0307      LD      GET INTERRUPT VECTOR
7127 C30774  0308      LD      CODE FOR # BYTES & WHEN
              0309      JP      AND FINISH
              0310      ;
              0311      ; PROCESS BRANCHES
              0312      ;
              0313      ; PERMCH      B,0
              0314      LD      C,(HL)
              0315      LD      IY,MSKTEL
              0316      SRL      C
              0317      SRL      C
              0318      SRL      C
              0319      SRL      C
              0320      DEC      C
              0321      ADD      IY,BC
              0322      INC      HL
              0323      BIT      1,C
              0324      LD      A,(1X+1)
              0325      LD      C,(1Y+0)
              0326      LD      B,(1Y+1)
              0327      JR      FLAG MASK
              0328      AND      NZ,BRSET-$
              0329      JR      Z,TRUE-$
              0330      JR      FALSE-$
              0331      AND      B
              0332      BRSET      NZ,TRUE-$
              0333      JR      FALSE-$
              0334      TRUE      LD      D,0
              0335      LD      E,(HL)
              0336      BIT      7,E
              0337      JR      Z,TRUE-$
              0338      DEC      D
              0339      TRUE      ADD      HL,DE
              0340      FALSE      LD      B,0
              0341      JR      END
              0342      ;
              0343      ; PROCESS JUMPS AND JSR JMP 0-4 AND JSR 0-4 GO INTO 780
              0344      ; ROUTINES PER JUMP TABLE AT USRO. CONTROL THEN RETURNS
              0345      ; TO SIMULATOR UPON 780 RET (C9). . ALL OTHERS PROCESSED
              0346      ; NORMALLY.
              0347      ;
              0348      PUSH      INC      HL
              0349      CALL      SCPTST
              0350      JR      NZ,PJS2-$
              0351      CALL      INUSR
              0352      CALL      PJS3-$
              0353      CALL      TSPY
              0354      LD      (1Y+0),H

0292      0355      DEC      (1Y+0),L
0293      0356      LD      LD
0294      0357      DEC      LD
0295      0358      CALL      TSPY
0296      0359      EX      DE,HL
0297 BRK1  0360 PJS3  LD      BC,273H
0298      0361      INC      EN01
0299      0362 PJS3  LD      BC,26FH
0300      0363      INC      HL
0301      0364      JR      DOUP-$
0302      0365 PJS3  LD      BC,26FH
0303      0366      INC      HL
0304      0367      INC      LD      E,(HL)
0305      0368      LD      D,(HL)
0306      0369      EX      DE,HL
0307      0370      LD      BC,006FH
0308      0371 DOUP  CALL      SCPTST
0309      0372      JR      NZ,DOU1-$
0310      0373      PUSH      BC
0311      0374      INUSR
0312      0375      CALL      PRET
0313      0376      POP      BC
0314      0377      EX      DE,HL
0315      0378 DOU1  EX      DE,HL
0316      0379      JP      EN01

0380      0381      ; TEST FOR USER SUBROUTINE CALLS/JUMPS, IF TARGET
0381      0382      ; ADDRESS < 0005 THEN RET WITH Z FLG SET, ELSE CLR
0382      0383      ;
0383      0384 SCPTST LD      E,(HL)
0384      0385      INC      LD      D,(HL)
0385      0386      LD      D,(HL)
0386      0387      INC      LD      A,0
0387      0388      LD      A,0
0388      0389      OR      D
0389      0390      RET      NZ
0390      0391      LD      A,4
0391      0392      CP      E
0392      0393      RET      C
0393      0394      XOR      A
0394      0395      RET
0395      0396      ;
0396      0397      ; INDEX INTO USER SUBROUTINE TABLE
0397      0398      ; PASS A, X, & Y TO/FROM USER ROUTINE AS A, B, & C.
0398      0399      ;
0399      0400      PUSH      BC
0400      0401      LD      D,0
0401      0402      LD      A,E
0402      0403      ADD      A,E
0403      0404      ADD      A,E
0404      0405      LD      E,A
0405      0406      LD      IY,USRO
0406      0407      LD      BC,USRET
0407      0408      PUSH      BC
0408      0409      ADD      IY,DE
0409      0410      LD      A,(1X+0)
0410      0411      LD      B,(1X+2)
0411      0412      LD      C,(1X+3)
0412      0413      JP      (1Y+3)
0413      0414      LD      (1Y+0),A
0414      0415      LD      (1X+2),B
0415      0416      LD      (1X+3),C
0416      0417      POP      BC

7173 FD2B    7174 5E      7144 5E      7145 23      0385      INC      LD      E,(HL)
7175 FD7500  7145 23      7146 56      0386      LD      D,(HL)
7178 FD2B    7146 56      7147 23      0387      INC      LD      D,(HL)
717A C00D75  7147 23      7148 3E00     0388      LD      A,0
717D EB      7148 3E00     0389      OR      D
717E EB      714A B2      0390      RET      NZ
7181 C3D774  714A B2      714B C0      0391      LD      A,4
7184 23      714B C0      714C 3E04     0392      CP      E
7185 016F02  714C 3E04     714E BB      0393      RET      C
7188 1808     714E BB      714F D8      0394      RET
718A 23      714F D8      7180 AF      0395      RET
718B 5E      7180 AF      7181 C9      0396      ;
718C 23      7181 C9      0397      ; INDEX INTO USER SUBROUTINE TABLE
718D 56      0398      ; PASS A, X, & Y TO/FROM USER ROUTINE AS A, B, & C.
718E EB      0399      ;
718F 016F0C   0400      0400      INUSR      0400      PUSH      BC
7192 C04471   0401      71B2 C5      0401      LD      D,0
7193 2009      0402      71B3 1600     0402      LD      A,E
7195 CS      0403      71B5 7B      0403      ADD      A,E
7196 CS      0404      71B6 83      0404      ADD      A,E
7197 CS      0405      71B7 83      0405      LD      E,A
7198 CS      0406      71B8 5F      0406      LD      IY,USRO
7199 CS      0407      71B9 FD21467A 0407      LD      BC,USRET
719A CS      0408      71BD 01CE71   0408      PUSH      BC
719B CS      0409      71C0 C5      0409      ADD      IY,DE
719C CS      0410      71C1 FD19      0410      LD      A,(1X+0)
719D CS      0411      71C3 D07E00     0411      LD      B,(1X+2)
719E CS      0412      71C5 D0602      0412      LD      C,(1X+3)
719F CS      0413      71C6 D04E03     0413      JP      (1Y+3)
71A0 CS      0414      71CC F0E503     0414      LD      (1Y+0),A
71A1 CS      0415      71CE F0E700     0415      LD      (1X+2),B
71A2 CS      0416      71D1 D07700     0416      LD      (1X+3),C
71A3 CS      0417      71D4 D07103     0417      POP      BC
71A4 CS      0418      71D7 C1

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71D8 C9	0418 RET	0419 ; PROCESS SR AND INTERRUPT RETURNS	0420 ;	0421 ;	0422 PRTI	0423 CALL	0424 INC	0425 A, (1Y+0)	0426 PRET1	0427 CALL	0428 LD	0429 PRTS	0430 CALL	0431 PRET	0432 BC, 4A9H	0433 PRTI	0434 INC	0435 IY	0436 LD	0437 IY, (1Y+0)	0438 ;	0439 ; PROCESS SP EXCHANGES	0440 CP	0441 80H	0442 NZ, PTX-#	0443 A, (1X+2)	0444 LD	0445 LD	0446 BC, 4D9H	0447 END	0448 A, (1X+4)	0449 LD	0450 C, 001H	0451 ;	0452 ; PROCESS ALL REMAINING IMPLIED INSTRUCTIONS	0453 ;	0454 PINPL	0455 LD	0456 C, A	0457 SRL	0458 C	0459 SRL	0460 C	0461 AND	0462 OFH	0463 8	0464 IY, IMPTEL	0465 Z, JFIB	0466 LD	0467 IY, IMPTEL+8	0468 ;	0469 ; IMPLIED INSTR PROCESSORS	0470 INC	0471 (1X+2)	0472 INC	0473 C, 65H	0474 LD	0475 IDEFLG-#	0476 INC	0477 (1X+3)	0478 LD	0479 C, 69H	0480 IDEFLG-#	0481 DEC	0482 (1X+2)	0483 LD	0484 C, 59H	0485 IDEFLG-#	0486 LD	0487 (1X+3)	0488 DEC	0489 (1X+4)	0490 LD	0491 C, 59H	0492 IDEFLG-#	0493 RES	0494 1, (1X+1)	0495 NZ, SINTST-#	0496 ;	0497 ;	0498 ;	0499 ;	0500 ;	0501 ;	0502 ;	0503 ;	0504 ;	0505 ;	0506 ;	0507 ;	0508 ;	0509 ;	0510 ;	0511 ;	0512 ;	0513 ;	0514 ;	0515 ;	0516 ;	0517 ;	0518 ;	0519 ;	0520 ;	0521 ;	0522 ;	0523 ;	0524 ;	0525 ;	0526 ;	0527 ;	0528 ;	0529 ;	0530 ;	0531 ;	0532 ;	0533 ;	0534 ;	0535 ;	0536 ;	0537 ;	0538 ;	0539 ;	0540 ;	0541 ;	0542 ;	0543 ;	0544 ;	0545 ;	0546 ;	0547 ;	0548 ;	0549 ;	0550 ;	0551 ;	0552 ;	0553 ;	0554 ;	0555 ;	0556 ;	0557 ;	0558 ;	0559 ;	0560 ;	0561 ;	0562 ;	0563 ;	0564 ;	0565 ;	0566 ;	0567 ;	0568 ;	0569 ;	0570 ;	0571 ;	0572 ;	0573 ;	0574 ;	0575 ;	0576 ;	0577 ;	0578 ;	0579 ;	0580 ;	0581 ;	0582 ;	0583 ;	0584 ;	0585 ;	0586 ;	0587 ;	0588 ;	0589 ;	0590 ;	0591 ;	0592 ;	0593 ;	0594 ;	0595 ;	0596 ;	0597 ;	0598 ;	0599 ;	0600 ;	0601 ;	0602 ;	0603 ;	0604 ;	0605 ;	0606 ;	0607 ;	0608 ;	0609 ;	0610 ;	0611 ;	0612 ;	0613 ;	0614 ;	0615 ;	0616 ;	0617 ;	0618 ;	0619 ;	0620 ;	0621 ;	0622 ;	0623 ;	0624 ;	0625 ;	0626 ;	0627 ;	0628 ;	0629 ;	0630 ;	0631 ;	0632 ;	0633 ;	0634 ;	0635 ;	0636 ;	0637 ;	0638 ;	0639 ;	0640 ;	0641 ;	0642 ;	0643 ;	0644 ;	0645 ;	0646 ;	0647 ;	0648 ;	0649 ;	0650 ;	0651 ;	0652 ;	0653 ;	0654 ;	0655 ;	0656 ;	0657 ;	0658 ;	0659 ;	0660 ;	0661 ;	0662 ;	0663 ;	0664 ;	0665 ;	0666 ;	0667 ;	0668 ;	0669 ;	0670 ;	0671 ;	0672 ;	0673 ;	0674 ;	0675 ;	0676 ;	0677 ;	0678 ;	0679 ;	0680 ;	0681 ;	0682 ;	0683 ;	0684 ;	0685 ;	0686 ;	0687 ;	0688 ;	0689 ;	0690 ;	0691 ;	0692 ;	0693 ;	0694 ;	0695 ;	0696 ;	0697 ;	0698 ;	0699 ;	0700 ;	0701 ;	0702 ;	0703 ;	0704 ;	0705 ;	0706 ;	0707 ;	0708 ;	0709 ;	0710 ;	0711 ;	0712 ;	0713 ;	0714 ;	0715 ;	0716 ;	0717 ;	0718 ;	0719 ;	0720 ;	0721 ;	0722 ;	0723 ;	0724 ;	0725 ;	0726 ;	0727 ;	0728 ;	0729 ;	0730 ;	0731 ;	0732 ;	0733 ;	0734 ;	0735 ;	0736 ;	0737 ;	0738 ;	0739 ;	0740 ;	0741 ;	0742 ;	0743 ;	0744 ;	0745 ;	0746 ;	0747 ;	0748 ;	0749 ;	0750 ;	0751 ;	0752 ;	0753 ;	0754 ;	0755 ;	0756 ;	0757 ;	0758 ;	0759 ;	0760 ;	0761 ;	0762 ;	0763 ;	0764 ;	0765 ;	0766 ;	0767 ;	0768 ;	0769 ;	0770 ;	0771 ;	0772 ;	0773 ;	0774 ;	0775 ;	0776 ;	0777 ;	0778 ;	0779 ;	0780 ;	0781 ;	0782 ;	0783 ;	0784 ;	0785 ;	0786 ;	0787 ;	0788 ;	0789 ;	0790 ;	0791 ;	0792 ;	0793 ;	0794 ;	0795 ;	0796 ;	0797 ;	0798 ;	0799 ;	0800 ;	0801 ;	0802 ;	0803 ;	0804 ;	0805 ;	0806 ;	0807 ;	0808 ;	0809 ;	0810 ;	0811 ;	0812 ;	0813 ;	0814 ;	0815 ;	0816 ;	0817 ;	0818 ;	0819 ;	0820 ;	0821 ;	0822 ;	0823 ;	0824 ;	0825 ;	0826 ;	0827 ;	0828 ;	0829 ;	0830 ;	0831 ;	0832 ;	0833 ;	0834 ;	0835 ;	0836 ;	0837 ;	0838 ;	0839 ;	0840 ;	0841 ;	0842 ;	0843 ;	0844 ;	0845 ;	0846 ;	0847 ;	0848 ;	0849 ;	0850 ;	0851 ;	0852 ;	0853 ;	0854 ;	0855 ;	0856 ;	0857 ;	0858 ;	0859 ;	0860 ;	0861 ;	0862 ;	0863 ;	0864 ;	0865 ;	0866 ;	0867 ;	0868 ;	0869 ;	0870 ;	0871 ;	0872 ;	0873 ;	0874 ;	0875 ;	0876 ;	0877 ;	0878 ;	0879 ;	0880 ;	0881 ;	0882 ;	0883 ;	0884 ;	0885 ;	0886 ;	0887 ;	0888 ;	0889 ;	0890 ;	0891 ;	0892 ;	0893 ;	0894 ;	0895 ;	0896 ;	0897 ;	0898 ;	0899 ;	0900 ;	0901 ;	0902 ;	0903 ;	0904 ;	0905 ;	0906 ;	0907 ;	0908 ;	0909 ;	0910 ;	0911 ;	0912 ;	0913 ;	0914 ;	0915 ;	0916 ;	0917 ;	0918 ;	0919 ;	0920 ;	0921 ;	0922 ;	0923 ;	0924 ;	0925 ;	0926 ;	0927 ;	0928 ;	0929 ;	0930 ;	0931 ;	0932 ;	0933 ;	0934 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;	1507 ;	1508 ;	1509 ;	1510 ;	1511 ;	1512 ;	1513 ;	1514 ;	1515 ;	1516 ;	1517 ;	1518 ;	1519 ;	1520 ;	1521 ;	1522 ;	1523 ;	1524 ;	1525 ;	1526 ;	1527 ;	1528 ;	1529 ;	1530 ;	1531 ;	1532 ;	1533 ;	1534 ;	1535 ;	1536 ;	1537 ;	1538 ;	1539 ;	1540 ;	1541 ;	1542 ;	1543 ;	1544 ;	1545 ;	1546 ;	1547 ;	1548 ;	1549 ;	1550 ;	1551 ;	1552 ;	1553 ;	1554 ;	1555 ;	1556 ;	1557 ;	1558 ;	1559 ;	1560 ;	1561 ;	1562 ;	1563 ;	1564 ;	1565 ;	1566 ;	1567 ;	1568 ;	1569 ;	1570 ;	1571 ;	1572 ;	1573 ;	1574 ;	1575 ;	1576 ;	1577 ;	1578 ;	1579 ;	1580 ;	1581 ;	1582 ;	1583 ;	1584 ;	1585 ;	1586 ;	1587 ;	1588 ;	1589 ;	1590 ;	1591 ;	1592 ;	1593 ;	1594 ;	1595 ;	1596 ;	1597 ;	1598 ;	1599 ;	1600 ;	1601 ;	1602 ;	1603 ;	1604 ;	1605 ;	1606 ;	1607 ;	1608 ;	1609 ;	1610 ;	1611 ;	1612 ;	1613 ;	1614 ;	1615 ;	1616 ;	1617 ;	161
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