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The 6502 and Its Little Brothers

If you haven't met them yet, here are the other members of the 6502 family.

The MCS6502 by MOS Technology is a well-known, popular microprocessor. That it is found in the PET, PAIA, KIM-1, Apple and OSI personal computers guarantees that much will be written about it and much software will be written for it. However, less well known are the other members of the MCS65XX family. Let's see how they compare and what they have to offer.

This article is an overview and not a tutorial (consult the references at the end of the article). The hardware manual, the software manual and the KIM-1 user manual, which retail for $30, are included with the purchase of the KIM-1.

General Features

While all of the members of the family share certain common characteristics, each has its own individual personality. Table 1 is a list of the features possessed by all of them. It has been said that the 6502 is closely related to the MC6800. In fact, it has been claimed by some writers that the 6502 is the second-generation 6800. Whether this is true or not, I'll leave up to the experts to argue.

Look at Table 1 while I elaborate on some of these features. Eight-bit parallel processing and the bidirectional bus are standard in the micro field, and the trend to +5 V dc-only requirements goes a long way toward simplifying power supply design and construction. The READY input allows the use of memory, which is slower than the processor.

Depending on the type of 65XX that is being used, an addressing capability of from 4K to 65K is available, as we shall see. Variations as to processor speed and clock types are also related to 65XX type. The architecture and instruction set allow decimal or binary arithmetic, 13 addressing modes, a programmable stack pointer, direct memory access and maskable or non-maskable interrupts. An output clock is provided for synchronizing the operation of support chips. All nine types recognize the same instruction set, which means that they are completely software compatible.

Specific Types

Table 2 shows the various members of the 65XX family and the features that make each of them unique. Each version is available for operation with either a 1 or 2 MHz clock. The 2 MHz types are suffixed with an "A" (6502A, 6512A, etc.) for identification purposes.

The 6502, 6503, 6504, 6505 and 6506, which operate from an internal clock, are aimed at high-performance/low-cost applications. The 6512, 6513, 6514 and 6515 require an external clock and are intended for multi-processor applications where all of the CPUs must march to the beat of the same drummer. The major differences between the family members relate to their memory-addressing ability and interrupt capabilities.

The 6502 and 6512 come in 40-pin DIPs (dual in-line package), while the rest are packaged in a 28-pin DIP, which does not provide enough pins to support all 16 address lines. This restriction is obviously deliberate, and these limited versions are intended for dedicated controller applications where access to great amounts of memory is not usually needed. What memory is required is usually in ROM or PROM.

Architecture

Fig. 1 is a block diagram of the 65XX internal makeup. The accumulator (A) handles eight bits of data at a time. The eight-bit X and Y registers are used in the indexed addressing modes and can also be used as storage and counting registers during the execution of a program.

The 16-bit Program Counter (PC) can access 65K bytes of memory (with the restrictions on some versions due to the lack of all 16 address leads). The 8-bit programmable Stack Pointer (S) always points to page one (0100 to 01FF hex).

The Processor Status (P) register contains flags that signal the occurrence of special events and can be used to direct conditional branching or

MC6800 compatible
Eight-bit parallel processing
Bidirectional data bus
Requires +5 V dc only
Will wait for slow memory (READY)
Addresses for 4K to 65K of memory
1 or 2 MHz operation
Choice of internal or external clocks
56 instructions
Decimal or binary arithmetic
Thirteen addressing modes
Programmable stack pointer
Direct memory access
Maskable and non-maskable interrupts
Output clock for timing support chips

Table 1. List of the features that are common to all members of the MCS65XX microprocessor family.

Type	Package	Clock	Features
6502	40-pin DIP	Internal	All
6512	40-pin DIP	External	All
6503	28-pin DIP	Internal	Can address 4K—maskable and non-maskable interrupts
6513	28-pin DIP	External	Can address 4K—maskable and non-maskable interrupts
6504	28-pin DIP	Internal	Can address 8K—maskable interrupt
6514	28-pin DIP	External	Can address 8K—maskable interrupt
6505	28-pin DIP	Internal	Can address 4K—maskable interrupt—READY lead
6515	28-pin DIP	External	Can address 4K—maskable interrupt—READY lead
6506	28-pin DIP	Internal	Can address 4K—maskable interrupt—2 phase clock output

Table 2. Features of the individual members of the 65XX microprocessor family. Each would fill certain requirements in a general or dedicated controller application.

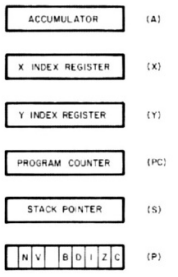

Fig. 1. The six registers contained within the MCS65XX microprocessors. Each is eight bits wide, except the Program Counter (PC), which is a 16-bit register.

indicate processor status. For instance, the Negative (N) flag is set to a 1 whenever the result of an operation is negative. The Branch on Minus (BMI) and Branch on Plus (BPL) use this flag to determine whether or not to branch.

The Zero (Z) flag is set if the result of an operation is zero, otherwise it is reset (0). The Branch on Zero (BEQ) and Branch on not Zero (BNE) instructions pivot on this flag.

The Branch on Overflow Set (BVS) and Branch on Overflow Clear (BVC) use the Overflow (V) flag, and the Branch on Carry Set (BCS) and Branch on Carry Clear (BCC) instructions utilize the Carry (C) flag in a like manner.

The Interrupt Disable (I) flag is set by the programmer (SEI) or the processor when interrupts are undesirable, such as during resets and previous interrupts. The Decimal Mode (D) flag is set by the programmer (SED) when the BCD (binary coded decimal) form of addition or subtraction is desired rather than the binary form.

And finally, the Break Command (B) flag is set by the processor whenever a Break instruction (BRK) has been executed. There is an eighth bit in the Processor Status register that is not being used.

Instruction Set

The 65XX instruction set consists of 56 different types, and since quite a few of these types can take more than one form, there are 146 op codes available to the programmer. Most of these variations have to do with addressing modes. Table 3 is a list of the instruction types, and Table 4 spells out the addressing modes.

This multiplicity of available addressing modes can make the programmer's life easier or harder depending on your point of view. Certainly the zero page, indexed and relative modes make for simpler, shorter code and make it easier to relocate programs due to the lack of a need for absolute addressing in most cases.

The 65XX series are memory-oriented processors as opposed to the 8080 and Z-80, which are register oriented.

ADC	Add memory to Accumulator with carry
AND	"AND" memory with Accumulator
ASL	Shift left one bit
BCC	Branch on Carry clear
BCS	Branch on Carry set
BEQ	Branch on result equal
BIT	Test bits in memory with Accumulator
BMI	Branch on result minus
BNE	Branch on result not zero
BPL	Branch on result plus
BRK	Force break
BVC	Branch on Overflow clear
BVS	Branch on Overflow set
CLC	Clear Carry flag
CLD	Clear decimal mode
CLI	Clear Interrupt disable
CLV	Clear Overflow flag
CMP	Compare memory and Accumulator
CPX	Compare memory and Index X
CPY	Compare memory and Index Y
DEC	Decrement memory
DEX	Decrement Index X
DEY	Decrement Index Y
EOR	"Exclusive OR" memory with Accumulator
INC	Increment memory
INX	Increment Index X
INY	Increment Index Y
JMP	Jump to new location
JSR	Jump to subroutine
LDA	Load Accumulator with memory
LDX	Load Index X with memory
LDY	Load Index Y with memory
LSR	Shift one bit right
NOP	No operation
ORA	"OR" memory with Accumulator
PHA	Push Accumulator on Stack
PHP	Push Process Status on stack
PLA	Pull Accumulator from Stack
PLP	Pull Process Status from stack
ROL	Rotate one bit left
ROR	Rotate one bit right
RTI	Return from interrupt
RTS	Return from subroutine
SBC	Subtract memory from Accumulator with borrow
SEC	Set Carry flag
SED	Set decimal mode
SEI	Set interrupt disable
STA	Store Accumulator in memory
STX	Store Index X in memory
STY	Store index Y in memory
TAX	Transfer Accumulator to Index X
TAY	Transfer Accumulator to Index Y
TSX	Transfer Stack Pointer to Index X
TXA	Transfer Index to Accumulator
TXS	Transfer Index X to Stack Pointer
TYA	Transfer Index Y to Accumulator

Table 3. Mnemonics and descriptions for the 65XX instruction set.

Accumulator
Immediate
Absolute
Zero Page
Indexed Zero Page
Indexed Absolute
Implied
Relative
Indexed Indirect
Indirect Indexed
Absolute Indirect

Table 4. Addressing modes available to the 65XX programmer. Since these are complex, I suggest the MOS Technology Programming Manual for a thorough explanation.

This means that most instruction results must be stored in memory, as in the 6800. The 8080 and Z-80 store most results in internal registers. Also, like the 6800, the 65XX has no specific provision for I/O addressing. I/O locations are handled exactly the same as memory locations. Therefore, any instruction that relates to memory operations will do the same for I/O.

Applications

The 65XX CPU family was designed with many different applications in mind. As I mentioned earlier, many general-purpose personal computers use the 6502. However, each member of the family is seeking its own little niche.

One computer that uses the 6503 is the PAIA 8700. The 8700 is designed to interface with a music synthesizer, but many control applications are certainly possible. More and more of the latest peripherals, such as floppy-disk interfaces, high-speed printers, etc., contain a dedicated controller . . . not to mention the kitchen ranges, washers, dryers, clocks and cars that have them now and the many more home appliances that will in the near future.

How about a subordinate processor with limited memory that acts as a printer buffer. Instead of your main CPU dumping one character at a time to the printer using the printer's time frame (slow!), why not dump a 256- or 512-byte block on the subordinate CPU to un-

MCS6520

Compatibility with MCS65XX microprocessors
Two 8-bit bidirectional ports
Two programmable Data Direction Registers
Four individually controlled Interrupt input lines
Two peripheral control lines
Handshake logic for input and output peripheral control
Tri-state input/output lines
8-bit bidirectional Data bus
Two programmable Control Registers
Program controlled interrupt capability

MCS6530

Compatibility with MCS65XX microprocessors
Two 8-bit bidirectional ports
Two programmable Data Direction Registers
1024 × 8 bit ROM
64 × 8 bit static RAM
Programmable Interval Timer
Programmable Interval Timer interrupt
TTL- and CMOS-compatible input/output lines
Tri-state input/output lines
8-bit bidirectional Data bus

Table 5. Features of the MCS6520 peripheral interface device and the MCS6530 peripheral interface-memory-timer device.

load on the printer. When that has been printed, an interrupt can signal the need for a new block. Meanwhile, the main CPU is handling other tasks. CPU prices have come down to the point where this is a feasible consideration.

Maybe you would consider an auxiliary CPU-driven real-time clock that is ready with the time whenever your programs need it without the need for the main CPU to be continually interrupted to update that clock.

You receive a bonus if your main and subordinate CPUs belong to the same family. You can use the assemblers, text editors, etc., on your big system to write programs for little brother. This is helpful since most of the controller-type applications don't allow elaborate keyboards, video terminals, etc. So you write your subordinate control software using the big gun, load it into RAM or burn it into PROM and free the big machine for the complex tasks.

A computer music system in which the music is composed on the big machine and played by the little one is another possibility. The main machine would contain the software that generated the code that the subordinate CPU executed.

Peripherals

There are two other members of this family that we haven't mentioned yet—the MCS6520 and 6530. The MCS6520 is a peripheral interface device and the MCS6530 is a peripheral interface-memory-timer device. Table 5 shows their features.

The 6520, which is pin-for-pin compatible with the MC6820 PIA (peripheral interface adapter), contains two eight-bit bidirectional parallel ports and four interrupt lines. Two of these lines can also be used as peripheral control lines.

The 6530 also contains two eight-bit bidirectional parallel ports but has other features as well. These include 1024 × 8 bit ROM, 64 × 8 bit RAM and a programmable interval timer that has the ability to interrupt the CPU or not as desired.

Two 6530s are utilized in the KIM-1. They provide the ROM operating system, RAM scratchpad, two timers and four ports. Two of the ports, one timer and part of the RAM are used by the operating system, leaving the rest for the programmer's use.

Conclusion

Early MOS Technology literature (1975) describes the MCS 6501 as a pin-for-pin replacement for the MC6800. For some reason, later data sheets omit the 6501.

Programmers familiar with the 6800 will feel at home with the MCS65XX, while the 8080 aficionado will face a whole new way of doing things. Most noticeable to the latter will be the lack of numerous registers that he used to use for storing, pointing and counting. He will also notice all of the extra addressing modes that the 65XX series possesses. The Z-80 contains some of both worlds.

MOS Technology has attempted to take the basic architecture of the MCS6502 and repackage it to fit various requirements. Have they been successful in this attempt? Only the end-user can answer that. ■

References

MOS Technology, 950 Rittenhouse Rd., Norristown PA 19401: *MCS6500 Programming Manual, MCS6500 Hardware Manual, KIM-1 User Manual, MCS6500 MPU Data Sheet, MCS6520 and MCS6530 Data Sheets* and *MCS6500 Instruction Set Summary Card.*

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PAIA Electronics, 1020 W. Wilshire Blvd., Oklahoma City OK 73116: *PAIA 8700 Computer/Controller Assembly and Using Manual.*

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