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Super-Tube

... jazzing up the Digital Group TVT

This article describes how a basic commercially available microprocessor kit can be enhanced with features normally found on more sophisticated minicomputer systems. The following enhancement features, although designed for "The Digital Group" TV display[1], can be applied with appropriate modifications to any similarly designed 7-bit ASCII TV display.

1. Full screen editing with characters entered, changed, and viewed on the screen.
2. Any character string can be read back into main memory from character storage.
3. Ability to display a 16-character graphic set.
4. Normal typewriter RETURN function.
5. Cursor movement up or down to any row without altering column location.
6. Cursor can be moved left or right to any column without changing the row location.
7. Ability to darken screen and/or cursor under program control.
8. Ability to read or write screen 0 (addresses 0-511) or screen 1 (addresses 512-1023) under program control; allows graphics on screen 1 to be viewed simultaneously with characters on screen 0.
9. Ability to start loading the character memory with any character and then, while awaiting END LOAD interrupt, let the CPU execute another task. When the loading is complete (about 16 ms), the character memory is reset to address 0 and the CPU is INTERRUPTED.

Before proceeding, the reader should understand the method by which the modifications are made. No printed circuit patterns have to be cut, nor are any connections made directly to any ICs. Whenever mention is made to *cutting* a connection to an IC pin, the cutting is done by inserting another *low profile* socket between the installed board IC socket and the IC, as shown in Fig. 1. The pin connection that is to be cut, is bent outwards before the extra socket is installed. Connections that are required are then made to this bent-out pin and to the now *open* land pattern.

The format of these articles is directed primarily toward *How To Do It* rather than the intimate design details that are always required to determine *Why*.

Note that there are places in the logic that appear as *inefficient* or *cumbersome* design; I'm aware of this. They came about due to the fact that as new features were added no attempt was made to rewire old logic to achieve optimized design.

Cursor Generation

A cursor is an indication of the position of the next character location to be changed on the screen. The change may be either to replace an existing character with a blank or to enter a new character. The cursor is illuminated and blanked under control of the MPU. The cursor is generated by essentially comparing the current scanning display address with the current character memory address and when they are equal generating a cursor pulse to brighten the screen. The address equal comparison is accomplished via three 4-bit comparators — ICC, ICD, and ICE. The trailing edge of the equal compare, ANDed with the bottom line and the cursor blinker via ICA, is applied to the cursor generator SS, ICB. This one-character delay is required to place the cursor under the next character to be changed. The cursor will be illuminated, in a blinking mode, if the program controlled blinker control is a logical 1 at pin *9*. (Refer to Fig. 2.)

Nondestructive Cursor Movement

The original logic connection of the character address registers was count-up only; the count-down connection (pin 4 of IC16) was connected to +5. The count signal applied to pin 5 changed from logical 0 to 1 to 0 during strobe time.

Address change, before character storage time (character storage is delayed 600us by IC23 pin 13) is affected on the leading edge (0 to 1) for the strobe pulse. In order to move the cursor both left and right, both count-up and count-down must be done. According to the module specs, the count direction that is not being executed must be at a logical 1. Since, as mentioned above, the current count-up signal goes from 0 to 1 to 0, this signal must be inverted to 1 to 0 to 1 to be able to execute the count-down. When this is done, however, the address advance is executed after, not

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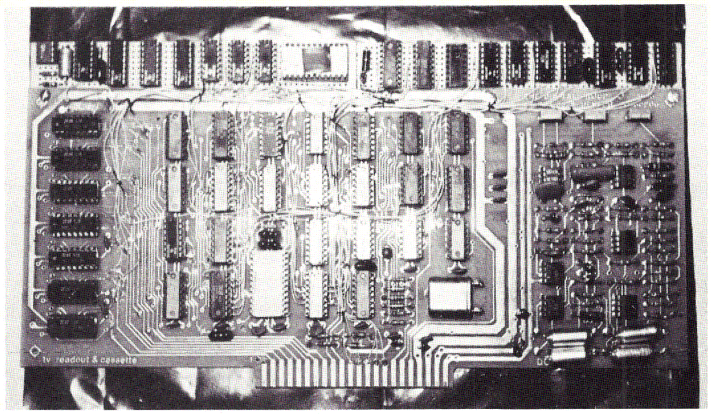
[1] *Byte*, August 1976.



Sockets are low profile obtained from Digikey Corp. *Note:* Solder tab type must be used for intermediate sockets.

ICA	ICB	ICC	ICD	ICE	ICF	ICG	ICH	IC JK	ICL	ICM	ICO	ICP	ICQ	ICR	ICS	ICT	ICU
NE555	74121	74157	74157	74157	74L04	74L04	74L04	1702A	74157	74157	74193	7474	7404	7402	74123	7402	7400

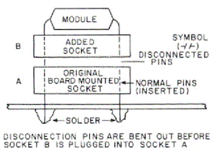


Fig. 1. Module Modification.

before, character storage. Therefore, address initialization must be to location 0, not 511, as in the original design.

This was done as shown in Fig. 3. With no cursor movements, both pins 4 and 5 are at +5. Application of either a left or right cursor movement changes the appropriate pin from a 1 to a 0 and back to a 1. Reset to location 0 will be described in the section on screen initialization.

Nondestructive UP/DOWN cursor movement, row change with no column change, is complicated by the fact that the column count (32) extends 1 bit into IC29 and requires no change, while the row count that must be changed, takes up the remainder of IC29.

During the UP/DOWN cursor movement, IC16 is not changed. Instead of incrementing/decrementing IC29, ICO keeps the count and is

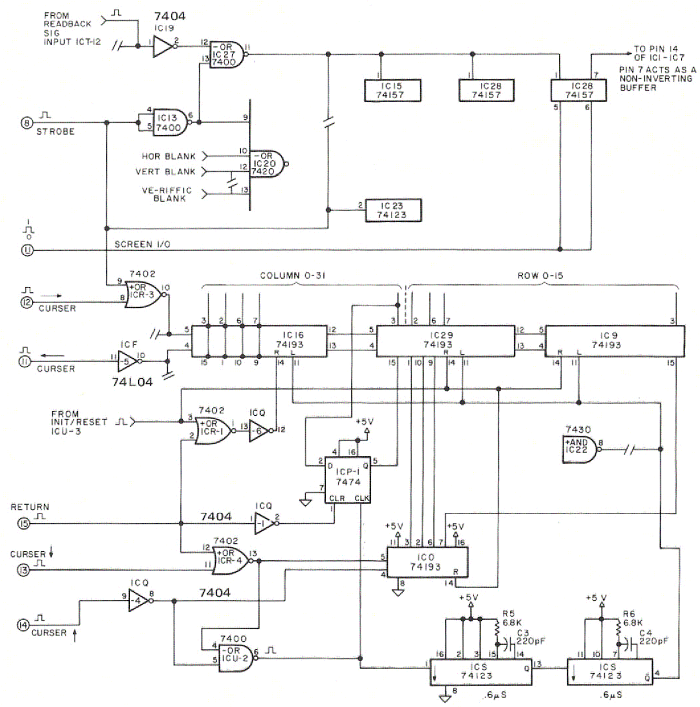


Fig. 2. Advance, cursor and blanking logic.

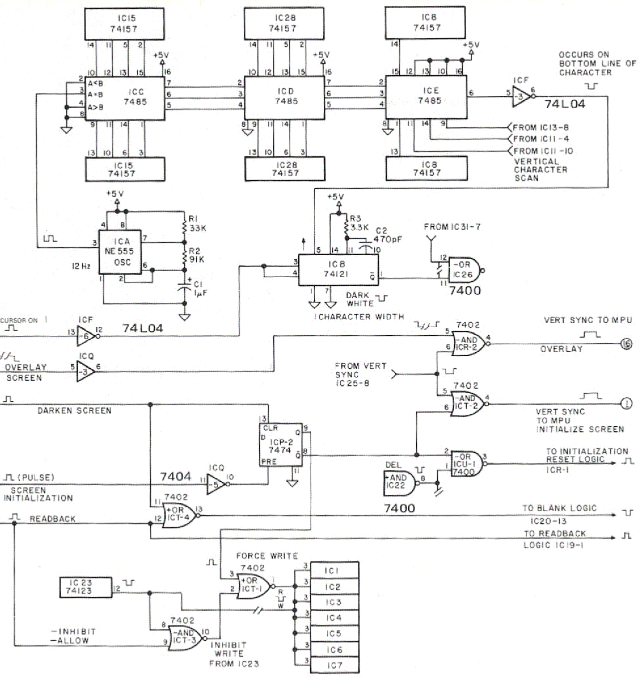


Fig. 3. Cursor generation and screen control logic.

incremented/decremented and then, 600us later, is loaded into IC29. In the absence of RETURN, ICP-5, the noninverted output is also loaded back into IC29. Therefore, IC29 bit one is not changed during UP/DOWN cursor movement.

Return is slightly different. During RETURN, the COLUMN value must be zeroed at the same time the row value must be incremented. Reset of bits 0-3 is accomplished via ICQ-11. The same loading process previously described is applied to IC29 and IC9. In this case, however, bit one of IC29 must be zeroed. This is a two-step operation. When the RETURN line is raised, ICP is reset. The leading edge of the return pulse is also applied to the clock input of ICP. Any attempt to *set* ICP by the leading edge of RETURN is overridden by the remainder of the clear pulse. Thus bit one of IC29 is always loaded as a 0 during return.

External Screen Control

This modification provides the following additional features: screen darkening, darkening of the screen during character readback, and initialization of screen to any desired character.

Screen control is applied via pin *12*. A 0 is bright and a 1 is dark. This control signal is applied via +OR ICI to IC20-13. Pin 13, separated from pin 12, provides the -OR entry to the blanking logic. (Refer to Fig. 2.)

The screen is also darkened during character readback by applying the positive readback control signal to the other input of +OR ICI.

Initialization of the screen is accomplished by a combination of software and hardware control as follows: First the screen is darkened by a 1 applied to pin *12*: this also preconditions ICP, the initialization control BIT register. Second, a positive pulse at pin *13* sets ICP. The output of ICP:

- forces a continous *write* to the character memory, thus permitting the video scanning registers IC32, IC17, and IC10 to write the selected character into every position;
- holds the character registers IC16, IC29, and IC9 in a reset condition via ICU-3;
- Permits the 3 msec vertical sync pulses to become active on pin *1* via ICI-4. The second of such pulses to arrive at the CPU is an indication that the initialization is complete.

When initialization is complete, the darkening signal at pin *12* is removed, lighting the screen and resetting ICP.

Screen Swapping

After assembly, only 512 positions of the 1024 possible positions of the character memory are used. Unfortunately, pin 14, the MSB is connected to ground under each module socket, this forcing a 0-511 address range. In this one case only, instead of breaking the connection to pin 14 by inserting an intermediate module with pin 14 bent out, it was more expedient to break the printed circuit pattern that connects all the pin 14s to ground near IC8 pin 8 and reconnect this common lead to IC8 pin 7. Pins 6 and 5 (both A and B) inputs to IC8 are connected to socket pin *11*. This makes IC8 look like a noninverting buffer. When edge connector pin *11* is at 0, screen addresses 0-511 are enabled; when a 1, screen addresses 512-1023 are enabled. (Refer to Figs. 3 and 4.)

Readback

Readback (see Figs. 2 and 3) of character strings from the character memory ICI-IC7 is accomplished by:

- forcing IC23 into a READ-ONLY mode;
- darkening the screen so that the character being read back does not show on the screen;
- forcing the memory addressing (via IC15, IC28, and IC8) to the character address registers;
- issuing, from the MPU, a series of either left or right cursor instructions followed immediately by a read port instruction to get the character being addressed back to the MPU. *Note*: If a backwards cursor movement is desired, a single dummy back movement must be issued since the cursor is positioned to the

NEXT, rather than the current, character location.

Forced inhibit write (from IC23) is accomplished by applying a continuous positive READBACK pulse (pin *15*) to pin 9 of ICT Fig. 2. Forced character register addressing of character storage is done by applying the continuous positive readback pulse, via IC19-1 and IC27-11 (Fig. 3) to the two-way switches IC15, IC28, and IC8.

The data outputs are read from low-loading inverters ICF, ICG, and ICH. The screen is blanked, via ICT-13 to prevent the TV beam, which is continually scanning, from displaying a full screen of the readback character.

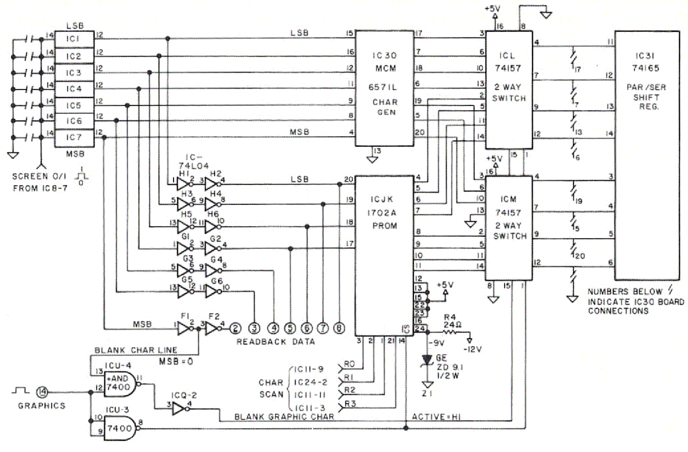


Fig. 4. Graphics generation and logic.

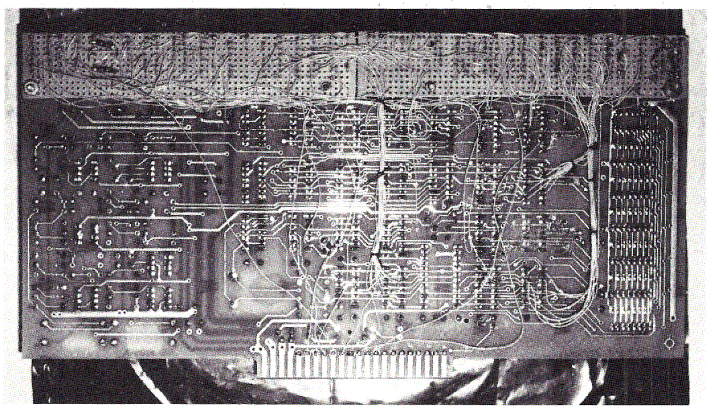
Graphics Modification

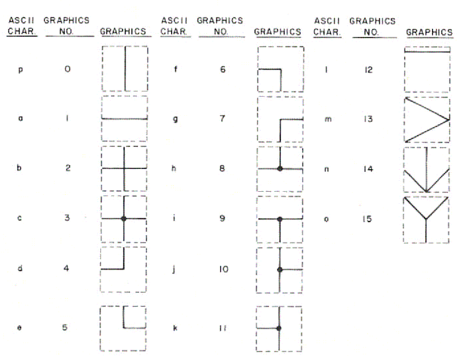
The fixed set of 16 graphics characters was implemented by paralleling the character memory to character generator data/address bus with a 1702A PROM graphic character generator ICJK. The graphics character set is detailed in Fig. 5 and Table 2. Since all 16 graphics characters were used in the PROM, a *blank* character was generated by using the MSB from the character memory IC1-IC7 via ICU-4. When MSB=0, a blank graphics character will be generated. Refer to Table 3 for an ASCII character set. Selection of which generator feeds the parallel to serial converter (IC31) is done by a signal applied to ICU via pin *14*. For minimization of power consumption, the 1702A is only gated on during graphics selection. (Refer to Fig. 4.)

Since only four of the seven output bits/characters are required, the other three can be used for color or *gray* scale control.

Construction

The 19 modules were mounted, as seen in the photograph, on 2 pieces of 1.125" x 6" perforated board, 0.100 x 0.100 C-C holes, attached to the top of The Digital Group TV display





Note: A blank can be obtained by using any character in the first 4 columns (MSB=0) of the character set shown in Table 2.

Only lower case entries are shown in Fig. 5 as they are easiest to enter. Refer to the ASCII chart for equivalents.

Fig. 5. Graphics characters.

The first digit of the address (in hex) is the graphics number (note 10-15 decimal = A-F hexadecimal).

Note: *the pattern is coded backwards with -F being the first address scanned during display of any character.*

HEX ADDR	HEX DATA	HEX ADDR	HEX DATA	HEX ADDR	HEX DATA	HEX ADDR	HEX DATA
00	00	40	00	80	00	C0	00
01	00	41	00	81	00	C1	00
02	00	42	00	82	00	C2	00
03	10	43	00	83	00	C3	00
04	10	44	00	84	00	C4	00
05	10	45	00	85	00	C5	00
06	10	46	00	86	00	C6	00
07	10	47	00	87	00	C7	00
08	10	48	00	88	00	C8	00
09	10	49	F0	89	FF	C9	00
0A	10	4A	10	8A	38	CA	00
0B	10	4B	10	8B	10	CB	00
0C	10	4C	10	8C	10	CC	00
0D	10	4D	10	8D	10	CD	00
0E	10	4E	10	8E	10	CE	00
0F	10	4F	10	8F	10	CF	FF
10	00	50	00	90	00	D0	00
11	00	51	00	91	00	D1	00
12	00	52	00	92	00	D2	00
13	00	53	00	93	10	D3	40
14	00	54	00	94	10	D4	20
15	00	55	00	95	10	D5	10
16	00	56	00	96	10	D6	08
17	00	57	00	97	10	D7	04
18	00	58	00	98	38	D8	02
19	FF	59	1F	99	FF	D9	01
1A	00	5A	10	9A	00	DA	02
1B	00	5B	10	9B	00	DB	04
1C	00	5C	10	9C	00	DC	08
1D	00	5D	10	9D	00	DD	10
1E	00	5E	10	9E	00	DE	20
1F	00	5F	10	9F	00	DF	40
20	00	60	00	A0	00	E0	00
21	00	61	00	A1	00	E1	00
22	00	62	00	A2	00	E2	00
23	10	63	10	A3	10	E3	10
24	10	64	10	A4	10	E4	38
25	10	65	10	A5	10	E5	54
26	10	66	10	A6	10	E6	92
27	10	67	10	A7	10	E7	10
28	10	68	10	A8	18	E8	10
29	FF	69	F0	A9	1F	E9	10
2A	10	6A	00	AA	18	EA	10
2B	10	6B	00	AB	10	EB	10
2C	10	6C	00	AC	10	EC	10
2D	10	6D	00	AD	10	ED	10
2E	10	6E	00	AE	10	EE	10
2F	10	6F	00	AF	10	EE	10
30	00	70	00	B0	00	F0	00
31	00	71	00	B1	00	F1	00
32	00	72	00	B2	00	F2	00
33	10	73	00	B3	10	F3	10
34	10	74	00	B4	10	F4	10
35	10	75	00	B5	10	F5	10
36	10	76	00	B6	10	F6	10
37	10	77	00	B7	10	F7	10
38	38	78	00	B8	30	F8	10
39	FF	79	1F	B9	F0	F9	10
3A	38	7A	00	BA	30	FA	10
3B	10	7B	00	BB	10	FB	10
3C	10	7C	00	BC	10	FC	10
3D	10	7D	00	BD	10	FD	28
3E	10	7E	00	BE	10	FE	44
3F	10	7F	00	BF	10	FF	82

Table 2. 1702A PROM Code for Graphics

card; connection was by handwiring. There are two places where the 4-40 flat head bolts pass through the ground bus. In order to keep ground bus continuity, the bolt heads were soldered to the ground bus.

There is one place where a signal bus must be scraped away and a jumper placed around the opening, clearing the perforated boards.

Cost

The cost for the parts is shown in Table 4. Total not counting PROM programming* — roughly $40.

Conclusion

The enhancements described in this article open the door to sophisticated applications of microprocessor video displays never before possible. A follow-on article will describe one such application now under development.■

* There are advertisements in Kilobaud and 73 for PROM programming services.

Bit Positions				HEX	0	1	2	3	4	5	6	7
				7	0	0	0	0	1	1	1	1
				6	0	0	1	1	0	0	1	1
				5	0	1	0	1	0	1	0	1
4	**3**	**2**	**1**	**HEX**								
0	0	0	0	0	NUL	DLE	SP	0	@	P	'	p
0	0	0	1	1	SOH	DC1	!	1	A	Q	a	q
0	0	1	0	2	STX	DC2	"	2	B	R	b	r
0	0	1	1	3	ETX	DC3	#	3	C	S	c	s
0	1	0	0	4	EOT	DC4	$	4	D	T	d	t
0	1	0	1	5	ENQ	NAK	%	5	E	U	e	u
0	1	1	0	6	ACK	SYN	&	6	F	V	f	v
0	1	1	1	7	BEL	ETB	'	7	G	W	g	w
1	0	0	0	8	BS	CAN	(	8	H	X	h	x
1	0	0	1	9	HT	EM	)	9	I	Y	i	y
1	0	1	0	A	LF	SUB	*	:	J	Z	j	z
1	0	1	1	B	VT	ESC	+	;	K	[	k	{
1	1	0	0	C	FF	FS	,	<	L		1	|
1	1	0	1	D	CR	GS	-	=	M	]	m	}
1	1	1	0	E	SO	RS	.	>	N		n	~
1	1	1	1	F	SI	US	/	?	O	—	o	DEL

MSB 7 6 5 4 3 2 1 LSB

Table 3. United States of America Standard Code for Information Exchange (USASCII).

17 Modules (average $1.00)	$17.00
26 Sockets (average $ .20)	5.20
1 1702A (average $7.50)	7.50
1 1702A Socket	.60
Miscellaneous discrete components	5.00
	$35.30

Table 4. Approximate cost for parts.

POSITIVE PULSE SIGNALS	PIN
Cursor Left	11
Cursor Right	12
Cursor Up	13
Cursor Down	14
Return	15
Screen Initialization	*13*

POSITIVE STEADY STATE LEVELS	PIN
Cursor on	*9*
Screen 0/1 Control	*11*
Darken Screen/Reset Initialization	*12*
Graphics	*14*
Readback	*15*
Overlay Screen Control	*17*

SUMMARY OF ATTENTION SIGNALS FROM TV DISPLAY	PIN
Overlay (bottom of screen)	*16*
Screen Initialization (bottom of screen)	*1*

Note: For efficiency of programming, pulse and steady state signals should be on separate CPU output groups.

Table 1 — Summary of Control Signals to TV Display