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Super Cheap 2708 Programmer

The advantages of programming your own 2708s are many. This easy to build programmer enables you to do the job—inexpensively.

As a KIM owner, I have spent many enjoyable hours running and programming my micro. But as I wrote more programs, I noticed that some of the subroutines were used over and over in different programs. I began looking for a suitable PROM on which to store them. The price and availability of the Intel 2708 PROM were attractive, so I looked for a programmer. Since there were no 2708 programmers compatible with KIM, I sat down, equipped with the *Intel Memory Design Handbook*, a prototyping board and some components, and made one.

Software

In theory, the 2708 PROM has a few simple requirements for entering data. A blank or erased 2708 has all bits in the high, or 1, state. Information is entered by selectively programming 0s into the desired locations. To enter data, the $\overline{CS}$/WE pin is raised to +12 volts to put the chip into the programming mode, the address of the word is selected and the data word is presented to the data pins.

After the data has settled (10^{-6} sec.), a programming pulse of +26 volts at 20 mA is applied to the programming pin. The next address is then selected and the process continued until all addresses have been programmed. This is defined as one programming loop.

To determine the number of programming loops required to ensure valid data entry, use the following formula: N x t_{PW} greater than 100 msec, where N is the number of programming loops, t_{PW} is the programming pulse width and can be varied from 0.1 to 1.0 msec. For rapid programming, t_{PW} should approach one msec. This then requires 100 programming loops; the time required for complete

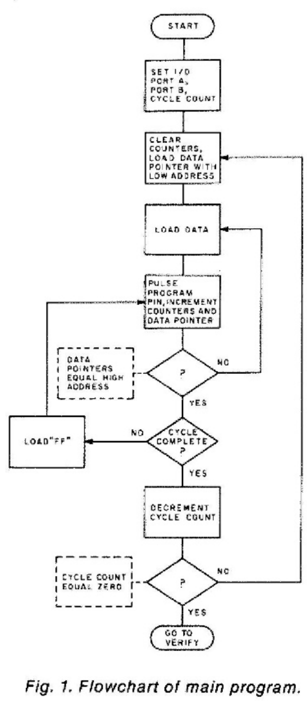


Fig. 1. Flowchart of main program.

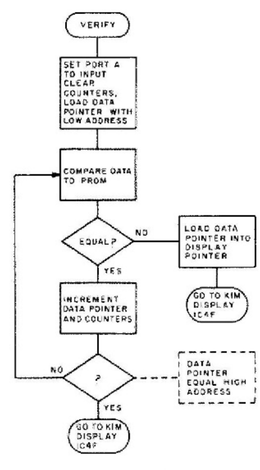


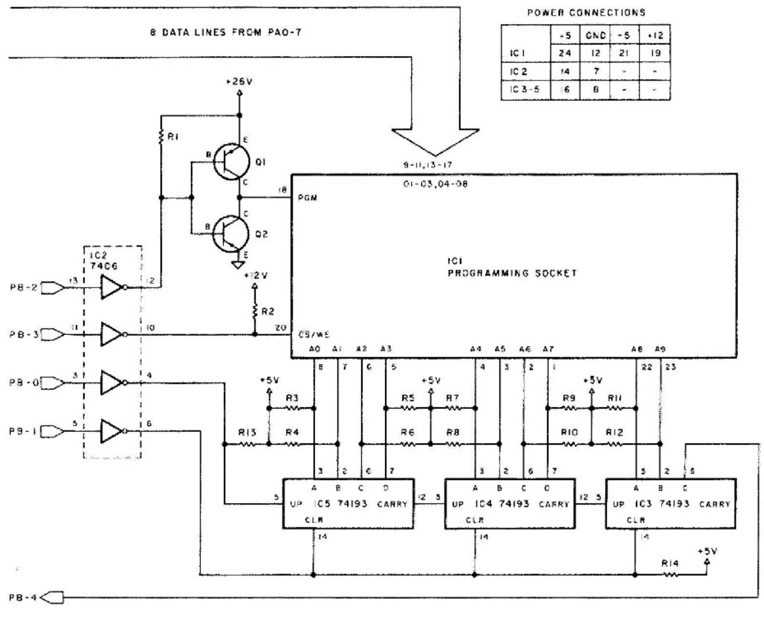
Fig. 2. Flowchart of verify program.

programming of 1K bytes is 1024 addresses times 1.0 msec times 100 programming loops, or about 103 seconds.

For KIM to perform the programming, it must control ten address lines, eight data lines, $\overline{CS}$/WE and programming pins. To do this directly KIM would have to be able to latch 20 I/O lines, but since the addresses are stepped through sequentially and completely, counters can be used to provide the address. Then KIM can use two lines to control the counters and a third to sense the end of the programming loop.

Since KIM has 15 I/O lines, this is perfectly adequate. The counters selected were 74193s because their pin-out gives a simple PC board layout; but any binary counter could be used.

The I/O port is connected to the up-count, the clear and the output of the 11th counting stage. The program pulses the clear, then toggles the up-



	-5	GND	-5	+12
IC 1	24	12	21	19
IC 2	14	7	-	-
IC 3-5	16	8	-	-

Fig. 3. Schematic diagram of programmer.

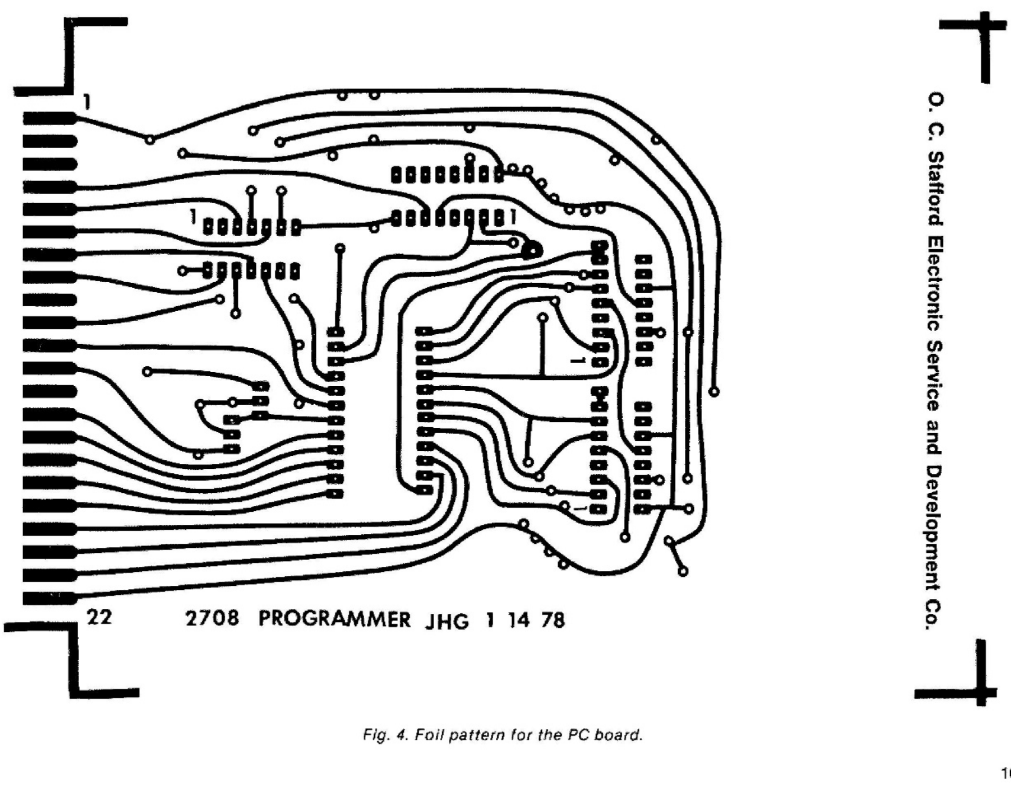


Fig. 4. Foil pattern for the PC board.

Model	Power Rating	Time of Exposure
S-68	12000uW/cm²	10 min.
S-52	12000uW/cm²	10 min.
UVS-54	5700uW/cm²	30 min.
R-52	13000uW/cm²	10 min.
UVS-11	5500uW/cm²	30 min.

All exposures are at a distance of one inch with the filter removed.

Table 1. Exposure guide for Ultra-Violet Products lamp. (Ultra-Violet Products, Inc., 5114 Walnut Grove Ave., San Gabriel CA.)

count and tests the 11th stage output. When the end of the programming loop is detected, the counters are cleared and

	Programmer
1	GND and KIM A-1
2	N.C.
3	N.C.
4	KIM A-13
5	KIM A-9
6	KIM A-10
7	KIM A-12
8	KIM A-11
9	N.C.
10	-5 volts
11	+12 volts
12	+26 volts
13	N.C.
14	KIM A-8
15	KIM A-7
16	KIM A-6
17	KIM A-5
18	KIM A-2
19	KIM A-3
20	KIM A-4
21	KIM A-14
22	+5 volts

Table 2. Connector assignments.

the cycle register, 00EE, is decremented (Fig. 1 is a flowchart of this main program).

To control the $\overline{CS}$/WE and programming pins, the lines are buffered with a 7406 (hex inverter with 30 volt open collectors). The programming pin requires a source of 26 volts at 20 mA and a sink of 1 to 2 mA, so push-pull transistors were used to control the actual input to the programming pin.

The program (listed in Program A) uses 00E7 through 00EE as address and counting registers on page zero and it occupies an additional 184 bytes of memory—either RAM or ROM. As written, it occupies page zero, which permits any RAM over 0200 as the source of data. It exits to the KIM monitor at 1C4F.

The body of the program consists of: an initialization routine that sets up the I/O ports, data pointer and cycle count; presentation of the data word and programming pulse; incrementing the counters and data pointer; testing for last data entry; testing for complete programming loop; and testing for end of programming.

When programming is completed, the routine jumps to a verify loop that compares the PROM contents to the data (see flowchart in Fig. 2). When the number of data words is less than 1024, the program enters FF into the remaining addresses. This permits additional entries to be made at a later date.

During verification, if an error is detected, the program jumps to the KIM monitor and displays the address of the error. Complete programming takes just under two minutes. Additional data can be entered into addresses containing FF, but all previous data must also be entered. All addresses must be programmed during each programming cycle.

The 2708 PROM can be erased by exposure to ultraviolet light at a wavelength of 2537 Å. The recommended dosage is 10 Watt-seconds per square centimeter. This can be determined by a UV meter or by following the exposures given in Table 1.

Hardware

A schematic of the programmer is shown in Fig. 3. The layout shown in Figs. 4 and 5 is a minimum hardware layout using a single-sided PC board

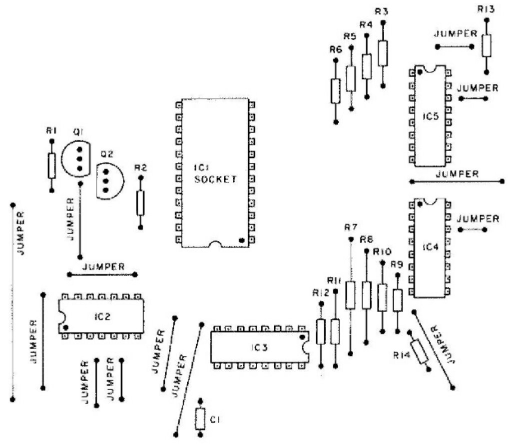


Fig. 5. Component placement.

IC1	2708 socket
IC2	7406 hex inverter (O.C.)
IC3-IC5	74193 binary counter
R1-R14	4.7k Ohm ¼W resistor
C1	0.1 uF capacitor
Q1	2N222 or 2N3904
Q2	2N3906

Table 3. Parts list.

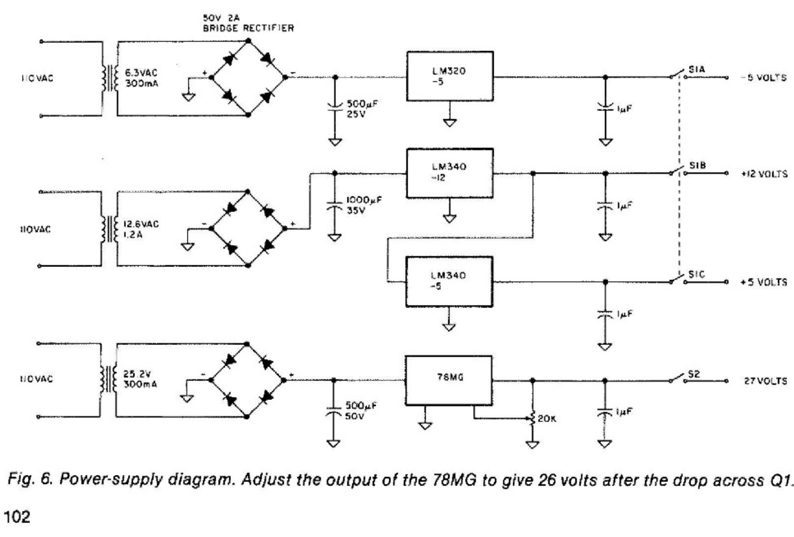


Fig. 6. Power-supply diagram. Adjust the output of the 78MG to give 26 volts after the drop across Q1.

with jumpers. It connects to the application connector supplied with KIM and the power supply. KIM's peripheral port A supplies the data to be entered; port B is used to control the counters and programming lines.

PB-0 is used to increment the counters, while PB-1 clears them. PB-2 controls the programming pulse and PB-3 controls $\overline{CS}$/WE. PB-4 is used to sense the completion of the programming loop by detecting a high on the C output of the high-order 74193. PB-5 and PB-7 are not used. The interface connections are shown in Table 2. Pull-up resistors are used on the TTL outputs to ensure that the logic levels required by the 2708 inputs (3.0 volts, V_{IH}) are met.

The programmer requires four voltages, in addition to the 5 volt supply for KIM; the 2708 requires a -5 volt supply at 45 mA, +12 volts at 65 mA and +26 volts at 20 mA. The diagram in Fig. 6 illustrates a suitable supply. The power for the programmer should be controlled separately so the programmer can be turned off when the PROM is being inserted or removed.

Programming Procedure

1. Turn off all power. Then plug the programming board into the application connector on the KIM. Insert the PROM to be programmed into the 24-pin programming socket. Check the orientation to make sure that the number one pin is in the proper alignment.

2. Turn on the power to KIM, enter the PROM programming routine and the appropriate data. Make sure that the programming routine and the data have been entered correctly.

3. Enter the low address of the data into 00EA, 00EB, and the high address into 00EC, 00ED. The program will enter the cycle count into 00EE and use 00E8, 00E9 as the data-byte pointer. (00E7 is used as a false address during the program, so the contents will be lost.)

4. Turn on power to the programmer and examine the contents of peripheral port A (1700). With a blank PROM in the programming socket the data byte should be FF. Go to 0000 and hit GO. The programming will take just under two minutes. When the programming finishes the display will be 0000-A0.

If there was an error detected during the verification routine, the display will light up with the address of the error. To verify

A kit for building Jim's EPROM Programmer is available from:
O.C. Stafford Electronic Service & Development Co.
427 South Benbow Road
Greensboro NC 27401

	Drilled	Undrilled
PC Board (Part number KB/JHG 11478)	$ 7.50	$5.80
Parts kit (no board)	43.00	
Negative or positive	3.50	

Add $1 for shipping.

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        Zero page registers:

00EE cycle count
00EC, 00ED high data address: HDAL, HDAH
00EA, 00EB low data address:  LDAL, LDAH
00E8, 00E9 data pointer: DPL, DPH
00E7  Dummy counting address

      Program:

0000  A0  00              LDY    #00                        Clear Y
0002  A9  64              LDA    #64                        Load cycle count
0004  85  EE              STA    EE                         and store 00EE.
0006  A9  FF              LDA    #FF                        Set I/O Port B reg. to
0008  8D  02  17          STA    DRB                        high state and I/O
000B  8D  01  17          STA    DDRA                       port A to output.
000E  A9  EF              LDA    #EF                        Set I/O Port B to output
0010  8D  03  17          STA    DDRB                       except pin PB-4.
0013  A9  F5        A1    LDA    #F5                        Clear programming
0015  8D  02  17          STA    DRB                        counters.
0018  20  6E  00          JSR    Mov                        Go Sub MOV.
001B  B1  E8        A2    LDA(Y) Data                       load data using data pointer.
001D  20  77  00          JSR    PRGM                       Go Sub PRGM.
0020  20  90  00          JSR    INCA                       Go Sub INCA.
0023  90  F6              Bcc    A2                         If less than or equal
0025  F0  F4              BEQ    A2                         to high Data Pointer
                                                            continue entering data.
0027  A9  10        A3    LDA    #10                        Bit test for end of
0029  2C  02  17          BIT    DRA                        cycle.
002C  F0  07              BEQ    A4                         if done go to A4.
002E  C6  EE              DEC    EE                         decrement cycle count
0030  D0  E1              BNE    A1                         and if not zero go to A1.
0032  4C  3D  00          JMP    VRFY                       Go to VRFY.
0035  A9  FF        A4    LDA    #FF                        Program FF into
0037  20  77  00          JSR    PRGM                       remainder of PROM.
003A  4C  27  00          JMP    A3                         Go to end of cycle test.
003D  A9  00        VRFY  LDA    #00                        Set I/O Port A as
003F  8D  01  17          STA    DDRA                       input.
0042  A9  FD              LDA    #FD                        Clear programming
0044  8D  02  17          STA    DRA                        counters with CS low .
0047  20  6E  00          JSR    MOV                        Go Sub MOV.
004A  AD  00  17          LDA    DRA                        Load data word from PROM.
004D  D1  E8        B1    CMP(Y) data                       compare to data word
                                                            in RAM.
004F  D0  12              BNE    B2                         On error go to B2.
0051  A9  FF              LDA    #FF                        Toggle the
0053  8D  02  17          STA    DRA                        programming
0056  CE  02  17          DEC    DRA                        counter.
005E  F0  EA              BEG    B1                         go to B1.
0060  4C  4F  1C          JMP    KIM                        Return to KIM program
0063  A5  E8        B2    LDA    DPL                        on error set
0065  85  FA              STA    KIM     pointer low        KIM pointer to
0067  A5  E9              LDA    DPH                        error address
0069  85  FB              STA    KIM     pointer high       and return to
006B  4C  4F  1C          JMP    KIM                        KIM program

      Subroutines:

006E  A5  EA        MOV   LDA    LDAL                       Move low data
0070  85  E8              STA    DPL                        address into
0072  A5  EB              LDA    LDAH                       the data
0074  85  E9              STA    DPH                        pointer and
0076  60                  RTS                               return.

0077  8D  00  17    PRGM  STA    DRA                        Output data to PROM.
007A  E6  E7              INC    Dummy Add.                 Delay for data setup.
007C  A9  03              LDA    #03                        Raise PGM pin to
007E  8D  02  17          STA    DRB                        26 volts.
0081  20  8A  00          JSR    DELAY                      Go Sub DELAY.
0084  A9  06              LDA    #06                        PGM pin returned to GND
0086  8D  02  17          STA    DRB                        and counter incremented.
0089  60                  RTS                               Return.
008A  A2  F8        DELAY LDX    F8                         Delay for .99 msec.
0080  CA            C1    DEX                               (992 clock cycles)
008D  D0  FD              BNE    C1                         and
008F  60                  RTS                               return
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0090  E6  E8        INCA  INC  DPL                    Increment
0092  D0  02              BNE  D1                     data pointer
0094  E6  E9              INC  DPH                    and
0096  A5  E9        D1    LDA  DPH                    compare to
0098  C5  ED              CMP  HDAH                   High Data
009A  90  04              BCC  D2                     address
009C  A5  EB              LDA  DPL                    and
009E  C5  EC              CMP  HDAL                   return
00A0  60            D2    RTS

      PEEK routine:

00A1  A9  00        PEEK  LDA  #00                    Set I/O Port A
00A3  8D  01  17          STA  DDRA                   as an input.
00A6  A9  FF              LDA  #FF                    then toggle
00A8  8D  02  17          STA  DRB                    the programming
00AB  CE  02  17          DEC  DRB                    counters.
00AE  A9  00              LDA  #00                    Set KIM pointer
00B1  85  FA              STA  KIM   pointer low      to I/O Port A
00B2  A9  17              LDA  #17                    and jump
00B4  85  FB              STA  KIM   pointer high     to KIM program
00B6  4C  4F  1C          JMP  KIM                    to display PROM data.
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Program A. The programming program. The PEEK routine is used by entering A1 into 17FA and 00 into 17FB. Go to address 1703, hit the data key and enter C,F,F. This will clear the programming counters. Then go to address 1700. The data word displayed should be the first data byte in the PROM. By hitting the stop key, the PROM address can be incremented, and the data displayed will be the contents of the PROM.

the error load A1 into 17FA and 00 into 17FB. Then go to 1700.

The data should be the first byte in the PROM. To increment the PROM address, hit STOP. The data should now be the second byte in the PROM. Step the PROM to the location of the error.

If the error is a high bit in the PROM (e.g., a 1 in place of a 0), the programming can be attempted again. If it is a 0 in place of a 1, turn off the power and erase the PROM. Then verify that the erasure has returned the problem bit to a 1 and repeat the programming. Always be sure to turn off the power before inserting or removing the PROM.■