Clement S. Pepper
3270-96 Caminito East Bluff
La Jolla CA 92037

Safe Ports

Protect your I/O ports with this bidirectional buffer.

The individually addressable I/O ports of my KIM-1 are a valuable feature I really prize. I use them a lot for a variety of circuit experiments. I have also been haunted by the fear that through some program or circuitry defect I would inadvertently write a "0" to a low-impedance 5 volt source. Replacing an expensive 40-pin DIP is not a task I anticipate with enthusiasm.

So I have been scanning the literature in an unsuccessful search for a bidirectional buffer IC. My objective is a transparent circuit I can connect and forget.

Since I didn't find what I was looking for ready-made, I devised a circuit of my own. In addition to safety, it has another benefit. The drive capability is several TTL loads — from five to ten depending on the combined tolerances of the devices.

"Why not," I mused over a cup of coffee, "connect two comparators so that the output of each is summed into the input of the other! Then signals will flow both ways . . . and presto! I'll have a bidirectional gate." It took a little bit more than that, but not a whole lot more. The result is displayed in the circuit of Fig. 1.

How It Works

The circuit is based on the capabilities of the LM339 comparator. This versatile device will operate from a single power supply with a range of +2 to +36 volts. The common mode input range includes ground. Input impedance is high; the typical bias current is 25 nA. The typical input offset is 3 mV. Best of all, the output is the open collector of an uncommitted transistor. A schematic of the internal circuitry and package pinning is shown in Fig. 2.

Now let's look at KIM's I/O ports. My milliammeter tells me a port delivers 0.4 mA from a nearly constant current source in both the read and write mode. That is, the same current flows into ground when the port is shorted as flows into the 3300 Ohm resistor shown in the circuit.

With the port open, the output equals V_{CC}. The switching point is the center of V_{CC}, about 2.5 volts. The 6530 data sheet specs the output high current sourcing as 100 uA minimum, with 1 mA typical.

It is the READ current that dictates the design, provided that an equal or greater current is sourced in the WRITE mode. If the current is too low, the gate input will not overcome the reference. If it is too high, such that it stays above 2.5 volts, the port will not read a zero. So it will be wise to measure the read current from your ports and revise the input resistor if necessary to maintain the 1.1 volt potential. There is only one current sinking mode; when writing a "0" the port terminal goes low.

So let's see how the circuit does its thing. Observe the table in the upper left of Fig. 1. Port voltages in the high and low states are given for the READ and WRITE modes.

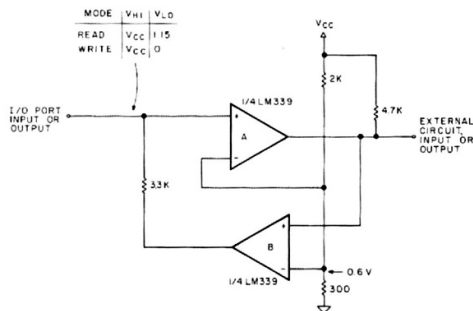Consider the READ first. VHI or VLO refers to the external cir-

Fig. 1. The bidirectional buffer. When connected to the KIM-1 I/O port it will both read and write to an external circuit. The buffer will also sink or source a greater current than the port.
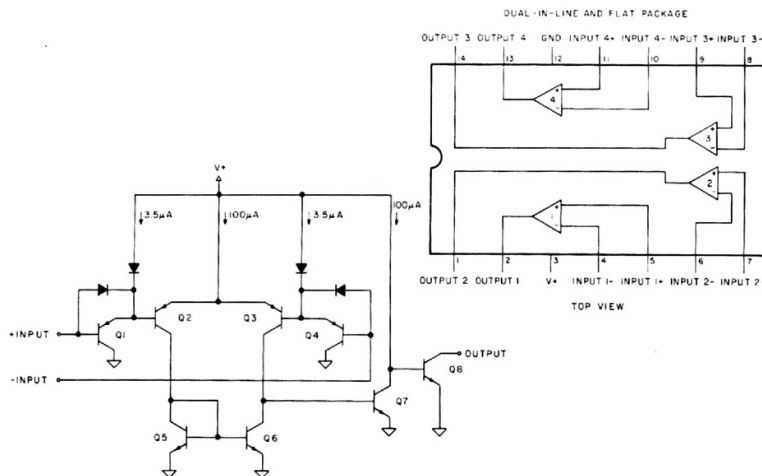

Fig. 2. LM339 internal schematic and pin connection diagrams.
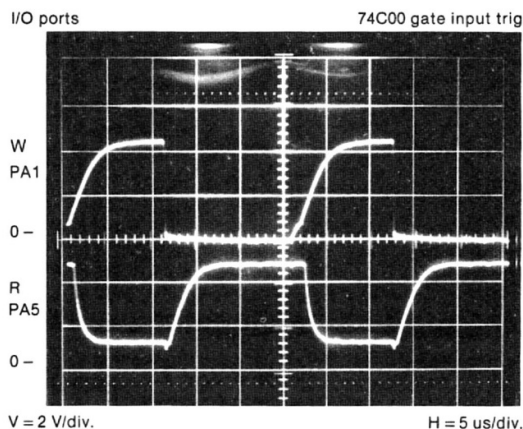
V = 2 V/div.   H = 5 us/div.

Photo 1. The upper trace is the I/O port write instructions. The lower trace is the port read signal. Observe that the trace bottoms out at about 1.2 volts when reading a zero. This is well below the switching threshold for the port.

V = 2 V/div.   H = 5 us/div.

Photo 2. The upper trace is the NAND input. The lower trace is the NAND output. The gate is a 74C00.

cuit. Observe that the non-inverting inputs of both comparators are connected to a reference of 0.6 volts. This establishes the switching threshold for the comparators.

An input from the external circuit exceeding the threshold will cause the "B" output to go high. Since the output is a transistor in cutoff, no current flows through the 3.3k resistor. The input of "A" draws negligible current; the port output is at V_{cc}. The "A" output is also cut off and has no effect on the external circuit.

Now suppose the external input goes to zero. The output of "B" now goes low, and the port sources current through the 3.3k load. This pulls the port potential down to 1.1 volts. Since this is well below 2.5 volts, the port reads a "0." However, the "A" input still exceeds the threshold, and the output remains in cutoff. This is essential, for should it go low, the gate will be locked up.

Now let's write a "1" to our external circuit. We will also assume a worst-case situation in which the external circuit is in the zero state. The output of "B" is low, drawing current from the port. Still, 1.1 V > 0.6 V and the output of "A" is off. Current flow through the 4.7k resistor pulls up the input to the external circuit and a "1" is written.

Next we elect to write a "0." The port goes low and pulls down the input of "A" below the threshold. Presto. "A" turns on, its output goes low and the zero is written. The zero is read back by "B," its output also goes low, but this has no effect.

Fig. 3 provides an illustration of a working circuit. The buffer is writing into a NAND gate from one port and reading back with a second. I wrote a looping routine for this and viewed the operation on my oscilloscope. Scope traces of the circuit in Fig. 3 are provided in Photos 1 and 2.

The upper trace of Photo 1 is the I/O write pulse at the KIM port. The lower trace is the I/O read. You can see that the bottom of the read is about 1.2 V above ground (vertical scale is 2 V per division). A 74C00 CMOS NAND is the external device. The 74C00 input and output are shown in the upper and lower traces of Photo 2.

Construction

I built up the circuit on perfboard. The layout is shown in Fig. 4. Eight LM339s are required for the 15 ports. Fourteen of the circuits are duplicates of Fig. 3 (don't put in the NAND!). Port PB7 requires a pull-up. Connect a 10k resistor between the port terminal and the +5 V bus.
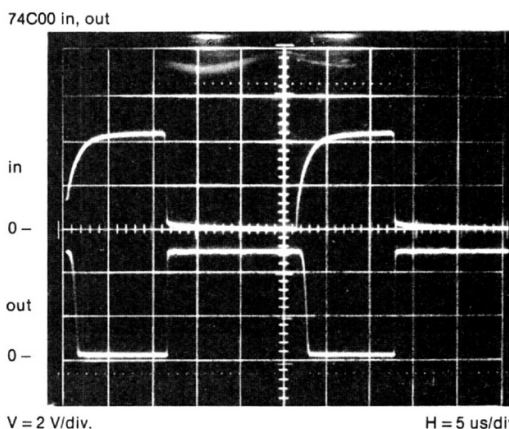
An AP Products 217L solderless plug-in matrix was split down the middle and one-half placed at each end as shown for input and output connections. Homemade ribbon cables provide quick connection to KIM at the input and to my external circuits at the output.

Only a single reference line is required for all the comparators. That is, a single 2k and 300 Ohm resistor are wired as shown, and pins 4, 6, 8 and 10 for all the devices are bused together.

Performance Testing

I wasn't about to connect the assembled circuit to my KIM-1 without a bench test. I did not solder the comparators to the board ... I used sockets. So before plugging in the ICs, I connected the 5 volt power to the bus and checked each socket pin for the correct voltages — 5, 0.6 or 0.

I then disconnected the power and plugged in the comparators. I gave each gate a performance test; for this I simulated the port with a test lead through a 10k pull-up to 5 volts. A voltmeter monitored the port
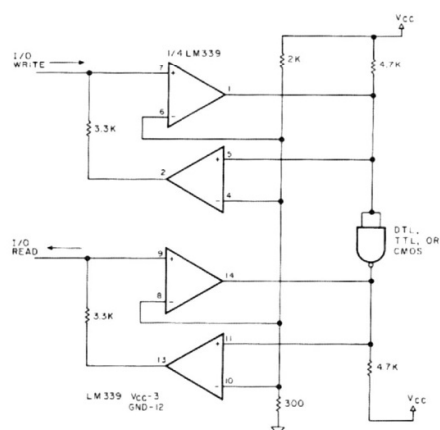

Fig. 3. An illustrative example of the buffer in operation. The upper port provides input to the NAND gate. The lower port reads the gate output.
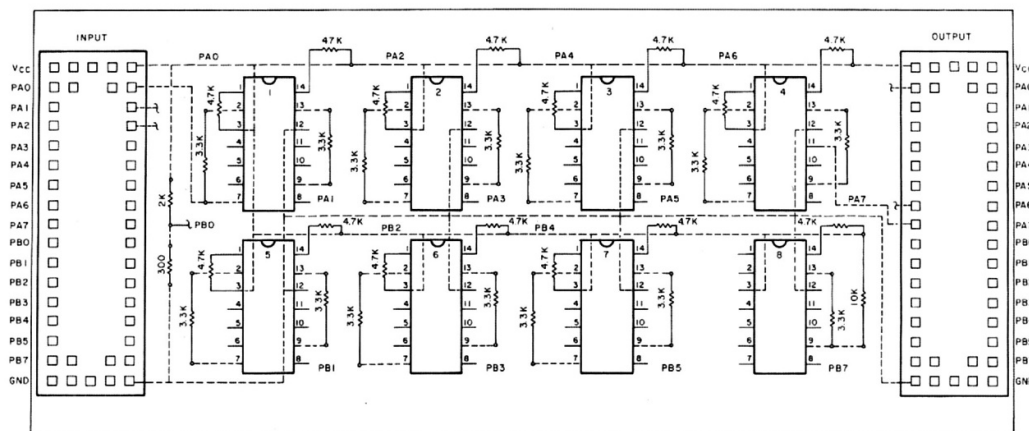
Fig. 4. Perfboard construction is efficient and compact. Circuit Stik Quik Circuits copper stick-ons enhance IC mounting. Upper row buffers ports PA0-PA7; lower row, PB0-PB7. Homemade ribbon cable provides quick connection to KIM and external circuits.

connection to the gate. With the gate output open, the meter will read 5 volts. Grounding the output will pull the reading down to about 1.2 volts. This test paid off — I found a bad solder joint. A higher reading will appear on PB7 because of the pull-up. It will be about 2.1 volts.

The KIM-1 Test

I connected my new gate assembly to KIM's dc power and the two ports with the power off. I then powered and reset KIM. Port A (1700) displayed FF; port B (1702) displayed BF as it should, since PB6 is always zero.

Next I grounded each gate output in turn, observing the port readout for the correct value. All went well.

That concluded the reading portion of the test. Now, will it write? I keyed in a short read, write and jump back to read routine and stepped it through. Bravo!

In my use of the gate so far, with both TTL and CMOS devices, it appears to be doing exactly what it was designed to do. Using the ports without fear is a good feeling. ■