KIMCTR

This KIM-1 frequency counter/timer can be used with any micro with comparable features.

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A low-cost frequency counter is readily constructed from an LSI counter IC and your KIM-1. KIM controls the counter, generates the one-second time base and displays the count.

If you don't have a KIM-1, read on anyway . . . the program is adaptable to any microcomputer on-a-board having comparable features. The prime requirements are addressable I/O ports and a hexadecimal display that can be controlled by your program.

The LS7030,[1] an 8-decade multiplexed MOS up counter, performs the counting. In addition to the counter and KIM, the design includes an input stage with threshold adjustment. I have also added circuitry for time mode measurement of both positive and negative pulses, with the widths displayed in microseconds for up to one second. I/O buffers are also provided—both to match the ports to the counter and to give protection, just in case. . . . The KIM-1 supply provides dc power.

Features

The frequency mode provides for two ranges: 1 Hz to 1 MHz with 1 Hz resolution or 10 Hz to 10 MHz with 10 Hz resolution. The LS7030 is specified to 5 MHz so the full x10 range may not be realized. If desired, the input can include pre-scaling, which I have not included. The time mode provides a measure of pulse width; positive- or negative-going pulses are switch selectable. The input may be a single pulse or a wave train. The sum of the positive and negative widths in a uniform train is the period. Resolution is 1 usec.

KIM provides full control of the counter via four I/O ports. Six digits of frequency or time are displayed on KIM's seven-segment readout. The display program is also the one-second time base for the frequency measurement.

Fig. 1 is a function diagram of the counter/timer. The basic functions are a high-impedance input stage with an adjustable threshold for sensitivity control, capture circuitry for the pulse width measurement, the LS7030 counter and KIM-1.

The LS7030 Counter IC

Fig. 2 is the internal circuitry of the counter. Key features of the LS7030 include dc to 5 MHz counting, multiplexed BCD and seven-segment outputs, single-power supply operation at 4.75 V dc to 15 V dc, high noise immunity, counter input latches and leading zero blanking.

The count input ripples through eight BCD counter stages. Each stage is provided with a 4-bit latch. Data stored in the latches is connected to the internal BCD bus by multiplexed switching. The switching sequence is controlled by a scan counter and decoder. The BCD lines are internally decoded to provide seven-segment outputs. Blanking for leading zero suppression is implemented internally.

All decades are reset to zero when $\overline{\text{RESET}}$ is brought low for a minimum of 4 usec. Contents of the counter are transferred to the latches when the $\overline{\text{LOAD}}$ signal is brought low for a minimum of 4 usec and kept low until a minimum of 17 usec has elapsed from the negative edge of the preceding count pulse. Raising the $\overline{\text{LOAD}}$ signal stores the counter data in the latches.

The counter scans from the most significant digit (MSD) to the least significant digit (LSD). When SCAN RESET is brought high, the scan counter is forced to the MSD state. The scan counter decrements one count on each negative transition of the SCAN INPUT.

Leading zero blanking is employed. At the start of each MSD-to-LSD scan, the seven-segment outputs are held low until a nonzero digit appears on the BCD bus. The display un-

1. The LS7030 is manufactured by LSI Computer Systems, Inc., 1235 Walt Whitman Road, Melville NY 11746. Telephone: (516) 271-0400. Query the manufacturer for distributors in your area. The device can be purchased from Mesa Engineering Sales, 7525 Convoy Court, San Diego CA 92111. Telephone: (714) 278-8021.

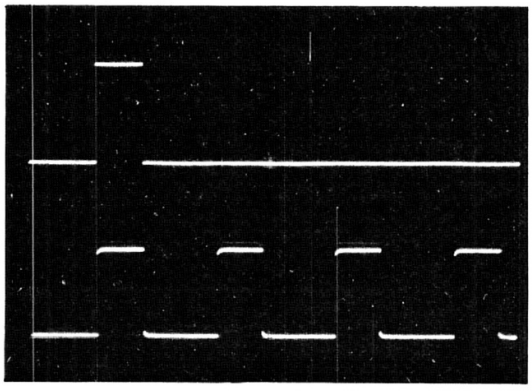

Photo 1. The first pulse of the train displayed in the lower trace has been detected and is displayed in the upper trace.

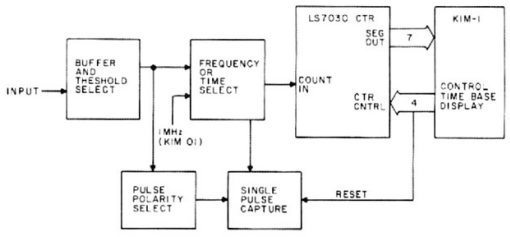

Fig. 1. KIMCTR function diagram.

blanks on the LSD; a zero is displayed when there is no counter input. A comment: In this program the zero is displayed on the x1 range; the entire display is blank on the x10.

All inputs are TTL compatible with +5 V operation. Outputs are CMOS compatible.

Counter Design

The complete circuitry for the counter/timer is shown in Fig. 3. The signal connects to the non-inverting input of an LM339 comparator. Input threshold is controlled by the setting of R4. The values shown yield a threshold of 0 to +2 volts. Other values may be chosen to extend the range if desired. In the frequency mode the signal is conducted through gates U1A and U1C to buffer U6A. The buffer is necessary because all the front-end circuitry operates from +12 V dc, with the counter and buffer at +5 V dc.

If frequency counting is all you need, ICs U1, U2, U3 and U4 will be omitted, along with comparators A1B, A1C and the switching.

The blanking output to PB0 shown is not used. Initially I thought it would be needed. PB5 and PB7 are shown grounded just to keep them from floating; they have no function.

Timer Circuitry

In the time mode a single pulse is plucked from the incoming train to enable gate U1B. A second input to this gate is the 1 MHz clock from KIM. This signal is counted for the duration of the pulse high time; thus the width is displayed in usec.

Now let's back up to see how the gating pulse is selected. Observe that the counter reset pulse is brought around to comparator A1C. This effects a translation from 5 volt logic to 12 volt. The trailing edge of the counter reset from KIM clocks the "D" flip-flop U2A. In so doing it places a "1" at the D input of U2B.

The next positive-going transition at pin 11 of U2B will set the Q output and enable gate U1B. U2A is reset at this time also. With the polarity switch in the "POS" position (as shown), this is the leading edge of an incoming pulse. EX-OR gate U4B is an inverter. The trailing edge of the pulse clocks U3A, which resets U2B, thereby inhibiting the gate and also resetting U3A. The operation of this circuit ensures that one complete pulse, and one pulse only, enables U1B for each counting cycle.

You can see the action in the scope traces in Photo 1. The lower trace is the incoming train; the upper shows that the first trace following reset has been captured.

Single pulse inputs will be accurately timed provided they occur within the one-second counting interval. With S2 in the "NEG" position, the negative portion of the wave is timed. If the pulse train is uniform, the sum of the two times is the period for one complete cycle.

The pulse width displayed corresponds to true width only for rectangular waveform inputs. For other waveforms the width measured is dependent on the waveshape and the threshold setting because of comparator squaring.

With the threshold at zero the displayed width is that of the entire positive or negative portion of the wave. This is illustrated in the scope traces in Photos 2-4. In Photo 2 the threshold is at zero; the comparator output is very nearly a square wave. The input is only 50 mV (RMS), which is about the ultimate sensitivity.

Increasing the input by a factor of 10 (Photo 3) with the

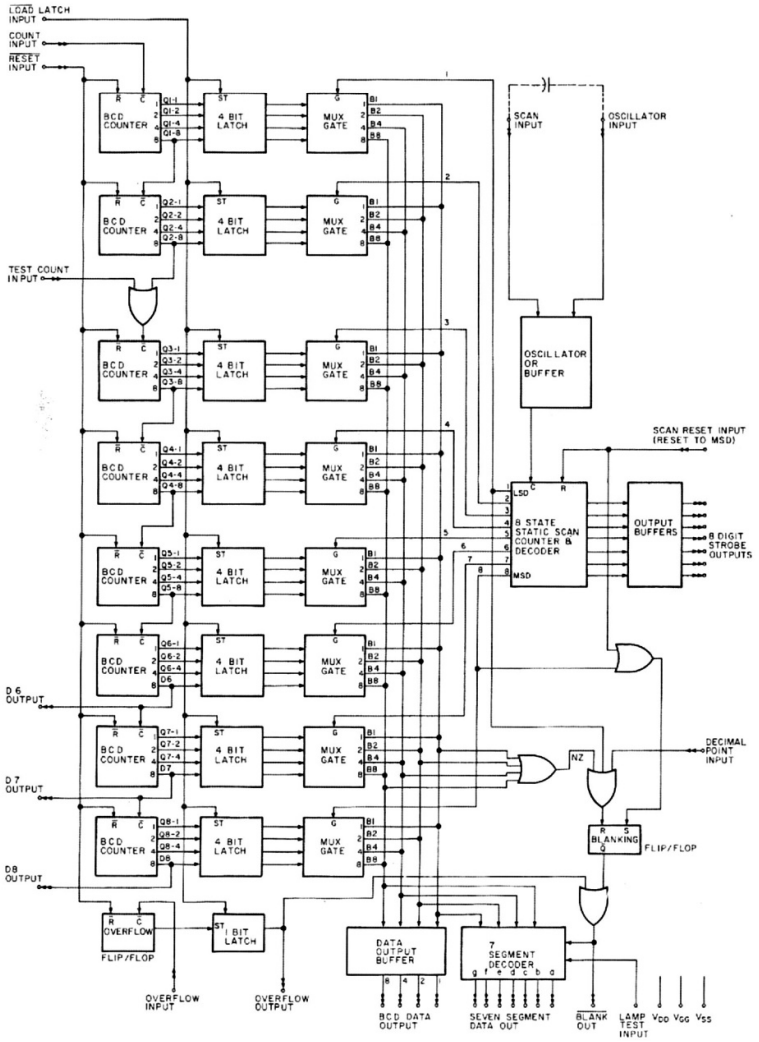

Fig. 2. Internal circuitry of the LS7030 counter. This device is ideally suited for microcomputer control.

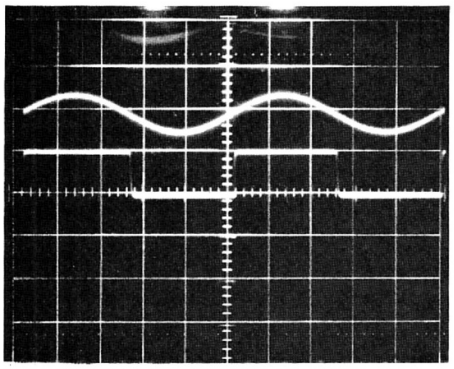

Photo 2. 50 mV (RMS) sine wave and comparator output. Threshold is at 0 V; output is nearly square.

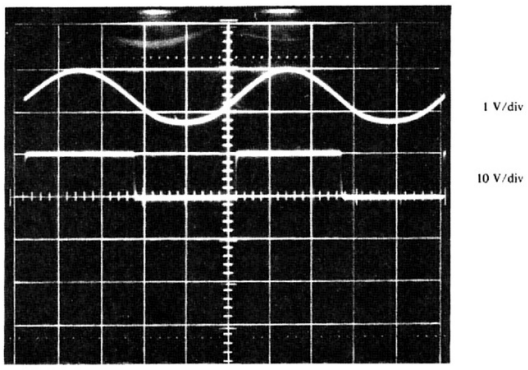

Photo 3. Signal increased to 500 mV (RMS); no change in threshold. Comparator output unchanged.

threshold unchanged shows little change in the output. In Photo 4 the threshold has been upped to 1.2 volts with a resulting drastic change in the output.

In Photo 5 the upper trace is the input, at 87 kHz. The measured width, that of the lower trace, matches the width of the input to within the 1 usec resolution of the measurement.

Counter Control

Reference to Fig. 3 shows four control inputs to the LS7030: LATCH, SCAN RESET, SCAN INPUT and CTR RESET. Control is exercised by KIM via I/O ports PB1-4. The 7408 AND gates are there to isolate the ports. Control waveforms and timing are shown in the diagram of Fig. 4. Numbers on the traces are time in usec.

Assume that the counter has accumulated data and it is time for KIM to take a collection. The initial step is to store the counter data in the latches and to reset the scan to the MSD. These two operations are performed simultaneously. Eighteen usec were allocated to assure a valid data store.

The SCAN INPUT is next

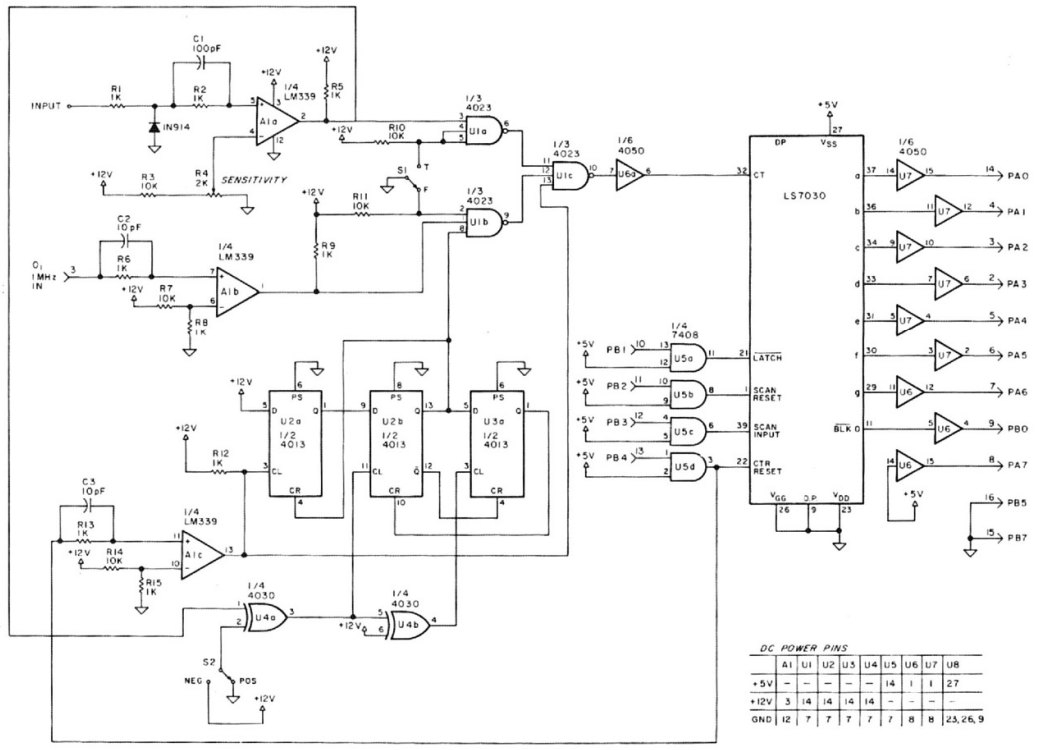

Fig. 3. Complete circuit diagram of the frequency counter/timer.

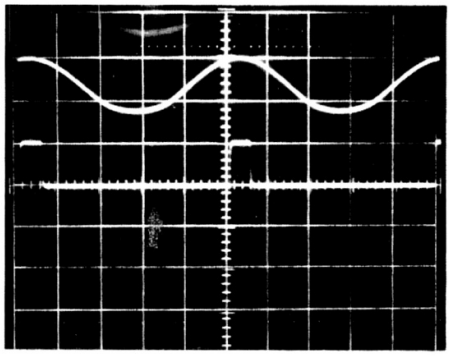

Photo 4. Threshold increase to 1.2 V narrows output pulse. Period is still the sum of positive and negative portions of output.

decremented to digit 7. Decrement occurs on the negative edge at 28 usec. This diagram is for the x1 range, decade 7 is not read and a second decrement is made. Twenty-one usec are absorbed to read and store the data from decade 6. The operation repeats until decade 1 has been read and stored. At 206 usec the counter is reset, and 12 usec later counting is resumed for the next update.

A flowchart for the control routine, CCNTRO, is provided in Fig. 5. The program is listed in Program A. Fig. 6 shows the sequence diagram and coding tables that I used to write the I/O instructions. I am not going into any detail on these as they are self-explanatory from the preceding descriptions after a bit of study. However, should you have any difficulty with these or any part of the system, send me a query with an SASE and I'll do my best to provide an answer.

Display and Timing

Subroutine DISPCT (Fig. 7) generates the six-digit display. The program has two delay loops (1 and 3) adjusted to yield the required one-second time base.

I suppose I could have utilized KIM's SCANDS routine, but I preferred to develop my own. It is a routine I use, with variations, for other things I also do with KIM.

The seven-segment data is read out by port A I/O during the CCNTRO routine and stored in locations 1781-86. The digit select codes are stored in locations 1787-8C; be sure to enter these with the program. Port A segment coding is illustrated in Fig. 8. The listing for DISPCT is provided in Program B.

Construction

I assembled all the circuitry on pegboard; the parts layout is

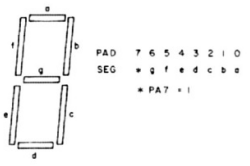

Fig. 8. Seven-segment display coding for Port A. PA7 is held high.

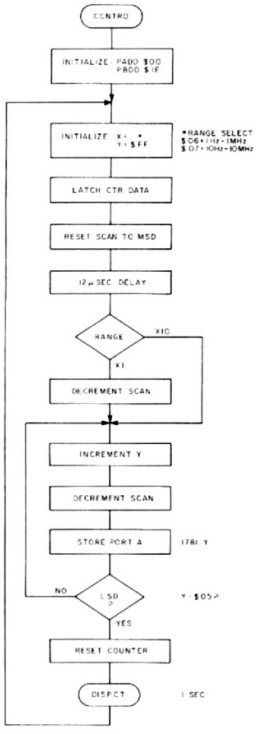

Fig. 5. CCNTRO flowchart.

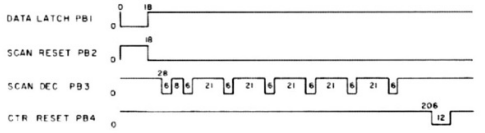

Fig. 4. KIMCTR control timing for x1 measurements. Numbers are time in usec.

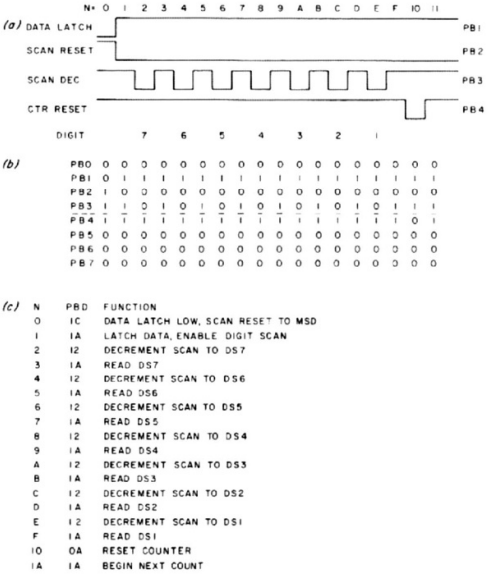

Fig. 6. (a) Sequence diagram. (b) Binary tabulation. (c) Code assignment and functions. This is the format I employ to assure true and complete I/O coding.

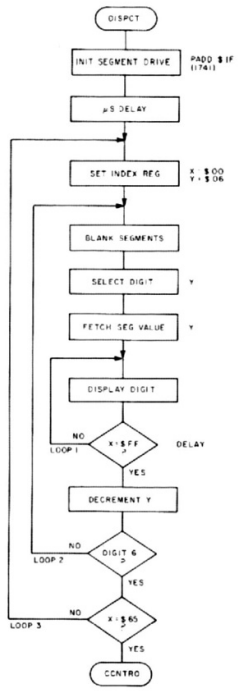

Fig. 7. DISPCT flowchart.

PROGRAM: KIMCTR
ROUTINE: CCNTRO

```
0300  A9 00     INIT    LDA #$00
0302  8D 01 17          STA PADD     PORT A DIR
0305  A9 1E             LDA #$1E
0307  8D 03 17          STA PBDD     PORT B DIR
030A  A2 06     BEGIN   LDX #$06     $06=X1, $07=X10
030C  A0 FF             LDY #$FF
030E  A9 1C             LDA #$1C
0310  8D 02 17          STA PBD      LATCH LOW; SCAN RESET
0313  EA                NOP          DELAY
0314  EA                NOP
0315  EA                NOP
0316  EA                NOP
0317  EA                NOP
0318  EA                NOP
0319  A9 1A             LDA #$1A
031B  8D 02 17          STA PBD      LATCH DATA
031E  E0 07             CPX $07      X10 SELECT
0320  F0 0A             BEQ LOOP1
0322  A9 12             LDA #$12
0324  8D 02 17          STA PBD
0327  A9 1A             LDA #$1A
0329  8D 02 17          STA PBD
032C  C8        LOOP1   INY          BEGIN SCAN AND READ
032D  A9 12             LDA #$12
032F  8D 02 17          STA PBD
0332  A9 1A             LDA #$1A
0334  8D 02 17          STA PBD
0337  AD 00 17          LDA PAD
033A  99 81 17          STA Y        STORE SEG CODE
033D  C0 05             CPY $05
033F  D0 EB             BNE LOOP1    NEXT DECADE
0341  A9 0A             LDA #$0A
0343  8D 02 17          STA PBD      RESET COUNTER
0346  EA                NOP          DELAY
0347  EA                NOP
0348  EA                NOP
0349  A9 1A             LDA #$1A
034B  8D 02 17          STA PBD      RESUME COUNT
034E  20 A0 17          JSR DISPCT   DISPLAY COUNT
0351  4C 0A 03          JMP BEGIN
```

Program A. CCNTRO program listing.

shown in Fig. 9. For connection to KIM, I hacksawed an AP Products #248-L terminal strip, seen in the upper right corner. Connection to KIM is by home-made ribbon cables, which connect at the far end to a similar strip. I brought out all of my KIM circuits to terminal strips for ready access when needed.

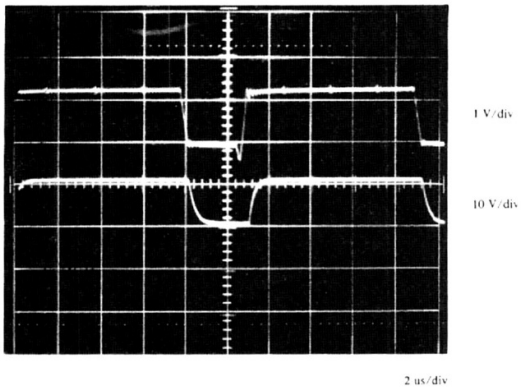

Photo 5. Rectangular input (upper trace) is reproduced in comparator output.

Thus, with the program stored on cassette tape, it takes but a few minutes to have my KIMCTR perking.

A Timer Application

Suppose you have some monostables on hand, perhaps from surplus or pulled from an ancient PC board, and you wonder if they are any good. Or perhaps you have a critical timing requirement and want to adjust the output pulse just so. These are accomplished quickly and easily with the setup illustrated in Fig. 10, where a 74121 is undergoing just such a test. The "B" input is triggered by the rising edge of the reset and the pulse width read out on KIM.

This project is inexpensive and easy to complete. With the foregoing materials and a little time on your part, you'll soon have a micro-controlled frequency counter/timer. ■

PROGRAM: KIMCTR.
ROUTINE: DISPCT.

```
17A0  A9 7F     DISPLA  LDA #$7F
17A2  8D 41 17          STA PADD     KIM'S DISPLAY
17A5  D8                CLD
17A6  A9 FF             LDA #$FF
17A8  85 10             STA          LOOP 3 INDEX
17AA  EA                NOP          DELAY
17AB  E6 10     LOOP3   INC
17AD  EA                NOP          DELAY
17AE  A2 00             LDX #$00     LOOP 1 INDEX
17B0  A0 06             LDY #$06     LOOP 2 INDEX
17B2  A9 80     LOOP2   LDA #$80
17B4  8D 40 17          STA SAD      BLANK DISPLAY
17B7  B9 86 17          LDA Y
17BA  8D 42 17          STA SBD      DIGIT STORE
17BD  B9 80 17          LDA Y
17C0  8D 40 17          STA SAD      SEGMENT STORE
17C3  E8        LOOP1   INX
17C4  E0 F6             CPX #$F6
17C6  D0 FB             BNE LOOP1    TIME DELAY
17C8  88                DEY
17C9  C0 00             CPY #$00
17CB  D0 E5             BNE LOOP2    NEXT DIGIT
17CD  A6 10             LDX
17CF  EA                NOP          FILLER
17D0  E0 5B             CPX #$5B
17D2  D0 D7             BNE LOOP3    TIME DELAY
17D4  60                RTS          RETURN TO CONTRO
```

Display Data

DIGIT	LOC	CODE	LOC
6	1786	13	178C
5	1785	11	178B
4	1784	0F	178A
3	1783	0D	1789
2	1782	0B	1788
1	1781	09	1787

Program B. DISPCT program listing.

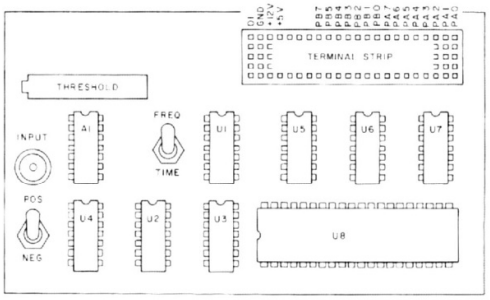

Fig. 9. Pegboard parts layout. I use Circuit Stik Quik Circuits copper stick-ons for parts attachment. Ribbon cable terminated in 8-pin connector plugs in AP Products terminal strip in upper right.

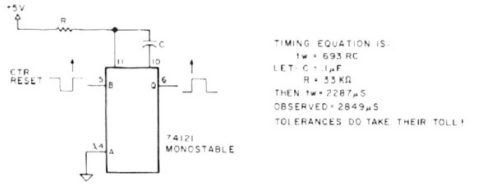

Fig. 10. KIMCTR provides an accurate indication of monostable pulse width.