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KIM-1 Memory Expansion

... adding memory to this popular system is a snap

When you get ready to sit down and write that construction article you've been putting off, let me suggest you go back and re-read this article on KIM-1 memory expansion as a good example of how to do it right. – John.

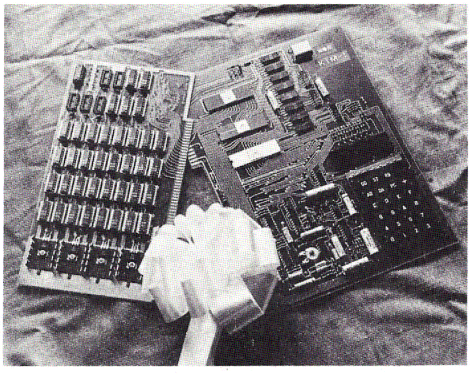
If you own an MOS Technology KIM-1 microcomputer and wish to add to its memory capacity, your first choices would be the KIM-2 (4K) and KIM-3 (8K) preassembled memory boards from MOS Technology. But, it is possible to modify Altair-compatible memory boards to work with KIM-1. One such board, the S. D. Sales 4K Low Power Ram Board Kit (available from S. D. Sales Co., P.O. Box 28810, Dallas, Texas 75228) is easy to modify. It can be connected to KIM-1 with the addition of only wire, connectors, four resistors, and a power supply. Therefore, it is an easy first step for the KIM-1 owner who is just beginning to expand his system. Furthermore this particular board can be modified without making any permanent changes to the board (i.e., no printed circuit trace cutting is required). The board can be restored to its original condition as an Altair-compatible board and resold to an Altair owner at a later time, if that should become desirable.

In addition to being easy to modify, the S. D. Sales memory board is an excellent value, being the most inexpensive kit of its kind that I am aware of. All parts are of high quality, including the solder-masked printed circuit board with plated through holes (like the KIM-1 board), and 21L02 high-speed (500 ns; within KIM-1 requirements) low-power RAMs. Address and data lines are fully buffered.

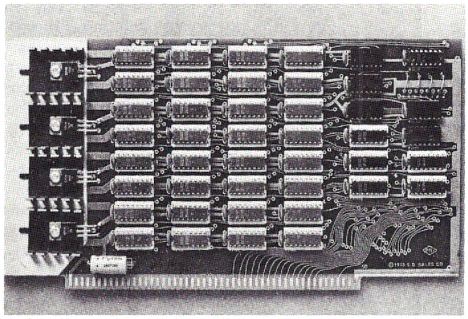
The board requires one ampere from an 8 volt (or so) unregulated power source. The power supply circuit shown in the KIM-1 User Manual *cannot* power both the memory board and KIM-1.

Theory of Operation

This modification uses the memory decoding already provided on the KIM-1 board. The added memory is logically concatenated with the 1K RAM on KIM-1; the result is 5K (5,120) bytes of contiguous RAM, with addresses from 0000 to 13FF (hex).



KIM-1 and the S. D. Sales 4K Low-power Memory Board pose for their formal wedding portrait.



The memory board after assembly and modification. Note that in the column of IC sockets on the far right two are empty, and that in the next column, three are empty. These ICs are omitted as part of the modification. Note also the address jumpers near the upper right corner of the board.

A simplified schematic of the modified memory is shown in Fig. 1. Most of the 21L02 RAMs have been deleted from the diagram of the memory to clarify it and make the basic organization easier to see. Most of the decoding circuitry on the original board is deleted as part of the modification. The only remaining portion of that circuitry, IC34, is shown. (In this discussion and in the modification instructions the IC numbers are those used in the kit manufacturer's documentation.)

The thirty-two 21L02 RAMs are connected in four rows of eight RAMs each. Each row stores 1,024 (1K) bytes, the eight RAMs in each row composing the eight bits of a byte. Only the left-most two columns and lower two rows are shown in the diagram. As can be seen, the four RAMs in each column have their inputs and outputs tied to common lines, and the eight RAMs in each row have their chip enable lines tied to common lines, which are the K1, K2, K3, and K4 lines from the memory decoder on KIM-1. When no access is being made to the added memory, K1-4 inputs are at a high (logic 1) level, pulled up by added resistors R1-4.

When the decoder on the KIM-1 detects that a reference is being made to an address in the range of 0400 to 13FF (hex), it *pulls down* (to a logic 0) one of the K lines. The eight 21L02s whose chip enables are connected to that particular line are enabled for reading or writing (which one is not known at this point). Eight 21L02s are enabled at once to compose the eight bits of a byte.

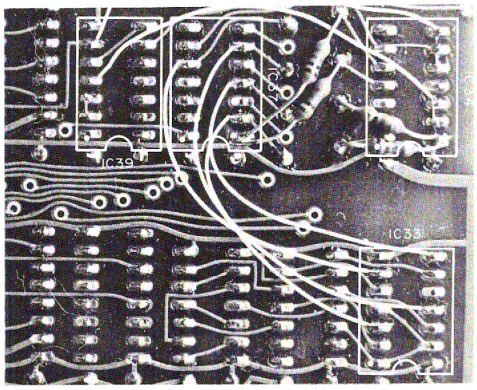
The K lines are also connected to a NAND gate, IC34a. It is shown as an OR gate with inverted inputs rather than as a NAND gate because it is performing an OR function: to detect if K1 *or* K2 *or* K3 *or* K4 goes low. When one of them does, IC34a's output will go high, denoting that one of the four rows of 21L02s has been enabled. IC34a's output can be called *board select* and it is labeled as such on the diagram. IC34b's inputs are R/W (read/write) from KIM-1 and board select. (IC34b is not used on the original board, but is used here because of the modification jumpers installed. IC34b is a four-input gate, but it is used as a two-input gate by connecting its inputs in pairs.)

The R/W line is high during processor read cycles and low during write cycles. IF R/W is high, denoting a *read*, and if board select is high, denoting an access to the board, then the output of IC34b will be low. This will enable Tri-state buffers IC38 and IC43, and the outputs of the enabled 21L02s will be connected to the system data bus, from which the processor will read the data.

During a write to the board, one of the K lines will be low and board select will be high. However, R/W will be low, therefore the output of IC34b will remain high, IC38 and IC43 will not be enabled, and the 21L02 outputs will not be connected to the data bus. This is as it should be, since the processor is supplying data to the data bus during a write cycle. The RAM-R/W line from KIM-1 is connected to the write inputs of the 21L02s; it goes low during the time that data is valid for a write cycle. Even though RAM-R/W is connected to all thirty-two 21L02s, data is written into only the eight that have their chip enable inputs low.

KIM-1 address lines AB0 through AB9 are applied to the 21L02 address lines by sections of IC40 and IC42, which are continuously enabled by their enable inputs being grounded. AB0 through AB9 are decoded internally by the 21L02s to select one of the 1,024 bits within each 21L02.

If you look at the KIM-1 schematic, you will see that the inputs and outputs of the on-board memory 6102s (which are 21L02 equivalents) are *split* by Tri-state buffers U13 and U14 (74125s) just as the 21L02 inputs and outputs are *split* by Tri-state buffers (8T97s) IC38 and IC43 on this memory board.



An enlargement of the portion of the back of the board in which the modification jumpers are installed. The four added resistors, the six insulated-wire jumpers, and the two bare-wire jumpers at IC34 and IC39, are visible.

Modifying and Connecting the Board

Begin the modification by constructing the board according to the instructions supplied. I repeat here the warning that appears in the instructions: "Assembly of this board requires experience in the soldering of very fine connections." A microspade soldering tip, such as the UNGAR PL-114 (available from James Electronics), is a great help. The solder mask on the board helps prevent solder bridges, but care must be used in the construction. Mount and solder the regulators to the board, but do not insert any ICs in sockets yet. All jumpers are installed on the back of the board (see photo). From this side of the board the view is of row upon row of IC socket pins, and it is difficult discerning which row belongs to which IC, so use care in installing the jumpers. Modification proceeds as follows:

1. Using a short piece of small diameter bare wire (such as #30 wire-wrap wire, stripped) solder a jumper between IC34 pins 6, 9, and 10. Solder a similar jumper between IC39 pins 2 and 3.
2. Using insulated wire, solder a jumper between IC34 pins 12 and 13 and IC39 pin 4. Solder a jumper between IC34 pin 8 and IC39 pin 6.
3. Solder four insulated wire jumpers between the following pins of ICs 37 and 33: IC37 pins 13, 11, 9 and 5 to IC33 pins 3, 8, 11 and 6, respectively.
4. Starting from the back of the board, insert one lead of each of four 560 Ohm, ¼ Watt resistors through the holes marked a, b, c, d nearest IC34. On the socket side of the board, bend the end of the resistor lead that comes through hole a near IC34 and pass it through hole a near IC37. Clip off the excess lead and solder both holes. Repeat this process for holes b through d. The other lead of each resistor must be connected to +5 volts. This is best done by bending the bodies of two of the resistors toward the connector edge of the board, clipping off the excess lead, and soldering them to IC37 pin 14. The other two resistors can be bent away from the con-

nector edge and soldered to IC34 pin 14.

5. Insert the 21L02s, IC34 (a 74S20), and ICs 38, 40, 41, 42 and 43 (8T97s). ICs 33, 35, 36, 37 and 39 are not used and must be omitted.

KIM-1 Expansion Connector	to	Memory Board Connector
pin A (AB0)		pin 79
pin B (AB1)		pin 80
pin C (AB2)		pin 81
pin D (AB3)		pin 31
pin E (AB4)		pin 30
pin F (AB5)		pin 29
pin H (AB6)		pin 82
pin J (AB7)		pin 83
pin K (AB8)		pin 84
pin L (AB9)		pin 34
pin Z (RAM-R/W)		pin 68
pin V (R/W)		pin 47
pin 8 (DB7)		pins 43 *and* 90
pin 9 (DB6)		pins 40 *and* 93
pin 10 (DB5)		pins 39 *and* 92
pin 11 (DB4)		pins 38 *and* 91
pin 12 (DB3)		pins 42 *and* 89
pin 13 (DB2)		pins 41 *and* 88
pin 14 (DB1)		pins 35 *and* 94
pin 15 (DB0)		pins 36 *and* 95
KIM-1 Application Connector		
pin C (K1)		pin 33
pin D (K2)		pin 85
pin E (K3)		pin 86
pin F (K4)		pin 32

Connection to the memory board requires an Altair bus 100-pin connector, available from several mail-order sources or computer stores. Connection to the KIM-1 expansion port requires a 44-pin connector, available at Radio Shack, part number 276-1551. Connections are as follows:

The above connections can be made with small diameter wire and should be no more than a foot long to minimize noise problems. The ground on the memory board, pins 50 and 100, should be connected to the ground on KIM-1 at expansion connector pin 22 or application connector pin 1 with number 18 or heavier wire. The negative side of the memory power supply, a source of about 8 volts unregulated at 1 ampere, should be connected to memory board pins 50 and 100. The positive side of the supply should be connected to memory board pins 1 and 51. These connections should be made with number 18 or heavier wire.

Note: the jumper from KIM-1 application connector pin K (decode enable) to pin 1 (ground) that is installed as part of the start-up instructions in the KIM-1 User Manual *must* be left in place.

Testing

Plug KIM-1 into the application and expansion connectors but do not plug the memory board into its connector. Apply power to KIM-1 and verify that all on-board functions work, e.g., try writing and reading cassette tape and altering and displaying memory. If any KIM-1 functions fail, remove power, unplug the expansion connector, and try again. If the failure disappears, the problem is probably a short between two pins on the expansion connector. If everything seems to be functioning, remove power, plug the memory board into its connector, and apply power to both the memory and KIM-1. Again verify that all on-board functions of KIM-1 operate properly.

Next, verify that the new memory can be examined and changed from the KIM-1 keyboard — enter AD (address) 0, 4, 0, 0 then DA (data) 0, 0, 1, 1, 2, 2, 3, 3, . . . ,E, E, F, F to verify that all bits are usable at address 0400. Repeat for addresses 0800, 0C00, and 1000.

If all addresses tested fail, suspect a problem with the data bus (DB0-DB7) wiring, or the RAM-R/W or R/W wiring. If some addresses work but others fail look for a problem in one or more of the K lines.

If these tests are successful, further testing must be done with a program. The logic of that program should be:

1. Store hex 00 in all locations to be tested. Verify that each location accepts the 00.
2. Store hex FF in the first location to be tested, verify that the FF has been accepted, then test all other locations to see that they still contain 00. Clear the first location to 00 store FF in the second location and test all other locations (including the first) to see that they still contain 00. Repeat for all remaining locations to be tested.

Testing by this kind of program will reveal problems in the address wiring (AB0-AB9, and K1-K4), or defective RAMs.

Conclusion

When I ordered my memory board from S. D. Sales, I did not know how difficult or easy it would be to adapt it to my KIM-1 system. I was pleasantly surprised at how easy it was, and I suspect that many other Altair-compatible accessories can be just as easily attached to KIM-1. With a bit of ingenuity, we KIM-1 owners can have the best of both worlds. ■

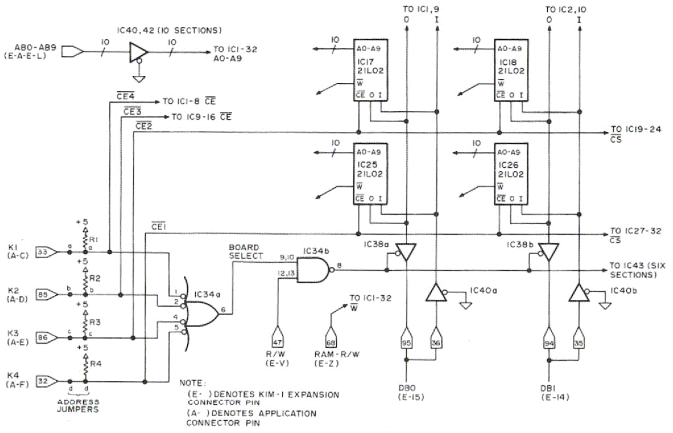


Fig. 1. Simplified schematic of modified memory board.