COMMON INSTRUCTIONS

OF THE 6800 AND 6502

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The 6800 and 6502 microprocessors share many common features in their architectures, instruction sets, busses, and general system philosophy. I have compiled for teaching purposes a list of their common instructions and their addressing modes. This list is used in conjunction with a programming model which shows only the two MPUs' common features (Fig. 1). The programming model has an 8-bit accumulator, index register, stack pointer and status register and a 16-bit program counter. Only 5 bits of the status register are used: carry/borrow, overflow, zero, negative and interrupt mask.

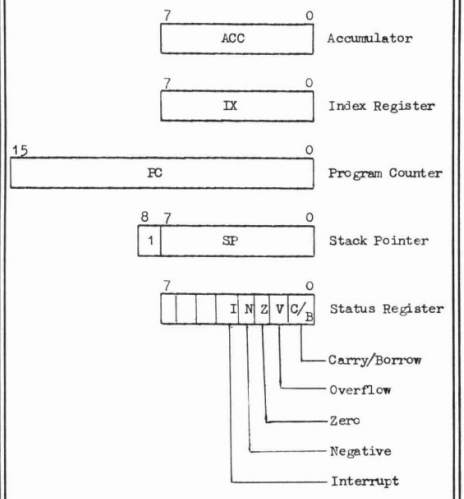

Figure 1. Programming Model

There are 43 instructions in the list (Fig. 2) common to the 6800 and 6502, which form a viable instruction set. This set is useful in the teaching of the two MPUs as well as in defining a common assembly language for them (In my microcomputer classes, I have given the name "5800" to this common microprocessor model).

	IMM	DIR	EXT	IMP	REL	IND
ADC	x	x	x			x
AND	x	x	x			x
ASL/ASLA			x	x		x
BCC					x	
BCS					x	
BEQ					x	
BIT		x	x			
BMI					x	
BNE					x	
BVC					x	
BVS					x	
BPL					x	
CLC/CLB				x		
CLI				x		
CLV				x		
CMP	x	x	x			x
CPX	x	x	x			
DEC			x			x
DEX				x		
EOR	x	x	x			x
INC			x			x
INX				x		
JMP			x			
JSR			x			
LDA	x	x	x			x
LDX	x	x	x			
LSR/LSRA			x	x		x
NOP				x		
ORA	x	x	x			x
PSH				x		
PUL				x		
ROL/ROLA			x	x		x
ROR/RORA			x	x		x
RTI				x		
RTS				x		
SBC	x	x	x			x
SBC/SEB				x		
SEI				x		
STA		x	x			x
STX		x	x			
SWI				x		
TSX				x		
TXS				x		

Figure 2. Instruction Set

Certain points should be noted about this instruction set:

1. The mnemonics used are generally those of the 6800, with the A or B accumulator specification omitted. For the 6502, PSH, PUL and SWI correspond to PHA, PLA and BRK respectively.
2. There are six addressing modes: immediate, direct, extended, implied, relative and indexed, as for the 6800. For the 6502 direct, extended and indexed correspond to zero page, absolute and zero page indexed respectively.

3. The indexed mode is restricted to a zero page addressing range, with a one-byte operand and an 8-bit index register. For the 6800, "00" should be loaded into the high byte of the 16-bit index register to simulate an 8-bit index register.
4. The 8-bit stack pointer operates like that of the 6502; its contents are always preceded by hex 01, so that the stack is always in the range hex 0100 to 01FF. For the 6800, hex 01 should be loaded into the high byte of the 16-bit stack pointer.
5. The borrow bit and the SBC instruction operate differently for the 6800 and 6502. For the 6800, the borrow bit is equal to the carry bit while for the 6502 it is the inverse of the carry bit. Two "pseudo- instructions" have been added to the instruction set: clear borrow bit (CLB) and set borrow bit (SEB). These are to be used in conjunction with the SBC instruction. For the 6800, CLB and SEB are replaced by CLC and SEC respectively, while for the 6502 the reverse is peformed, *i.e.* SEC replaces CLB and CLC replaces SEB. This enables us to add SBC to the list of common instructions.

The list and programming model have been useful to me both in teaching and writing source programs that will run on both MPUs. I have prepared for my students a more comprehensive data sheet that also gives the respective op codes for the 6800 and 6502, which I will be happy to send to interested readers (the new Motorola 6805 microcomputer, strangely enough, resembles the above model in some respects).