

A NOTE ON 6502 INDIRECT ADDRESSING

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There are two kinds of indirect addressing on the 6502, both of them with indexing. Except for JMP, however, indirect addressing *without* indexing is not provided. Since indirect addressing seems to be more useful without indexing than with it, many people have erroneously regarded this as a design flaw.

In fact, anything you can do with indirect addressing without indexing can be done, and done faster, with post-indexed (Y-register) indirect addressing on the 6502. We shall now give several illustrations of this.

Suppose we have two zero-page locations called IA and IA+1 for holding an indirect address. We can initialize these by setting them to AD and AD+1, as follows:

```
LDY AD
STY IA
LDY AD+1
STY IA+1
```

At this point we may do a JMP (IA), but not a STA (IA) (for example), since that instruction does not exist on the 6502. It may be simulated, of course, by loading the Y register with zero, so that the full sequence becomes

```
LDY AD
STY IA
LDY AD+1
STY IA+1
LDY #0
STA (IA),Y
```

But this is unnecessary. All we have to do is keep IA (the low-order address) set to zero at all times, and write

```
LDY AD+1
STY IA+1
LDY AD
STA (IA),Y
```

which is a *decrease* in the number of instructions (from 5 to 4), rather than an *increase* (from 5 to 6).

Why does this work? Suppose that the

indirect address is 2345. Then AD contains 45 (hex) and AD+1 contains 23. Instead of putting 45 in IA and 23 in IA+1 (giving an indirect address of 2345, without indexing), we put *zero* in IA and 23 in IA+1, giving an indirect address of 2300. To this we apply indexing, with 45 (hex) in the Y register; 2300 plus 45 makes 2345.

A common use of this capability is in processing arrays of strings. Suppose we have an array T of *n* strings, with $n \leq 128$. This is implemented as an array of *n* addresses, with T(2*k*-1) and T(2*k*) containing, respectively, the low-order and high-order parts of the address of the first character of the *k*-th string in the string array T, for $1 \leq k \leq n$. To get the first character of the *k*-th string, we perform

```
LDA K
ASL
TAY
LDA T-1,Y
STA IA+1
LDA T-2,Y
TAY
LDA (IA),Y
```

This assumes that T(1) is contained at T, T(2) at T+1, etc., so that T(2*k*-1) is kept at T+2*k*-2 (= (T-2)+2*k*), and that IA contains the constant zero as before. This time the saving is not quite as great because we cannot do an LDY T-2,Y directly (we could not even do an LDY T-2,X unless T is in page zero). But TAY is certainly both shorter and faster than STA IA (which is what we would have done if indirect addressing without indexing had been available). (Note: ASL, in the above code, shifts the A register left by one, thus multiplying it by 2. On some assemblers one writes ASL A instead of simply ASL for this.)

The same sort of savings accrue if T is a parallel array rather than a serial array. That is, suppose we keep two arrays, T1 and T2, where all the low-order bytes are in T1 and all the high-order bytes are in T2. That is, what was in T(2*k*-1) and

T(2*k*), respectively, is now in T1(*k*) and T2(*k*). There is now no need to multiply *k* by 2, and, perhaps more importantly, we can have $n \leq 256$ rather than $n \leq 128$ as in the preceding example. (The reason in both cases, of course, is that our indices into the arrays T, T1, and T2 must, in each case, fit into an eight-bit register, and must therefore be between 0 and 255, inclusive. Arrays with this property may be referred to as *short arrays*.) The code is now

```
LDY K
LDA T2-1,Y
STA IA+1
LDA T1-1,Y
TAY
LDA (IA),Y
```

under the same assumptions as before.

In either case, incrementing the calculated indirect address is also speeded up. Incrementing the 16-bit quantity in IA and IA+1, if we needed that, would have been performed by

```
INC IA
BNE NXT
INC IA+1
NXT (next instruction)
```

In the actual case, the incrementation is performed by

```
INY
BNE NXT2
INC IA+1
NXT2 (next instruction)
```

which is again both shorter and faster.

It is true that, in this case, if we know that none of our strings has length greater than 256, we can do even better by using straightforward post-indexing rather than simulated non-indexing. The setup takes a little longer—we have to write something like

```
LDA K
ASL
TAY
LDA T-1,Y
```

```

STA IA2+1
LDA T-2,Y
STA IA2
LDY #0
LDA (IA2),Y

```

—but now a simple INY suffices for incrementing the indirect address. Note that we carefully set up two further page-zero locations here, IA2 and IA2+1, because IA2, unlike IA, is *not* kept at the constant value of zero.

Another, even more common, application of these ideas is in indexing *long arrays* (this is, arrays of more than 256 bytes). Suppose that U is such an array and we wish to index U(J), where J has just been calculated. Here both U and J are 16-bit quantities. Assuming that #U and /U represent, respectively, the (constant) lower half and upper half of the address of U, we can add U and J and store the result at IA2 by the following code:

```

CLC
LDA #U
ADC J
STA IA2
LDA /U
ADC J+1
STA IA2+1

```

and then, if we had indirect addressing without indexing, we would be ready to apply it. As it is, all we have to write is

```

CLC
LDA #U
ADC J
TAY
LDA /U
ADC J+1
STA IA+1

```

with IA set permanently to zero as before, and we are ready to use an instruction like LDA (IA),Y (again, this is both shorter and faster than what preceded it).

If we can set aside another two bytes in page zero for use only with *this particular array* U, we can do even better than that. Let us call them IA3 and IA3+1; the permanent contents of IA3 are the low-order byte of the address of U, rather than zero. This can be set up with a declaration like

```
IA3 ADR U
```

which actually sets up *both* IA3 and IA3+1, although only IA3 will be needed. We can now save two instructions each by writing

```

CLC
LDA /U
ADC J+1
STA IA3+1
LDY J

```

and now LDA (IA3),Y will load U(J) into the A register. Why does that work? Let us make the following abbreviations:

p — high-order byte of address of U (i.e., /U)
q — low-order byte of address of U (i.e., #U)
r — high-order byte of J (contents of location J+1)
s — low-order byte of J (contents of location J)

The 16-bit quantities we are adding are $256p+q$ and $256r+s$. The two bytes IA3 and IA3+1 contain, respectively, *q* and *p+r*, so that this 16-bit quantity is $256(p+r)+q$. To this we add *s* by post-indexing, so that the computed address is actually $(256(p+r)+q)+s = (256p+q)+(256r+s)$, or J plus the address of U.

The above may be extended immediately to arrays U of two-byte or four-byte quantities. A curious intermittent error may arise, however, if three-byte quantities are used. We would, of course, multiply the 16-bit quantity in J and J+1 by 3 before using it, and then we would increment Y by one (using INY) to get the second byte set up, and again to get the third byte set up. This works fine, 99% of the time. However, if J is 85, so that 3J is 255, then incrementing Y by one is not enough, since there is carry into the high-order byte of 3J. We must test for nonzero after the increment, and then increment IA3+1 otherwise. (Similar problems arise for J = 170, 341, 426, etc.) It should not be hard to see that there will never be carry of this kind for an array of *n*-byte quantities where *n* is

2, 4, 8, or in general any power of 2.

In the above case it was assumed that U(0), rather than U(1), is contained at U; if this is not the case, then the address of U minus 1 must be substituted, in the above, for the address of U. We assume throughout, of course, that all 16-bit quantities are kept with the low-order byte first, as is customary on the 6502. The concepts of serial and parallel array are discussed further in [1]. Finally, users of the LISA assembler for the 6502 should substitute \$0, \$1, and \$2 for 0, 1, and 2 respectively, throughout the coding examples above.

Reference: Maurer, W.D., *Programming*, Holden-Day, 1972, pp. 74-75.

About himself, Prof. Maurer has this to say:

I've worked for CSC, Lockheed, Project MAC, UC Berkeley (as an Assistant Professor) and The George Washington University, Washington, D.C. (as an Associate Professor and now a full Professor). I've written a book called Programming as well as The Programmer's Introduction to LISP and The Programmer's Introduction to SNOBOL. In my spare time I write songs (My Pet Rock Is In Love, Dracula's Mood Ring, etc.) and have them performed by a group of weird people called The Hexagon Club.

LISTING

```

JPRINT ""
!LOAD PPR5
BLOAD PPR5, A#2000
OX!LIST

```

```

1      ORG $18
2      ADR U
3      ORG $0800
4      LDA #L2
5      STA AD
6      LDA /L2
7      STA AD+*1
8      LDA #*0
9      STA P
10     LDY AD
11     STY IA
12     LDY AD+*1
13     STY IA+*1
14     JMP (IA)
15     L2  LDA #P
16     STA AD
17     LDA /P
18     STA AD+*1
19     LDY AD
20     STY IA
21     LDY AD+*1
22     STY IA+*1
23     LDY #*0
24     LDA #*37
25     STA (IA), Y
26     JSR TS1
27     LDA #*0

```

```

28     STA IA
29     LDY AD+*1
30     STY IA+*1
31     LDY AD
32     LDA #*37
33     STA (IA), Y
34     JSR TS1
35     LDA #*11
36     STA K
37     LDA #P
38     STA T+*20
39     STA T1+*10
40     LDA /P
41     STA T+*21
42     STA T2+*10
43     LDA K
44     ASL
45     TAY
46     LDA T-*$1, Y
47     STA IA+*1
48     LDA T-*$2, Y
49     TAY
50     LDA (IA), Y
51     CMP #*0
52     BEQ L4
53     BRK
54     L4  LDA #*15
55     STA P
56     LDY K
57     LDA T2-*$1, Y
58     STA IA+*1
59     LDA T1-*$1, Y
60     TAY
61     LDA (IA), Y

```

62		CMP #15	119	STA IA2+1	0812 841A	11	STY IA
63		BEQ L5	120	LDY #10	0814 AC4009	12	LDY AD+1
64		BRK	121	LDA (IA2), Y	0817 841B	13	STY IA+1
65	L5	LDA #153	122	CMP #14	0819 6C1A00	14	JMP (IA)
66		STA P+1	123	BNE BK	081C A930	15	LDA #P
67		LDX IA	124	CLC	081E 8D3F09	16	STA AD
68		LDA #P	125	LDA #J	0821 A909	17	LDA /P
69		STA IA	126	ADC J	0823 8D4009	18	STA AD+1
70		LDA /P	127	TAY	0826 AC3F09	19	LDY AD
71		STA IA+1	128	LDA /U	0829 841A	20	STY IA
72		INC IA	129	ADC J+1	082B AC4009	21	LDY AD+1
73		BNE NXT	130	STA IA+1	082E 841B	22	STY IA+1
74		INC IA+1	131	LDA (IA), Y	0830 A000	23	LDY #0
75	NXT	LDY #0	132	CMP #14	0832 A937	24	LDA #153
76		LDA (IA), Y	133	BNE BK	0834 911A	25	STA (IA), Y
77		CMP #153	134	CLC	0836 203209	26	JSR TS1
78		BEQ L6	135	LDA /U	0839 A900	27	LDA #0
79		BRK	136	ADC J+1	083B 851A	28	STA IA
80	L6	STX IA	137	STA IA3+1	083D AC4009	29	LDY AD+1
81		LDY #P	138	LDY J	0840 841B	30	STY IA+1
82		INY	139	LDA (IA3), Y	0842 AC3F09	31	LDY AD
83		BNE NXT2	140	CMP #14	0845 A937	32	LDA #153
84		INC IA+1	141	BNE BK	0847 911A	33	STA (IA), Y
85	NXT2	LDA (IA), Y	142	BRK	0849 203209	34	JSR TS1
86		CMP #153	143	BRK	084C A911	35	LDA #11
87		BNE BK	144	ORG ++1	084E 8D4109	36	STA K
88		LDA #7	145	ORG ++1	0851 A930	37	LDA #P
89		STA P	146	LDA #153	0853 8D4209	38	STA T+1
90		LDA #9	147	CMP P	0856 8D4209	39	STA T+1
91		STA P2	148	BNE BK	0859 A909	40	LDA /P
92		LDA K	149	LDA #0	085B 8D6309	41	STA T+2
93		ASL	150	STA P	085E 8D6309	42	STA T2+1
94		TAY	151	RTS	0861 AD4109	43	LDA K
95		LDA T-1, Y	152	EP2 #18	0864 0A	44	ASL
96		STA IA2+1	153	EP2 #1A	0865 A8	45	TAY
97		LDA T-2, Y	154	EP2 #1C	0866 B94109	46	LDA T-1, Y
98		LDY #0	155	ADR L2	0869 851B	47	STA IA+1
99		LDA (IA2), Y	156	ORG ++1	086B B94009	48	LDA T-2, Y
100		CMP #7	157	ORG ++1	086E A8	49	TAY
101		BNE BK	158	T1	086F B11A	50	LDA (IA), Y
102		INY	159	T2	0871 C900	51	CMP #0
103		LDA (IA2), Y	160	ORG ++1	0873 F001	52	BEQ L4
104		CMP #9	161	J	0875 00	53	BRK
105		BNE BK	162	END	0876 A915	54	LDA #15
106		STA J	**END OF PASS 1		0878 8D3009	55	STA P
107		LDA #1	**END OF PASS 2		087B AC4109	56	LDY K
108		LDA #3	0018 320A	1	0881 851B	58	LDA T2-1, Y
109		STA J+1	0018	2	0883 B99109	59	STA IA+1
110		LDA #14	0800	3	0886 A8	60	TAY
111		STA U+351	0800 A91C	4	0887 B11A	61	LDA (IA), Y
112		CLC	0802 8D3F09	5	0889 C915	62	CMP #15
113		LDA #J	0805 A908	6	088B F001	63	BEQ L5
114		ADC J	0807 8D4009	7	088D 00	64	BRK
115		STA IA2	080A A900	8	088E A953	65	LDA #153
116		LDA /U	080C 8D3009	9	0890 8D3109	66	STA P+1
117		ADC J+1	080F AC3F09	10	0893 A61A	67	LDX IA
118							

```

0895 A930 68 LDA #P
0897 851A 69 STA IA
0899 A909 70 LDA /P
089B 851B 71 STA IA+*1
089D E61A 72 INC IA
089F D002 73 BNE NXT
08A1 E61B 74 INC IA+*1
08A3 A000 75 LDA #0
08A5 B11A 76 LDA (IA),Y
08A7 C953 77 CMP #*53
08A9 F001 78 BEQ L6
08AB 00 79 BRK
08AC 861A 80 STX IA
08AE A030 81 LDY #P
08B0 C8 82 INV
08B1 D002 83 BNE NXT2
08B3 E61B 84 INC IA+*1
08B5 B11A 85 LDA (IA),Y
08B7 C953 86 CMP #*53
08B9 D074 87 BNE BK
08BB A907 88 LDA #*7
08BD 8D3009 89 STA P
08BD 8D3009 89 LDA #*9
08BD 8D3009 89 STA P2
08C2 8D3109 91 STA P2
08C5 AD4109 92 LDA K
08C8 0A 93 ASL
08C9 A8 94 TAY
08CA B94109 95 LDA T-$1,Y
08CD 851D 96 STA IA2+*1
08CF B94009 97 LDA T-$2,Y
08D2 851C 98 STA IA2
08D4 A000 99 LDY #0
08D6 B11C 100 LDA (IA2),Y
08D8 C907 101 CMP #*7
08DA D053 102 BNE BK
08DC C8 103 INV
08DD B11C 104 LDA (IA2),Y
08DF C909 105 CMP #*9
08E1 D04C 106 BNE BK
08E3 A951 107 LDA #*51
08E5 8D320F 108 STA J
08E8 A903 109 LDA #*3
08EA 8D330F 110 STA J+*1
08ED A914 111 LDA #*14
08EF 8D830D 112 STA U+*351
08F2 18 113 CLC
08F3 A932 114 LDA #U
08F5 8D320F 115 ADC J
08F8 851C 116 STA IA2
08FA A90A 117 LDA /U
08FC 8D330F 118 ADC J+*1
08FF 851D 119 STA IA2+*1
0901 A000 120 LDY #0
0903 B11C 121 LDA (IA2),Y
0905 C914 122 CMP #*14
0907 D026 123 BNE BK

0909 18 124 CLC
090A A932 125 LDA #U
090C 8D320F 126 ADC J
090F A8 127 TAY
0910 A90A 128 LDA /U
0912 8D330F 129 ADC J+*1
0915 851B 130 STA IA+*1
0917 B11A 131 LDA (IA),Y
0919 C914 132 CMP #*14
091B D012 133 BNE BK
091D 18 134 CLC
091E A90A 135 LDA /U
0920 8D330F 136 ADC J+*1
0923 8519 137 STA IA3+*1
0925 AC320F 138 LDY J
0928 B118 139 LDA (IA3),Y
092A C914 140 CMP #*14
092C D001 141 BNE BK
092E 00 142 EN
092F 00 143 BK
0931 144 P
0932 A937 145 P2
0932 A937 145 TS1
0934 CD3009 147 CMP P
0937 D0F6 148 BNE BK
0939 A900 149 LDA #*0
093B 8D3009 150 STA P
093E 60 151 RTS
093F 152 IA3
093F 153 IA
093F 154 IA2
093F 155 AD
0942 156 K
0942 157 T
0942 158 T1
0942 159 T2
0942 160 U
0942 161 J
0942 162 J

***** END OF ASSEMBLY

*****
* SYMBOL TABLE -- V I O *
*****
LABEL LOC LABEL LOC
IA3 0018 IA 001A IA2 001C
L2 081C L4 0876 L5 088E
NXT 08A3 L4 08AC NXT2 0885
EN 092E BK 0925 P 0930
P2 0931 TS1 0932 AD 093F
K 0941 T 0942 T1 0942 T 0942
T2 09E2 U 0942 J 0F32

```

093B-	8D 30 09	STA	\$0930	0869-	85 1B	STA	\$1B	08A9-	F0 01	BE0	\$08AC
A=00	X=00 Y=00 P=33 S=E1			A=09	X=00 Y=22 P=30 S=E3			A=53	X=00 Y=00 P=33 S=E3		
093E-	60	RTS		086B-	B9 40 09	LDA	\$0940, Y	08AC-	84 1A	STX	\$1A
A=00	X=00 Y=00 P=33 S=E1			A=30	X=00 Y=22 P=30 S=E3			A=53	X=00 Y=00 P=33 S=E3		
0839-	A9 00	LDA	\$#00	086E-	A8	TAY		08AE-	A0 30	LDY	\$#30
A=00	X=00 Y=00 P=33 S=E3			A=30	X=00 Y=30 P=30 S=E3			A=53	X=00 Y=00 P=31 S=E3		
083B-	85 1A	STA	\$1A	086F-	B1 1A	LDA	(\$1A), Y	08B0-	C8	INV	
A=00	X=00 Y=00 P=33 S=E3			A=00	X=00 Y=30 P=32 S=E3			A=53	X=00 Y=31 P=31 S=E3		
083D-	AC 40 09	LDY	\$0940	0871-	C9 00	CHP	\$#00	08B1-	D0 02	BNE	\$08B5
A=00	X=00 Y=09 P=31 S=E3			A=00	X=00 Y=30 P=33 S=E3			A=53	X=00 Y=31 P=31 S=E3		
0840-	84 1B	STY	\$1B	0873-	F0 01	BE0	\$0876	08B5-	B1 1A	LDA	(\$1A), Y
A=00	X=00 Y=09 P=31 S=E3			A=00	X=00 Y=30 P=33 S=E3			08B7-	C9 53	CHP	\$#53
0842-	AC 3F 09	LDY	\$093F	0876-	A9 15	LDA	\$#15	08B9-	D0 74	BNE	\$092F
A=00	X=00 Y=30 P=31 S=E3			A=15	X=00 Y=30 P=31 S=E3			08BB-	A9 07	LDA	\$#07
0845-	A9 37	LDA	\$#37	0878-	8D 30 09	STA	\$0930	08BD-	8D 30 09	STA	\$0930
A=37	X=00 Y=30 P=31 S=E3			A=15	X=00 Y=30 P=31 S=E3			08C0-	A9 09	LDA	\$#09
0847-	91 1A	STA	(\$1A), Y	087B-	AC 41 09	LDY	\$0941	08C2-	8D 31 09	STA	\$0931
A=37	X=00 Y=30 P=31 S=E3			A=15	X=00 Y=11 P=31 S=E3			08C3-	AD 41 09	LDA	\$0941
0849-	20 32 09	JSR	\$0932	087E-	B9 E1 09	LDA	\$09E1, Y	08C8-	0A	ASL	
A=37	X=00 Y=30 P=31 S=E3			A=09	X=00 Y=11 P=31 S=E3			08C9-	A8	TAY	
0932-	A9 37	LDA	\$#37	0881-	85 1B	STA	\$1B	08CA-	B9 41 09	LDA	\$0941, Y
A=37	X=00 Y=30 P=31 S=E1			A=09	X=00 Y=11 P=31 S=E3			08CD-	85 1D	STA	\$1D
0934-	CD 30 09	CHP	\$0930	0883-	B9 91 09	LDA	\$0991, Y	08CF-	B9 40 09	LDA	\$0940, Y
A=37	X=00 Y=30 P=33 S=E1			A=30	X=00 Y=11 P=31 S=E3			08D2-	85 1C	STA	\$1C
0937-	D0 F6	BNE	\$092F	0886-	A8	TAY		08D4-	A0 00	LDY	\$#00
A=37	X=00 Y=30 P=33 S=E1			A=30	X=00 Y=30 P=31 S=E3			08D6-	B1 1C	LDA	(\$1C), Y
0939-	A9 00	LDA	\$#00	0887-	B1 1A	LDA	(\$1A), Y	08D8-	C9 07	CHP	\$#07
A=00	X=00 Y=30 P=33 S=E1			A=15	X=00 Y=30 P=31 S=E3			08DA-	D0 53	BNE	\$092F
093B-	8D 30 09	STA	\$0930	0889-	C9 15	CHP	\$#15	08DC-	C8	INV	
A=00	X=00 Y=30 P=33 S=E1			A=15	X=00 Y=30 P=33 S=E3			08DD-	B1 1C	LDA	(\$1C), Y
093E-	60	RTS		088B-	F0 01	BE0	\$088E	08DF-	C9 09	CHP	\$#09
A=00	X=00 Y=30 P=33 S=E1			088E-	A9 53	LDA	\$#53	08E1-	D0 4C	BNE	\$092F
084C-	A9 11	LDA	\$#11	0890-	8D 31 09	STA	\$0931	08E3-	A9 51	LDA	\$#51
A=11	X=00 Y=30 P=31 S=E3			A=53	X=00 Y=30 P=31 S=E3			A=51	X=00 Y=01 P=31 S=E3		
084E-	8D 41 09	STA	\$0941	0893-	A6 1A	LDY	\$1A				
A=11	X=00 Y=30 P=31 S=E3			0895-	A9 30	LDA	\$#30				
0851-	A9 30	LDA	\$#30	0897-	85 1A	STA	\$1A				
A=30	X=00 Y=30 P=31 S=E3			A=30	X=00 Y=30 P=31 S=E3						
0853-	8D 42 09	STA	\$0942	0899-	A9 09	LDA	\$#09				
A=30	X=00 Y=30 P=31 S=E3			A=09	X=00 Y=30 P=31 S=E3						
0856-	8D A2 09	STA	\$09A2	089B-	85 1B	STA	\$1B				
A=30	X=00 Y=30 P=31 S=E3			A=09	X=00 Y=30 P=31 S=E3						
0859-	A9 09	LDA	\$#09	089D-	E6 1A	INC	\$1A				
A=09	X=00 Y=30 P=31 S=E3			089F-	D0 02	BNE	\$09A3				
085B-	8D 63 09	STA	\$0963	08A3-	A0 00	LDY	\$#00				
A=09	X=00 Y=30 P=31 S=E3			08A5-	B1 1A	LDA	(\$1A), Y				
085E-	8D F2 09	STA	\$09F2	08A7-	C9 53	CHP	\$#53				
A=09	X=00 Y=30 P=31 S=E3			A=53	X=00 Y=00 P=33 S=E3						
0861-	AD 41 09	LDA	\$0941								
A=11	X=00 Y=30 P=31 S=E3										
0864-	0A	ASL									
A=22	X=00 Y=30 P=30 S=E3										
0865-	AB	TAY									
A=22	X=00 Y=22 P=30 S=E3										
0866-	B9 41 09	LDA	\$0941, Y								
A=09	X=00 Y=22 P=30 S=E3										

08E5-	8D 32 0F	STA	\$0F32	090C-	6D 32 0F	ADC	\$0F32
A=51	X=00 Y=01 P=31	S=E3		A=83	X=00 Y=00 P=F0	S=E3	
08E8-	A9 03	LDA	##03	090F-	A8	TAY	
A=03	X=00 Y=01 P=31	S=E3		A=83	X=00 Y=83 P=F0	S=E3	
08EA-	8D 33 0F	STA	\$0F33	0910-	A9 0A	LDA	##0A
A=03	X=00 Y=01 P=31	S=E3		A=0A	X=00 Y=83 P=70	S=E3	
08ED-	A9 14	LDA	##14	0912-	6D 33 0F	ADC	\$0F33
A=14	X=00 Y=01 P=31	S=E3		A=0D	X=00 Y=83 P=30	S=E3	
08EF-	8D 83 0D	STA	\$0D83	0915-	85 1B	STA	\$1B
A=14	X=00 Y=01 P=31	S=E3		A=0D	X=00 Y=83 P=30	S=E3	
08F2-	18	CLC		0917-	B1 1A	LDA	(\$1A), Y
A=14	X=00 Y=01 P=30	S=E3		A=14	X=00 Y=83 P=30	S=E3	
08F3-	A9 32	LDA	##32	0919-	C9 14	CMP	##14
A=32	X=00 Y=01 P=30	S=E3		A=14	X=00 Y=83 P=33	S=E3	
08F5-	6D 32 0F	ADC	\$0F32	091B-	D0 12	BNE	\$092F
A=83	X=00 Y=01 P=F0	S=E3		A=14	X=00 Y=83 P=33	S=E3	
08F8-	85 1C	STA	\$1C	091D-	18	CLC	
A=83	X=00 Y=01 P=F0	S=E3		A=14	X=00 Y=83 P=32	S=E3	
08FA-	A9 0A	LDA	##0A	091E-	A9 0A	LDA	##0A
A=0A	X=00 Y=01 P=70	S=E3		A=0A	X=00 Y=83 P=30	S=E3	
08FC-	6D 33 0F	ADC	\$0F33	0920-	6D 33 0F	ADC	\$0F33
A=0D	X=00 Y=01 P=30	S=E3		A=0D	X=00 Y=83 P=30	S=E3	
08FF-	85 1D	STA	\$1D	0923-	85 19	STA	\$19
A=0D	X=00 Y=01 P=30	S=E3		A=0D	X=00 Y=83 P=30	S=E3	
0901-	A0 00	LDY	##00	0925-	AC 32 0F	LDY	\$0F32
A=0D	X=00 Y=00 P=32	S=E3		A=0D	X=00 Y=51 P=30	S=E3	
0903-	B1 1C	LDA	(\$1C), Y	0928-	B1 18	LDA	(\$18), Y
A=14	X=00 Y=00 P=30	S=E3		A=14	X=00 Y=51 P=30	S=E3	
0905-	C9 14	CMP	##14	092A-	C9 14	CMP	##14
A=14	X=00 Y=00 P=33	S=E3		A=14	X=00 Y=51 P=33	S=E3	
0907-	D0 26	BNE	\$092F	092C-	D0 01	BNE	\$092F
A=14	X=00 Y=00 P=33	S=E3		A=14	X=00 Y=51 P=33	S=E3	
0909-	18	CLC		092E-	00	BRK	
A=14	X=00 Y=00 P=32	S=E3		092E-	A=14 X=00 Y=51 P=33	S=E3	
090A-	A9 32	LDA	##32	*0800G			
A=32	X=00 Y=00 P=30	S=E3		0930-	A=14 X=00 Y=51 P=33	S=DF	



This interface will allow the USART, package 3A, and the software which controls it to interface the H-14 at any baud rate up to and including 4800.

Sincerely,
Robert Rennard

2281 Cobble Stone Court
Dayton, OH 45431

CP/M COMPATIBLE SOFTWARE MARKETING

Dear DDJ:

As the developers of CP/M and MP/M, Digital Research is preparing a list of vendors of CP/M-compatible software. We would appreciate the help of readers of your magazine in compiling this list for distribution to all interested persons who contact us.

If any readers are currently marketing CP/M-compatible software, please send us any or all literature pertaining to your software which controls it to interface the H-14 at any baud rate up to and including 4800.

Thank you,
Marilyn Darling

Digital Research
P.O. Box 579
Pacific Grove, CA 93950

AT ODDS WITH DDJ

Dear DDJ:

I have received my copies of Volume 5, Issue 8 of DDJ, which contains my article (*A Note On 6502 Indirect Addressing*), and I am slightly upset.

I have about 70 papers to my credit, in all kinds of journals, and this is the *very first time* that I have not had the courtesy of having galley proofs to review before an article of mine is printed.

I understand about your policy of quick publication; I want to see my ideas on programming published as quickly as possible, too—but not with typists' mistakes still in them! Typists are not infallible, nor should they be expected to be. For the record, the mistakes were as follows:

P. 26 col. 1 line 37: "is keep" should be "is to keep"
P. 26 col. 3 line 34: left paren should line up under I
P. 27 col. 1 line 57: "each by" should be "each time by"
P. 27 col. 3 line 11: [1] refers to *reference number 1*, which is not marked as such. (I don't mind if you want to set up your own conventional notation for references to journal papers and books, but it has to be consistent with itself.)

None of these turned out to be really serious, in this case—which is why I am slightly, rather than considerably, upset.

Sincerely,
Professor W. D. Maurer

George Washington University
S.E.A.S.
Washington, DC 20052

Prof. Maurer's objection is well taken and the subject of this month's editorial (see p. 1). —JP

SIGNED COMPARISON: ALTERNATE ROUTINE

Dear DDJ:

While scanning the listing of the runtime library for the Small C compiler in issue #48, I happened to notice the signed compare routine ("ccomp"). This routine performs a comparison of two 16-bit signed numbers (two's complement) by subtracting one of the numbers from the other and then examining the sign of the result. This technique works fine as long as the difference between the numbers being compared is less

than or equal to 32767; however, if the numbers differ by more than 32767, the result of the compare will be incorrect due to arithmetic overflow during the calculation.

A different way to accomplish a signed comparison is to invert the sign bits of the two numbers being compared and then to perform an unsigned compare using the new numbers. A routine using this technique is shown below:

```
; Common routine to perform a signed compare of DE & HL.
; This routine compares DE & HL and sets the conditions:
;   Carry reflects sign of difference (set if DE < HL)
;   Zero/non-zero set according to equality.
;
ccomp: MOV  A,H      ; invert sign of HL.
       XRI  80H
       MOV  H,A

       MOV  A,D      ; invert sign of DE.
       XRI  80H

       CMP  H        ; compare msbs.
       JNZ  cccmpl    ; unequal—comparison done.

       MOV  A,E      ; equal—compare lsbs.
       CMP  L

ccmpl: LXI  H,1      ; (required by Small C).
       RET
```

This new method works by mapping the signed number domain into the unsigned number domain, where 16-bit comparisons may be easily made, before making the comparison. A few examples of number mappings are shown below:

Decimal number	Hex number before map	Hex number after map
-32768	8000	0000
-32767	8001	0001
...		
-1	FFFF	7FFF
0	0000	8000
1	0001	8001
...		
32767	7FFF	FFFF

Now, does this solve a problem or just create a new problem? Consider the two expressions shown below, which appear to be equivalent:

Expression	New result	Old result	"Correct" result
(-4000 < 30000)	True	False	True
(-4000 - 30000 < 0)	False	False	False

Because of arithmetic overflow in the second expression, where "-4000 - 30000" is correctly interpreted as 31536 (not -34000), the expressions have different values. The new "improved" compare yields the differing results, depending upon how the expression is formed; whereas the old compare yields identical (but incorrect in one case) results no matter which way the expression is formed. Which attribute appeals to you more: correctness or apparent consistency? I vote for correctness in this case.

Yours truly,
Harry B. Stewart

Neoteric
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