



MICROCOMPUTERS

MOS TECHNOLOGY, INC.

VALLEY FORGE CORPORATE CENTER (215) 666-7950
950 RITTENHOUSE ROAD, NORRISTOWN, PA. 19401

BULK RATE

Permit No.

925

Norristown, Pa.

19401



MOS TECHNOLOGY, INC.

VALLEY FORGE CORPORATE CENTER

950 RITTENHOUSE ROAD • NORRISTOWN, PA. 19401

TO

CARNEGIE MELLON UNIVERSITY
D/PHYSICS
5000 FORBES AVE
PITTSBURGH PA
MR BOB FINDLAY

15213

D



APRIL, 1976

We know you will be pleased that MOS TECHNOLOGY, INC. and Motorola have settled their suit and countersuit and have signed a patent cross license covering both company's microcomputer lines. We really appreciated your expressions of support during the past few months. As part of the overall settlement, MOS TECHNOLOGY, INC. has agreed to withdraw the MCS6501 from the marketplace - thus ending any sensitivity about compatibility.

Now that we're at peace, here's some good news for everyone on our mailing list - we are introducing five new microprocessors in June and three new I/O products later in the summer. The MCS6506 is a 28 lead microprocessor with both ϕ_1 (OUT) and ϕ_2 (OUT) made available and with on-the-chip clock. The MCS6512, MCS6513, MCS6514, and MCS6515 are the counterparts, functionally, to the MCS6502, MCS6503, MCS6504 and MCS6505 with the difference being a two phase clock input on the new products. This line of new microprocessors is especially suited to multi-processor systems where maximum control of timing relationships is of paramount importance as well as utilization of memory sharing wherever possible to save on system costs. Included in this newsletter are pinout diagrams of the entire current microprocessor family (all nine microprocessors) which are all software compatible and will be available in maximum frequencies of 1MHz and 2MHz. The new devices will be available for sampling in June at the same low prices you have come to expect from MOS TECHNOLOGY, INC. The 1-99 pricing will be \$20.00 for the 40 lead MCS6512 and 28 lead MCS6506 with on-board clock, and \$18.00 for the 28 lead MCS6513, MCS6514 and MCS6515.

New I/O products due for introduction in the next few months will include the MCS6520, MCS6522 and MCS6532.

The MCS6520 is a direct replacement for the MC6820, Motorola's "Peripheral Interface Adapter". As such, it will contain the same powerful features (data direction registers, control register, dual eight bit peripheral ports, handshake capability, etc.) as the popular "PIA". We would like to point out that this chip was designed by our second source, Synertek, in Santa Clara - the relationship between the two companies is indeed one characterized by efficiency, mutual support, and above all productivity.

The MCS6522 will contain essentially the same basic features of the MCS6520 and in addition will include latching on the peripheral data ports, a register for serial capability, and two programmable interval timers. Termed the "Versatile Interface Adapter" or "VIA", this product will find use in nearly all microcomputer systems requiring special timing functions and/or serial stream data flow.

The MCS6532 is similar to our MCS6530 "Combo" chip except we have deleted the ROM but doubled the RAM size to 128 x 8. The chip continues to have essentially the same I/O and Timer features with 16 bi-directional peripheral data pins and a programmable interval timer. The chip is designed for those applications where more RAM than the 64 bytes of the MCS6530 is needed - hence the increase to 128 bytes of RAM. Exclusion of the 1024 x 8 ROM allows the user to go to larger off board ROM or PROM for program storage.

More details on all of our new products will follow in our next newsletter, with data sheets on the new I/O products available with the samples this summer. Until then, thanks for your support and interest in the broadest microprocessor family in the industry.

MOS TECHNOLOGY, INC.

V _{ss}	1	40	RES
RDY	2	39	Ø2(OUT)
Ø1(OUT)	3	38	S.O.
IRQ	4	37	Ø0(IN)
N.C.	5	36	N.C.
NMI	6	35	N.C.
SYNC	7	34	R/W
V _{cc}	8	33	DB0
AB0	9	32	DB1
AB1	10	31	DB2
AB2	11	30	DB3
AB3	12	29	DB4
AB4	13	28	DB5
AB5	14	27	DB6
AB6	15	26	DB7
AB7	16	25	AB15
AB8	17	24	AB14
AB9	18	23	AB13
AB10	19	22	AB12
AB11	20	21	V _{ss}

MCS6502

RES	1	28	Ø2(OUT)
V _{ss}	2	27	Ø0(IN)
IRQ	3	26	R/W
NMI	4	25	DB0
V _{cc}	5	24	DB1
AB0	6	23	DB2
AB1	7	22	DB3
AB2	8	21	DB4
AB3	9	20	DB5
AB4	10	19	DB6
AB5	11	18	DB7
AB6	12	17	AB11
AB7	13	16	AB10
AB8	14	15	AB9

MCS6503

V _{ss}	1	40	RES
RDY	2	39	Ø2(OUT)
Ø1	3	38	S.O.
IRQ	4	37	Ø2
V _{ss}	5	36	DBE
NMI	6	35	N.C.
SYNC	7	34	R/W
V _{cc}	8	33	DB0
AB0	9	32	DB1
AB1	10	31	DB2
AB2	11	30	DB3
AB3	12	29	DB4
AB4	13	28	DB5
AB5	14	27	DB6
AB6	15	26	DB7
AB7	16	25	AB15
AB8	17	24	AB14
AB9	18	23	AB13
AB10	19	22	AB12
AB11	20	21	V _{ss}

MCS6512

RES	1	28	Ø2(OUT)
V _{ss}	2	27	Ø0(IN)
IRQ	3	26	R/W
V _{cc}	4	25	DB0
AB0	5	24	DB1
AB1	6	23	DB2
AB2	7	22	DB3
AB3	8	21	DB4
AB4	9	20	DB5
AB5	10	19	DB6
AB6	11	18	DB7
AB7	12	17	AB12
AB8	13	16	AB11
AB9	14	15	AB10

MCS6504

V _{ss}	1	28	RES
Ø1	2	27	Ø2
IRQ	3	26	R/W
NMI	4	25	DB0
V _{cc}	5	24	DB1
AB0	6	23	DB2
AB1	7	22	DB3
AB2	8	21	DB4
AB3	9	20	DB5
AB4	10	19	DB6
AB5	11	18	DB7
AB6	12	17	AB11
AB7	13	16	AB10
AB8	14	15	AB9

MCS6513

RES	1	28	Ø2(OUT)
V _{ss}	2	27	Ø0(IN)
RDY	3	26	R/W
IRQ	4	25	DB0
V _{cc}	5	24	DB1
AB0	6	23	DB2
AB1	7	22	DB3
AB2	8	21	DB4
AB3	9	20	DB5
AB4	10	19	DB6
AB5	11	18	DB7
AB6	12	17	AB11
AB7	13	16	AB10
AB8	14	15	AB9

MCS6505

V _{ss}	1	28	RES
Ø1	2	27	Ø2
IRQ	3	26	R/W
V _{cc}	4	25	DB0
AB0	5	24	DB1
AB1	6	23	DB2
AB2	7	22	DB3
AB3	8	21	DB4
AB4	9	20	DB5
AB5	10	19	DB6
AB6	11	18	DB7
AB7	12	17	AB12
AB8	13	16	AB11
AB9	14	15	AB10

MCS6514

RES	1	28	Ø2(OUT)
V _{ss}	2	27	Ø0(IN)
Ø1(OUT)	3	26	R/W
IRQ	4	25	DB0
V _{cc}	5	24	DB1
AB0	6	23	DB2
AB1	7	22	DB3
AB2	8	21	DB4
AB3	9	20	DB5
AB4	10	19	DB6
AB5	11	18	DB7
AB6	12	17	AB11
AB7	13	16	AB10
AB8	14	15	AB9

MCS6506

V _{ss}	1	28	RES
RDY	2	27	Ø2
Ø1	3	26	R/W
IRQ	4	25	DB0
V _{cc}	5	24	DB1
AB0	6	23	DB2
AB1	7	22	DB3
AB2	8	21	DB4
AB3	9	20	DB5
AB4	10	19	DB6
AB5	11	18	DB7
AB6	12	17	AB11
AB7	13	16	AB10
AB8	14	15	AB9

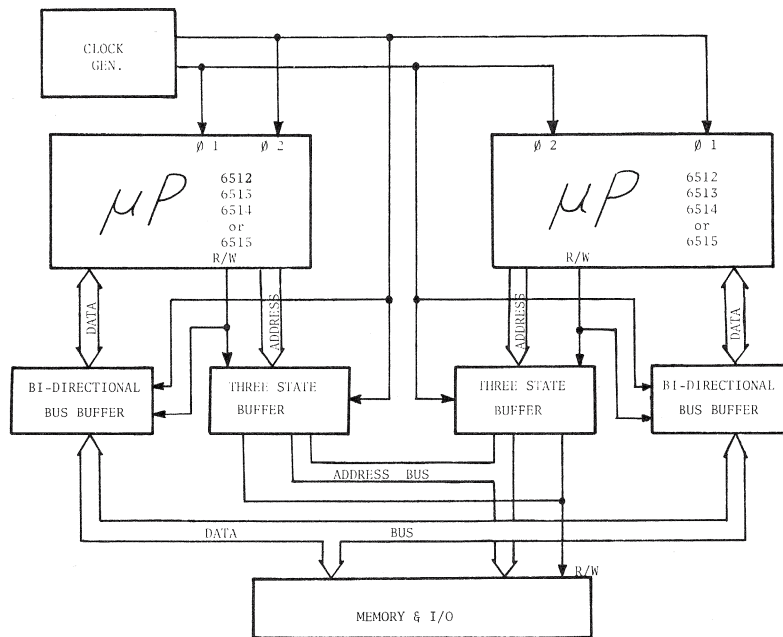
MCS6515

MCS6500
MICROPROCESSOR
FAMILY

*9 MICRO'S

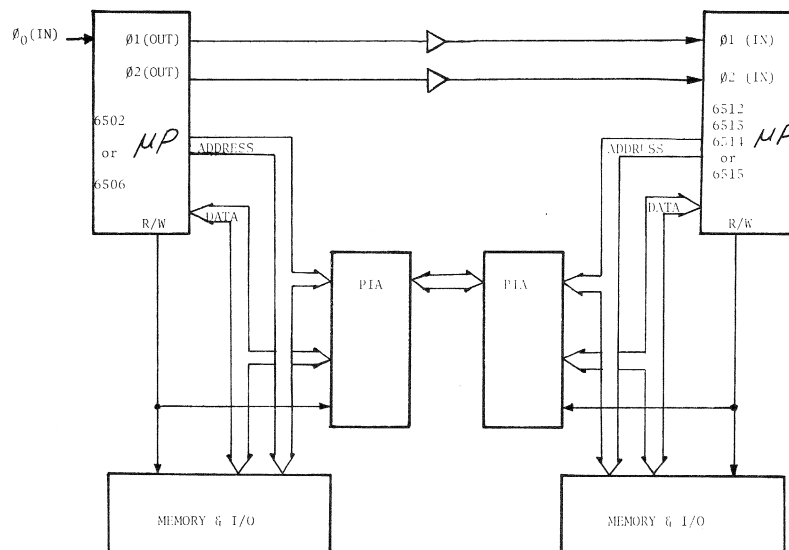
*ALL SOFTWARE
COMPATIBLE

*UP TO 2MHZ
CLOCK RATE



This configuration allows two microprocessors to share memory and I/O by accessing memory during opposite phases of the system clock.

MULTIPLE PROCESSORS DRIVEN FROM EXTERNAL CLOCK



This configuration allows multiple processors to communicate through peripheral adapters.

MULTIPLE PROCESSOR SYSTEMS DRIVEN BY ON-CHIP CLOCK

**this document was
generously contributed by:
Barry Luokkala
Department of Physics,
Carnegie Mellon University**

scanned by:
www.commodore.international
2023-06-27