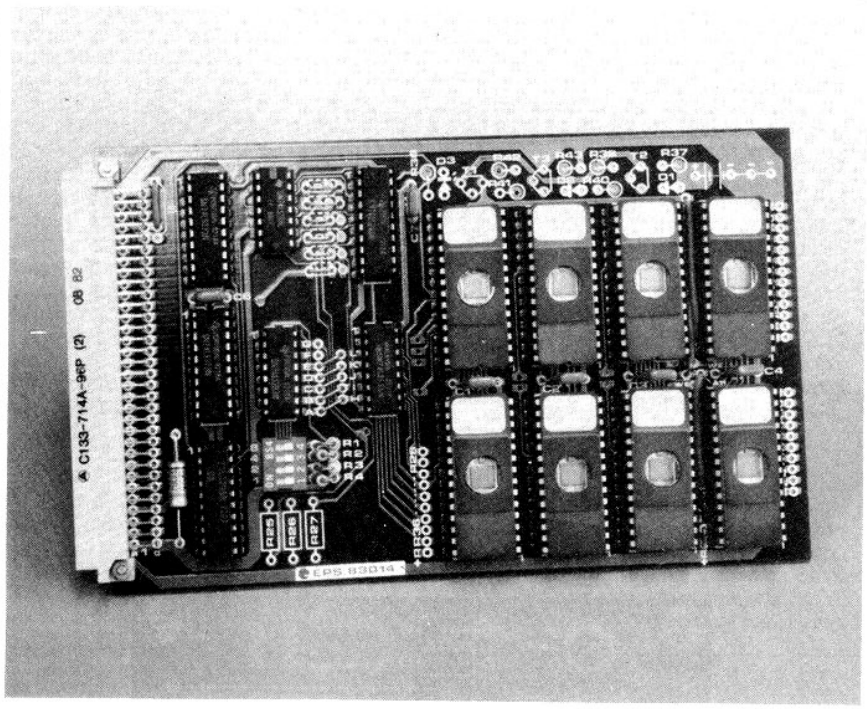


The continuing development of 'bigger' memory ICs obliges us to develop new, versatile and more powerful RAM/EPROM cards at regular intervals. The universal memory card described here is suitable for most microcomputers with an 8-bit data bus and it can accept up to 64 K RAM or EPROM. A combination of both types of memory is also possible. If CMOS RAMs are utilised, a backup battery will protect the memory contents for a considerable time, thus preventing the data from being lost when the computer is switched off (power-down).

universal memory card

64 K RAM and/or EPROM with battery backup

The computer memory

In general, a microcomputer system contains the sections shown in figure 1. The microprocessor chip contains various registers, the program counter and the arithmetic and logic unit (ALU); the clock generator may also be included on-chip in certain microprocessor types. The other main section is the memory, usually consisting of both RAM and ROM or (E)PROM. The data to be processed are stored in the RAM and called as required; the EPROM contains 'permanent' operating instructions for the microprocessor. In most cases the so-called operating program (monitor) for the microcomputer is resident in this section of memory.
Addresses, data and control signals processed and output by the computer are transferred via the address bus, data bus and control signal bus. It would be beyond the scope of this article to consider the many details that must be taken into account when utilising the basic system of figure 1 with a particular microprocessor. Instead, we shall take a closer look at the data memory and program memory block.
Those readers who have worked with the Elektor SC/MP system or Junior Computer from the start know how quickly the maximum memory capacity of a basic system is reached. No wonder we had to meet the demand for bigger memories by developing 4 K RAM, 8 K RAM/EPROM and 16 K 'dynamic' RAM cards. This progress was possible because the need for greater memories was also experienced commercially, stimulating manufacturers to develop and produce 'bigger' ICs.

Dedicated systems as opposed to development systems

A development system can also be used for 'dedicated' applications, but the reverse is

1

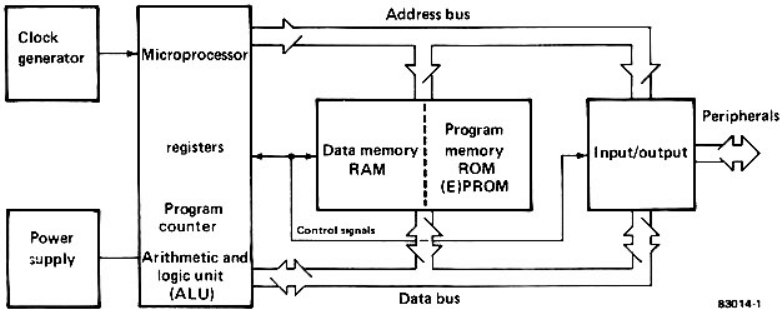


Figure 1. In general, a microcomputer system consists of the microprocessor and two distinct types of memory. The data to be processed are stored in the (RAM) data memory and called as required. The program memory contains the operating program (monitor) for the microcomputer. This is stored in ROM or (E)PROM.

2

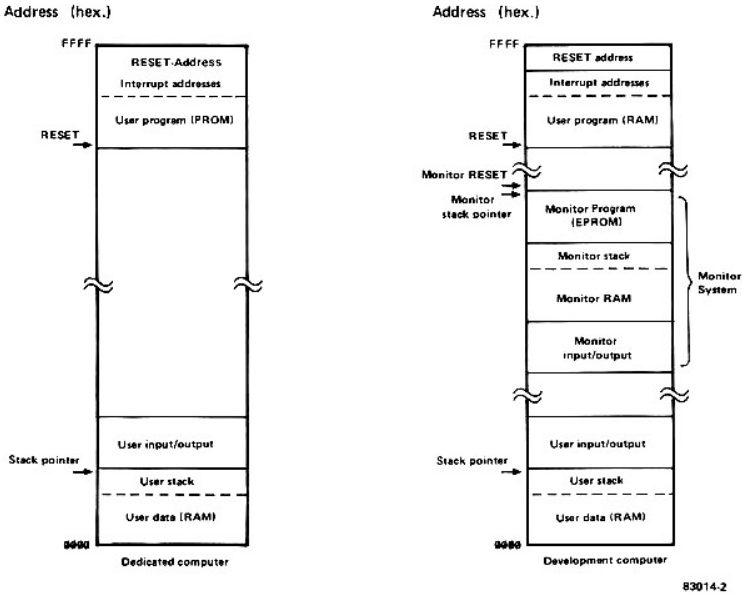


Figure 2. Development computers, such as the Junior or SC/MP, use RAMs in the program memory area. A large part of the addressable memory area is occupied by the monitor program, in ROM or (E)PROM, with its associated 'monitor RAM' area. Dedicated computers such as Intelekt, the 6502 housekeeper and the darkroom computer are more common. Their program memories consist of an (E)PROM. The large monitor memory is not required.

not true. The difference between a dedicated system and a development system is shown in figure 2. The computers that tend to run out of memory space are the development systems (SC/MP, Junior and so on). Their data and program memories are typically organised as in figure 2. RAMs are used in the program memory area. The monitor program occupies a large part of the addressable memory area. It consists of a ROM or (E)PROM containing the operating instructions, a RAM area for intermediate storage and a memory-mapped input/output block. The monitor program itself contains various routines that are needed for developing other programs, such as: input/output routines, memory scan and memory input. Elektor has published several 'dedicated computers', such as Intelekt, the 6502 housekeeper and the darkroom computer. Their program memories consist of an EPROM. A monitor is not required, thus obviating the need for the large monitor memory.

But, to get back to the development computer: a 16-bit address bus can define and call a total of $2^{16} = 65536 = 64$ K addresses. (The location of an address is normally expressed in hexadecimal: thus an address range of 0000_{hex} to $FFFF_{hex}$ covers 64 K.) Given this fact, it would seem logical to provide a microcomputer system with a 64 K memory from the outset. However, this is the exception rather than the rule – mainly because that type of memory was too bulky and expensive until quite recently!

Memory development at Elektor

Figure 3 shows the development of Elektor memory cards. In March 1978, when the memory card for the SC/MP system was introduced, only MOS ICs with an organisation of 256 x 4 bits were available. This meant that 32 ICs were needed for a 4 K

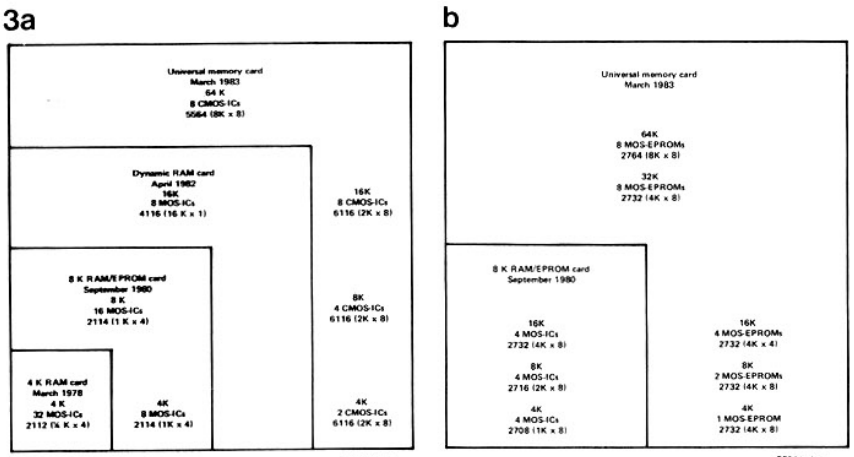
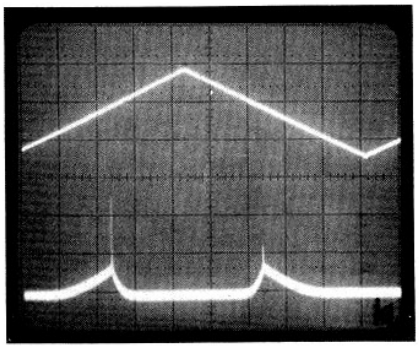


Figure 3. The development of Elektor RAM and/or EPROM memory cards. From 4 K RAM in 1978 to 64 K in 1983 and from 16 K EPROM in 1980 to 64 K in 1983, with the same space requirement in each case. Although not shown, 2716 2 K EPROMs can also be mounted on the universal memory card. The types indicated stand for the device type: '2716' means 'a 2 K x 8 EPROM', say, and '6116' means 'a 2 K x 8 RAM'.

memory. Nowadays the same memory capacity can be achieved with only two 6116 CMOS ICs. In the near future, 8 K x 8 CMOS RAMs will be available – making it possible to store 65536 bytes on a single 'universal memory card'!
PROMs and EPROMs reached this stage of development some time ago, and 65536 bytes can also be stored in eight MOS EPROMs on the universal memory card. (In fact, even 32 K x 8 CMOS PROMs are now available. Only two of these ICs would therefore be needed in order to store the total 62 K! However, these ICs are not suitable for the universal memory card.)
For the computer hobbyist the development of 'bigger' memory ICs means that a single Eurocard will now provide as much memory as 16 cards did 4 years ago. Over the same period, the cost of memories has dropped considerably: 4 K of RAM cost about 80 pounds then, but now (using 6116's) the same storage area costs less than 10 pounds!

The universal memory card

Figure 4 is the circuit diagram of the universal memory card. 2 K (2716), 4 K (2732) or 8 K (2764) EPROMs and 2 K (6116) or 8 K (5564) CMOS RAMs can be used. The type numbers in parentheses stand for all memory ICs with the same organisation and same pin assignments.
Two versions of this memory card can be built: with or without battery backup (CMOS version or MOS version respectively). In the former case the power supply for the *CMOS* RAMs is backed up with two miniature cells so that the data are not lost when the computer is switched off. Mixed operation (CMOS *and* MOS ICs) is not possible, nor would it serve any useful purpose. The battery would be quickly discharged and T1 would not be capable of supplying the necessary current.
In the CMOS version, the circuit draws approximately 200 mA in operation. Only one RAM is accessed at a time and this draws approximately 35 mA. However, the rest of the circuit requires about 165 mA. The average operation current for a RAM is less than 35 mA. The figure depends on the number of times the RAM is accessed in a given period. The quiescent current of the RAM ($\overline{CE}$ = 1) is only a few μA. One more important point: the CMOS version requires pull-down resistors, open-collector ICs and the circuit associated with T1 . . . T3.
When the supply voltage is switched off (power-down) inputs $\overline{CE}$ or $\overline{OE}$ and $\overline{WE}$ of the RAMs *must* be inhibited (logic 1). Open-collector ICs with pull-up resistors to the battery supply rail are used for this reason: the inputs will automatically go to logic 1 and inhibit the RAMs.
Pull-down resistors are also required for (some) CMOS RAMs. The reason is illustrated in photograph 1. The upper trace is



the voltage on one of the address lines of a Hitachi 6116 CMOS RAM, and shown below it is the current drawn by this IC. There are no pull-up or pull-down resistors. At approximately half the operating voltage (one half of 2.4 V in this case), the current rises considerably (up to approximately 200 μA). The same effect occurs at each of the 11 address lines, so that the total current can be 2.2 mA instead of 'typically 2 μA', as specified in the datasheet for the HM 6116 LP. To avoid this problem, pull-down resistors are essential: a current which is greater than expected by a factor of 1000 will quickly discharge the battery!
This heavy current consumption occurs when a floating address input causes both CMOS transistors conduct. This is not always the case, nor does it apply to all

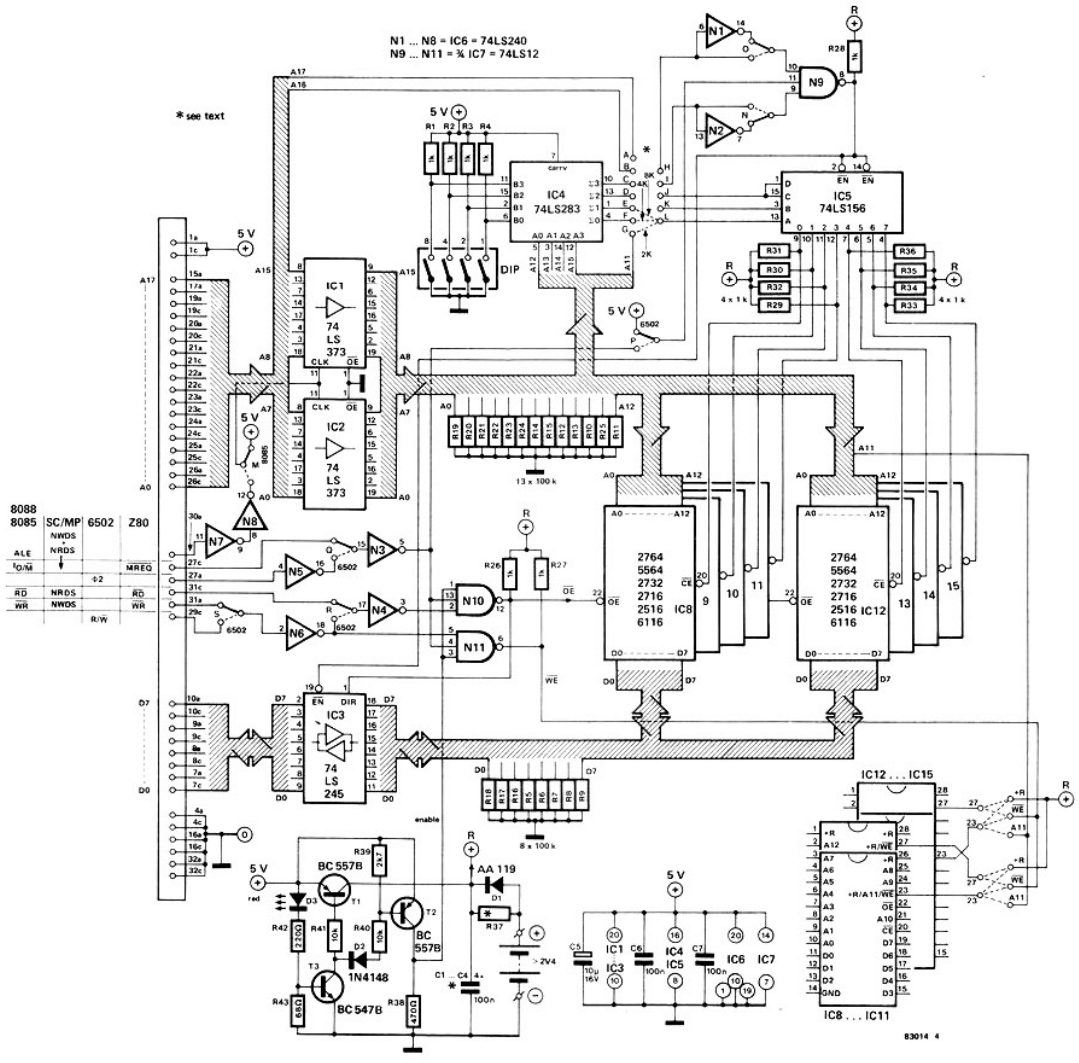
inputs. The 6116, for example, doesn't need pull-down resistors for the data lines. With ICs from other manufacturers, the situation may be different. The best solution is to play it safe, and mount all resistors shown. They cannot do any harm, and there is room for them on the printed circuit board.
The MOS version has a higher quiescent current consumption. MOS devices can be used for all the RAMs and EPROMs; the advantage is that these ICs cost only half as much as the CMOS devices. The disadvantage is that each 2716 EPROM, for example, draws a *quiescent* current of about 35 mA. Multiplied by 8: nearly 300 mA. Add about 165 mA for the rest of the circuit: a total quiescent current of 450 mA! The MOS version does not need open-collector ICs, and all the resistors are omitted except for R1 . . . R4. The circuit associated with T1 . . . T3 is not required, and wire links are inserted in place of the collector-emitter paths of the transistors T1 and T2.
The address and data lines are fully buffered except for A16 and A17. However, A16 and A17 are rarely utilised. The card need not have a full complement of ICs, of course: it will also operate perfectly with only one EPROM or RAM.

Address decoding

The address decoding is unusual. The addresses are summed in two's complement. This corresponds to a subtraction, as shown in the example (next page). If the address selected on the board corresponds to the incoming address, the result is zero. The actual address decoder IC5 is then enabled via N9 and generates the $\overline{CE}$ signal that selects the appropriate RAM or EPROM.

Figure 4. Two versions in one circuit diagram. The MOS version is less expensive and less involved. It merely contains resistors R1 . . . R4, capacitors C1 . . . C7, IC1 . . . IC7 and IC8 . . . IC15, as required (from 1 to 8 devices). Wire links are used for matching to different processors and memory ICs. IC5 and IC7 are different types than with the CMOS version. With the CMOS version a permanent memory can be created whose data will not be lost. Nickel cadmium rechargeable cells or disposable batteries are used to provide backup when the operating voltage is switched off. A power-down circuit with T1 . . . T3 is also provided.

4



As an example, assume that the address 8000$_{hex}$ is selected with the DIP switches. In accordance with the two's *complement* method, only switch 'A15' is closed (see $\overline{B}$ in the calculation). The *two's* complement is obtained by adding a 1 to the carry input of IC4 (pin 7). Now, if 1000 is also available at the A-inputs of IC4 (for the 8000 address block), the information 0000 appears at the outputs. Let us assume that the wire links for 2 K RAMs or EPROMs are inserted; then IC5 sees 000 at its A, B and C-inputs ('A11' is also 0 for this address block). The activating signal, logic zero, is also present at the enable inputs (pin 2 and pin 14), via N9. Thus the address decoder is switched on and provides a $\overline{CE}$ signal for IC8 at output 0. This RAM or EPROM is enabled.
Next, let us assume that address 8800 appears. There is a logic 1 on address line A11 but the output from IC4 is still '0000'. The address decoder switches to the next 2 K RAM or EPROM. Readers who feel like trying their hand at binary and hexadecimal calculations can work out other examples and create a memory chart for all possible settings of the DIP switches and wire links A . . . L. The example shows that 2, 4 and 8 K ICs cannot be mixed easily.

If the memory area is organised in 8 K blocks, the card will respond to all possible 64 K addresses (even if ICs are not mounted in all positions). If, for example, the address 8000 is selected, the memory is scanned from 8000 to FFFF, and then from (1)0000 to (1)7FFF! If the monitor is located somewhere in this area, something is bound to go wrong. There is a way of avoiding this, however: memory areas can be blocked with address lines A16 and A17 as required. The way in which this is done must be worked out in each case. Once again, the calculation example should be consulted. Wire links '0' and 'N' at N1 and N2 can be used to select 'active low' or 'active high' control. A logic 0 must be present at the output of N9 (i.e. a logic 1 at all inputs) for IC5 to be activated.

Example of calculation with two's complement:

B	= 1000 =	8_{hex}
$\overline{B}$	= 0111	
+1	1	two's
	1000	complement
A	= 1000	+
	(1) 0000	

Control signals

The control signals provided by the different types of processors are listed in the table in figure 4, next to terminals 27, 31 and 29. The 8085 processor cannot be connected without modifications, since the data and addresses must be de-multiplexed before they are applied to the memory card. The data bus buffer outputs data when the $\overline{RD}$

5

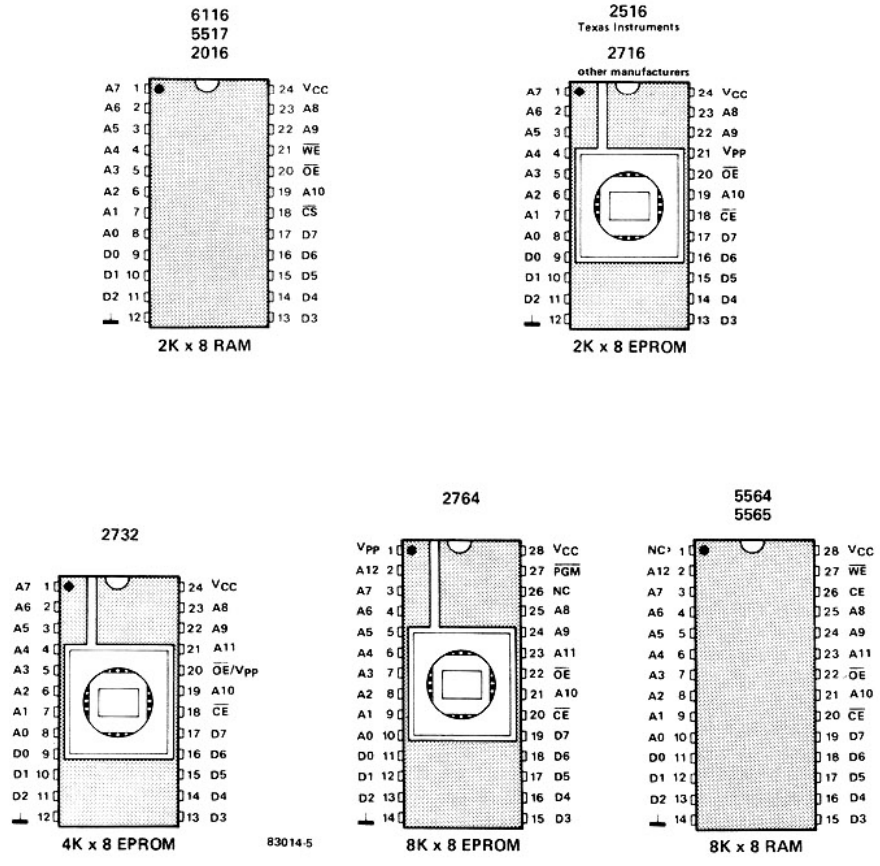
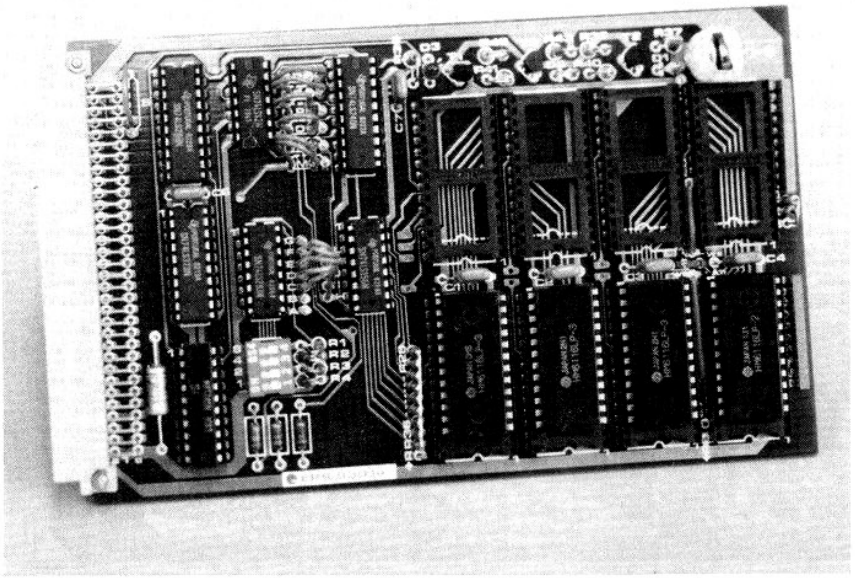


Figure 5. These are the RAM and EPROM types that can be used. The designations stand for memory ICs with the same function, organisation and pin assigments. Other information, particularly concerning equivalent types, can be found on info cards 75 . . . 79. The Texas Instruments EPROMs 2532 and 2564 can only be used in conjunction with an adapter socket. Although the various CMOS RAMs have the same pin assignments, the quiescent current consumption depends on the type.



signal is present.
The memory card can also be used with a ZX 81. A0 ... A14 and D0 ... D7 are connected to the computer in order to create a 16 K memory. The control signals are applied as for the Z80. The address is set to 4000_{hex} with the DIP switches (only close '4'). One more problem must be solved: the internal RAM in the ZX81 operates in parallel with the memory card. The solution is to connect the $\overline{RAMCS}$ output (pin 2A) of the ZX81 to +5 V. Furthermore, the ZX81 does strange things with its A15 output, so this input to the memory card should be connected to supply common instead.
The 2650 processor can also be connected (TV games computer!). 6502 operation is selected: OPREQ/2650 at Φ2/6502; invert $\overline{R}$/W/2650 and apply to R/$\overline{W}$/6502. In the TV games computer, the necessary R/$\overline{W}$ signal is already present at point 17. Also connect the address and data lines. Line M/$\overline{IO}$ remains unused, but this is no real disadvantage, because IO is rarely used. For the odd exception, M/$\overline{IO}$ and OPREQ must be combined externally.
If the card is used in conjunction with the SC/MP system, bus line 27a must not be overlooked; the *input* of the SC/MP oscillator is connected here. With N5 connected, the oscillator may stop. The remedy is to cut this track (it has not been used so far) or to select the other connection point for the oscillator on the SC/MP CPU board.

Power-down and battery backup

The power-down circuit consists of transistors T1 ... T3. It is used in conjunction with CMOS RAMS, and explained earlier. The operating voltage 'R' is present before the enable signal, because T1 is switched on before T2 (power-up). T3 serves as a switch and D3 lights up when the operating voltage is present. The enable signal inhibits reading and writing via N10 and N11.
The battery backup itself can consist of either disposable or rechargeable batteries. If the former are utilised, R37 *must* be omitted. For rechargeable batteries the value of the charging resistor can be calculated according to the rule of thumb: R37 is equal to 2.5 V divided by one twentieth of the battery capacity.

RAMs and EPROMs

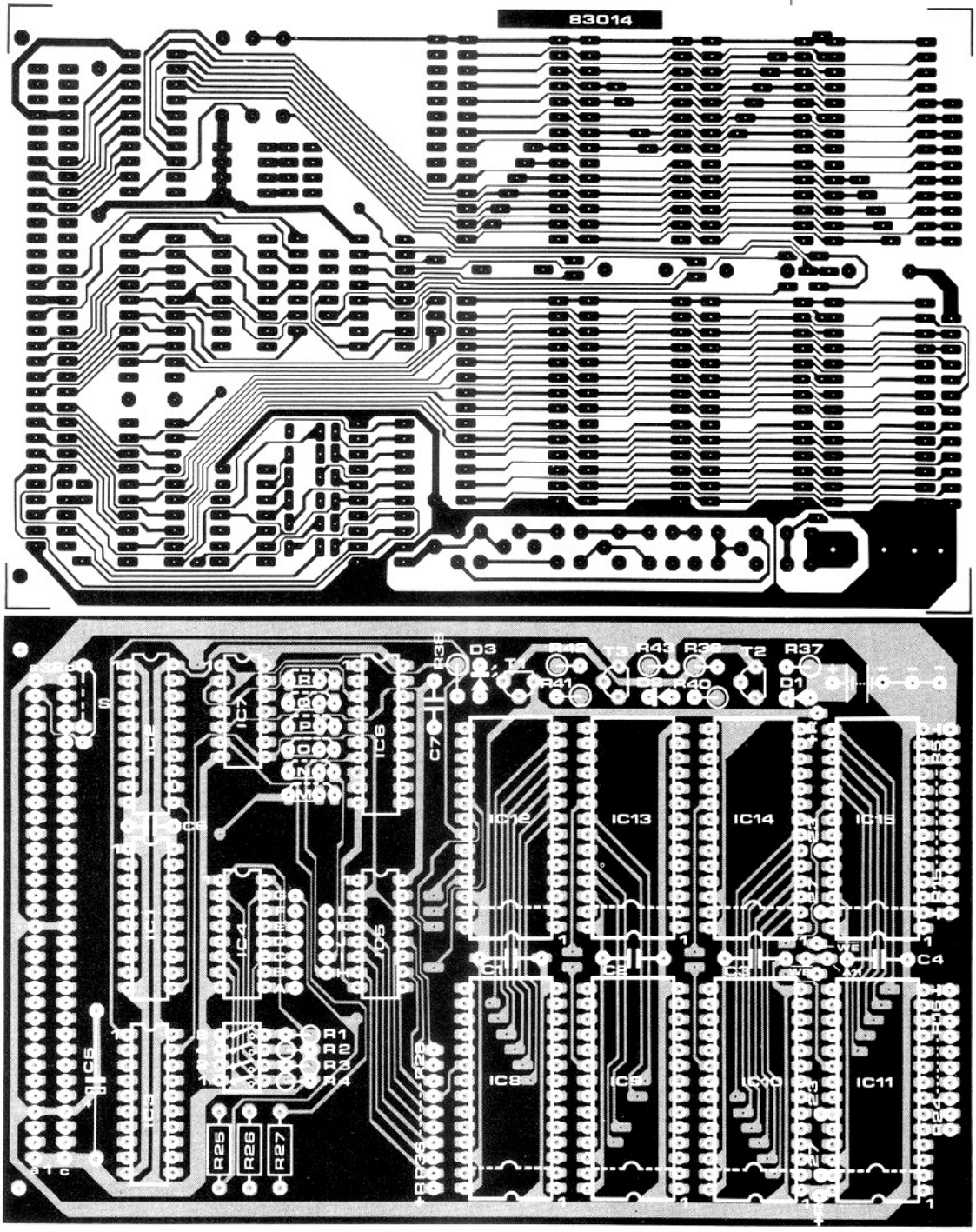
The parts lists for the CMOS or MOS versions of the memory card obviously do not include all possible memory devices, but the types specified are a general designation for ICs with the same function, organisation and, hopefully, the same pinning. The pin assignments for EPROMs and RAMs are given in figure 5. Other information, particularly on equivalent types, can be found on the *info cards* 75 ... 79. One important point to note is that the Texas Instruments EPROMs 2532 and 2564 can only be used if their pin assignments are matched to the equivalent memory ICs by means of an adapter socket.
The RAM and EPROM types to be used are matched to the memory card according to 'size' and function, using the wire links at pins 23 and 27. This match applies to four ICs simultaneously (IC8 ... IC11 and IC12 ... IC15)! A further subdivision is only possible if the corresponding tracks are cut and the pins wired separately.

Timing

Some problems may occur with the timing when connecting the memory card to different processors. The adjacent table shows which RAMs and EPROMs can be

6502				Z80	
1 MHz		2 MHz		2 MHz	4 MHz
EPROM	RAM	EPROM	RAM	EPROM	RAM
450ns	250ns	350ns, or faster	250 ns	450ns	250ns	faster than 350ns	250ns

6



used at different clock frequencies. There shouldn't be any problems unless fast CPUs are used, in which case it may be necessary to use faster EPROMs. The RAMs are fast enough (250ns).

Control signal delays are also important in this context. The $\overline{MREQ}$ signal appears as the $\overline{CE}$ signal at the RAMs or EPROMs after a (typical) delay of 50 ns, caused by N3 (10 ns), N9 (10 ns), IC5 (20 ns) and IC3 (10 ns). The delay for the Φ2 signal is: N5 (10 ns) – N3 (10 ns) – N10 (10 ns) equals 30 ns (typical), after which it appears as $\overline{OE}$ or $\overline{WE}$. In this case the $\overline{CE}$ signal is obtained from the addresses. The delay caused by the data bus buffers is 10 ns (typical). For these purposes we have assumed that the addresses are already present, i.e. that they have already passed the buffer and adder. Otherwise an additional delay of 37 ns (typical) would have to be added for this path.

Construction

Before mounting any components on the p.c. board (figure 6), it is always a wise precaution to check the board for short-

Wire links M – S:
8088
8085 SC/MP 6502 Z80
M --- —— — —
N } see 'address decoding'
O } normally —
P --- --- —— ---
Q —— —— --- ——
R —— —— --- ——
S —— —— --- ——

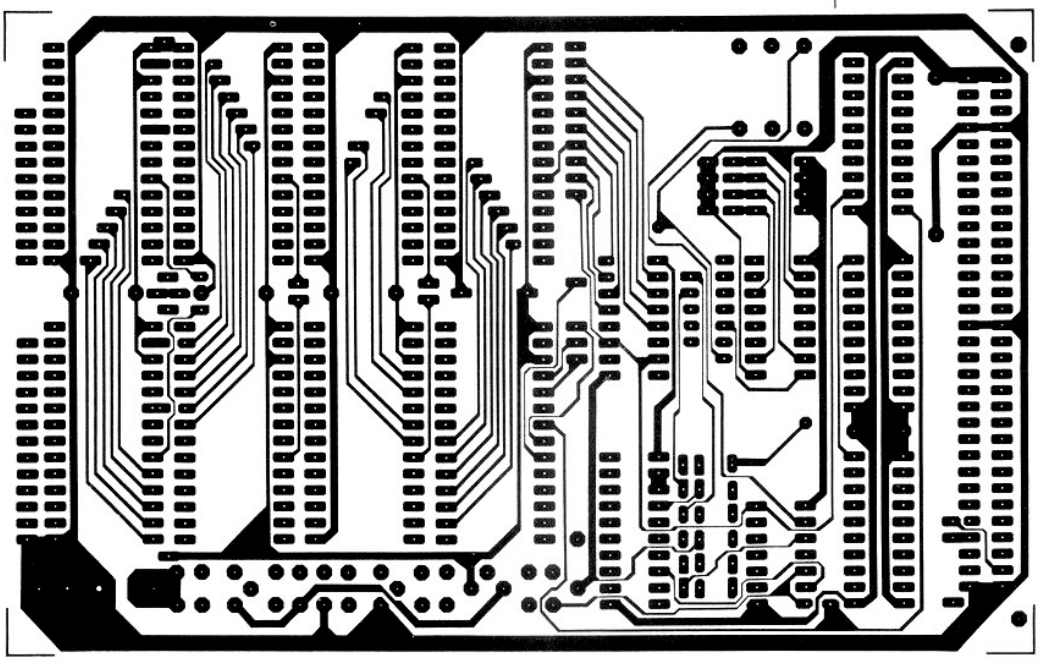


Figure 6. One p.c.b. for both versions (see parts lists). Readers wishing to use a memory card for experimenting with different processors should solder wires to the centre contacts of the 'wire link switches' on the p.c.b. and fit plug-in connectors to the free ends. Matching pins are then inserted into the terminals for the remaining contacts. The memory card then becomes truly universal.

Parts list for MOS version

Resistors:
R1 . . . R4 = 1 k

Capacitors:
C1 . . . C4,C6,C7 = 100 n
C5 = 10 µ/16 V

Semiconductors:
IC1,IC2 = 74LS373
IC3 = 74LS245
IC4 = 74LS283
IC5 = 74LS155*
IC6 = 74LS240
IC7 = 74LS10*
IC8 . . . IC15 = RAM and/or EPROM see text, figures 4 and 5
* different from CMOS version

Miscellaneous:
IC sockets
4-pole DIP switch
64-pin connector

Parts list for CMOS version

Resistors: 1/8 W
R1 . . . R4 = 1 k
R5 . . . R25 = 100 k*
R26 . . . R36 = 1 k*
R37 see text
R38 = 470 Ω
R39 = 2k7
R40,R41 = 10 k
R42 = 220 Ω
R43 = 68 Ω
*Note that 18 of the 100 k resistors can be replaced by two 9x100 k single-in-line resistor networks; similarly, one 9x1 k network can replace nine of the 1 k resistors.

Capacitors:
C1 . . . C4,C6,C7 = 100 n
C5 = 10 µ/16 V

Semiconductors:
D1 = AA119
D2 = 1N4148
D3 = LED red (not high efficiency)
T1,T2 = BC 557B
T3 = BC 547B
IC1,IC2 = 74LS373
IC3 = 74LS245
IC4 = 74LS283
IC5 = 74LS156
IC6 = 74LS240
IC7 = 74LS12
IC8 . . . IC15 = CMOS-RAM 6116, 5564 or similar see text, figures 4 and 5
Miscellaneous:
IC sockets
4-pole DIP switch
64 pin connector
2 . . . 3 NiCd-cells or disposable batteries see text
Nicad: 20 PK
silveroxide: V 76 ris
mercury: V 675 PX

Wire links A . . . L when using:

2 K RAM and EPROM:
G – L
F – K
E – J
D – I
C – H

4 K EPROM:
F – L
E – K
D – J
C – I
B – H

8 K RAM and EPROM:
E – L
D – K
C – J
B – I
A – H

circuits, faulty tracks and continuity of the plated-through holes, using an ohmmeter or continuity tester. In general, however, boards supplied by Elektor should be in order.

The wire links that determine the processor type can now be inserted and the IC sockets soldered in. At this stage it is well worth taking the trouble of checking continuity in the IC sockets. Subsequent fault-finding is extremely tedious . . . The next step is to mount the resistors if it is going to be a CMOS RAM card. If the resistor networks specified in the parts list for the CMOS version are not available, normal resistors can be used instead. They are inserted vertically, and their free ends are interconnected and brought down to the common terminal on the p.c.b. Mounting the remaining components should be no problem. Note that IC5 and IC7 are different for the CMOS and MOS versions!

It is best to use two solderable, miniature nickel cadmium cells as the backup supply for a CMOS RAM. Large batteries will not fit on the p.c.b., but they can always be connected with two wires.

This memory card should provide any personal computer with sufficient memory space. It should be noted that the card is designed for the Elektor bus. If it is to be used with other buses, an adapter must be improvised.