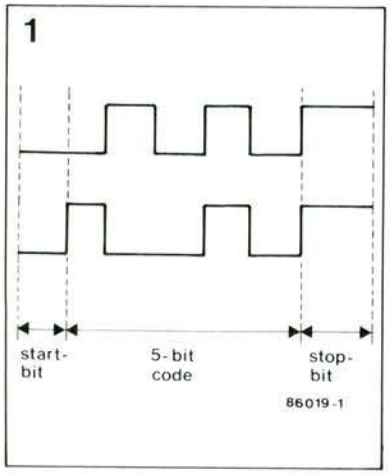
RTTY interface

Some parts of the short-wave radio communications band are swarming with radio teletype (RTTY) signals from all over the world. Although it is an offence under the Wireless Telegraphy Act 1949 to 1967 to intercept many of these transmissions, there are others, such as weather reports, amateur teletype messages, and public newscasts that may be received with impunity. The interface described in this article, in conjunction with a suitable RTTY software package, enables the received teletype message to be displayed on a computer monitor.

Fig. 1. The Baudot code is composed of 5 character bits, preceded and followed by a start and stop bit respectively.



If you use a Junior Computer or DOS Junior, a suitable decoding programme was published in the June 1983 issue (*RTTY Decoder*, p. 30) of *Elektor Electronics*. That same issue contains a useful background to the reception of teletype signals (*Morse and Radio Teletype*, p. 52). EPROMs with RTTY decoding programmes are commercially available for most other types of home computer.

RTTY and FSK

Although morse (CW = continuous wave) and RTTY are often bracketed together, these modes of radio communications differ as to encoding methods and particular use.

With morse, length of the transmitted code depends on the particular character, whereas with RTTY it is always the same, namely seven bits per character using the Baudot convention (see Fig. 1). Many teletype stations still use Baudot coding, but systems based on FEC and ARQ (automatic repeat request) are becoming more numerous as the use of sophisticated computer equipment spreads all over the world.

In conventional radio-based communication, the Baudot pulse train is nearly always transmitted with a modulation system known as frequency shift keying (FSK); the transmitter carrier is switched (shifted) between f_1 (mark = logic 1) and f_2 (space = logic Ø).

Unfortunately, there is no single convention regarding mark and space level assignment, and neither is there one to define baud rate (transmission speed) or shift [$\Delta (f_1 - f_2)$]. Shift, however, is always small relative to the mean carrier frequency; any value between 85 and 700 Hz may be encountered, while 1 kHz seems to have been accepted as the absolute maximum for use on the SW bands.

In the receiver, a beat frequency oscillator (BFO) is used to obtain decoded tones with a frequency difference equal to the shift employed at the transmitter side. The output signal of the receiver is fed to the interface board (described later) for decoding into logic levels corresponding to the transmitted code.

The computer, as the last link in the signal chain, is programmed to form legible text out of the pulse train coming from the interface board. Hard copy of the received message can then be obtained by having the computer mass store texts which may be printed at a later stage.

A versatile RTTY interface

A notorious problem associated with many RTTY interfaces, as well as stand-alone systems, is the difficulty in "getting tuned" to a particular station's shift and baud rate; newcomers to RTTY are frequently baffled by the time it takes to get the unit to recognize valid mark and space signals and it often happens that the transmitting station signs off just when the first legible characters start to appear on screen.

The present design out-performs a number of commercially available RTTY interfaces as well as home made units, in that it alleviates the plight of getting and staying tuned by incorporating a unique FM dis-

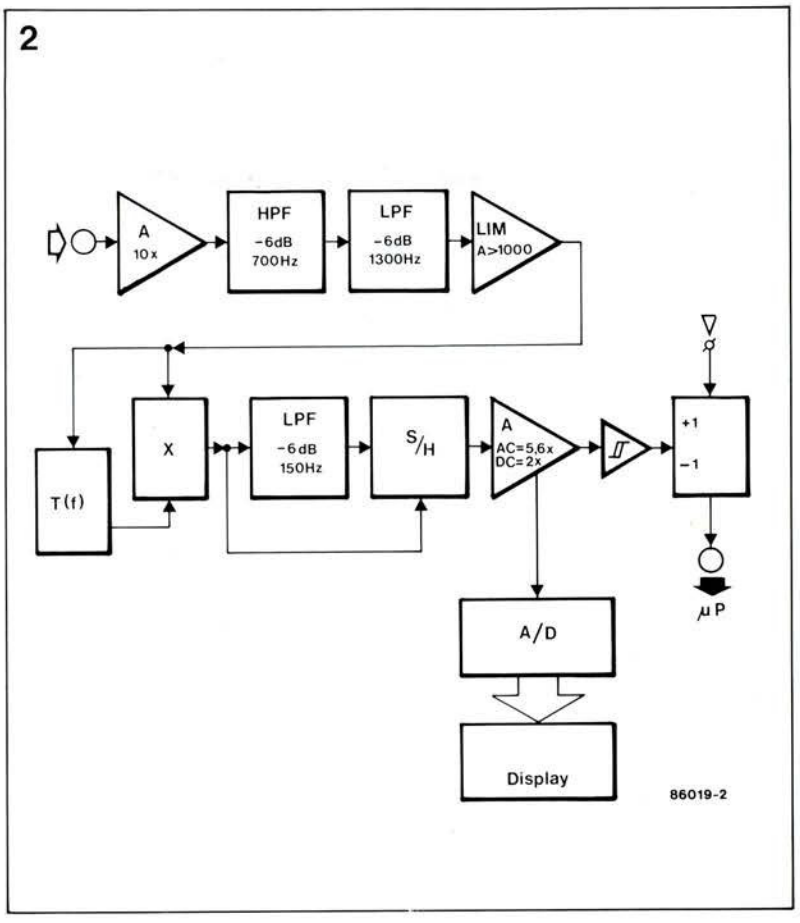


Fig. 2. Block schematic diagram of the RTTY interface. The most essential circuit sections are FM discriminator X and threshold correction stage AAC-ADC.

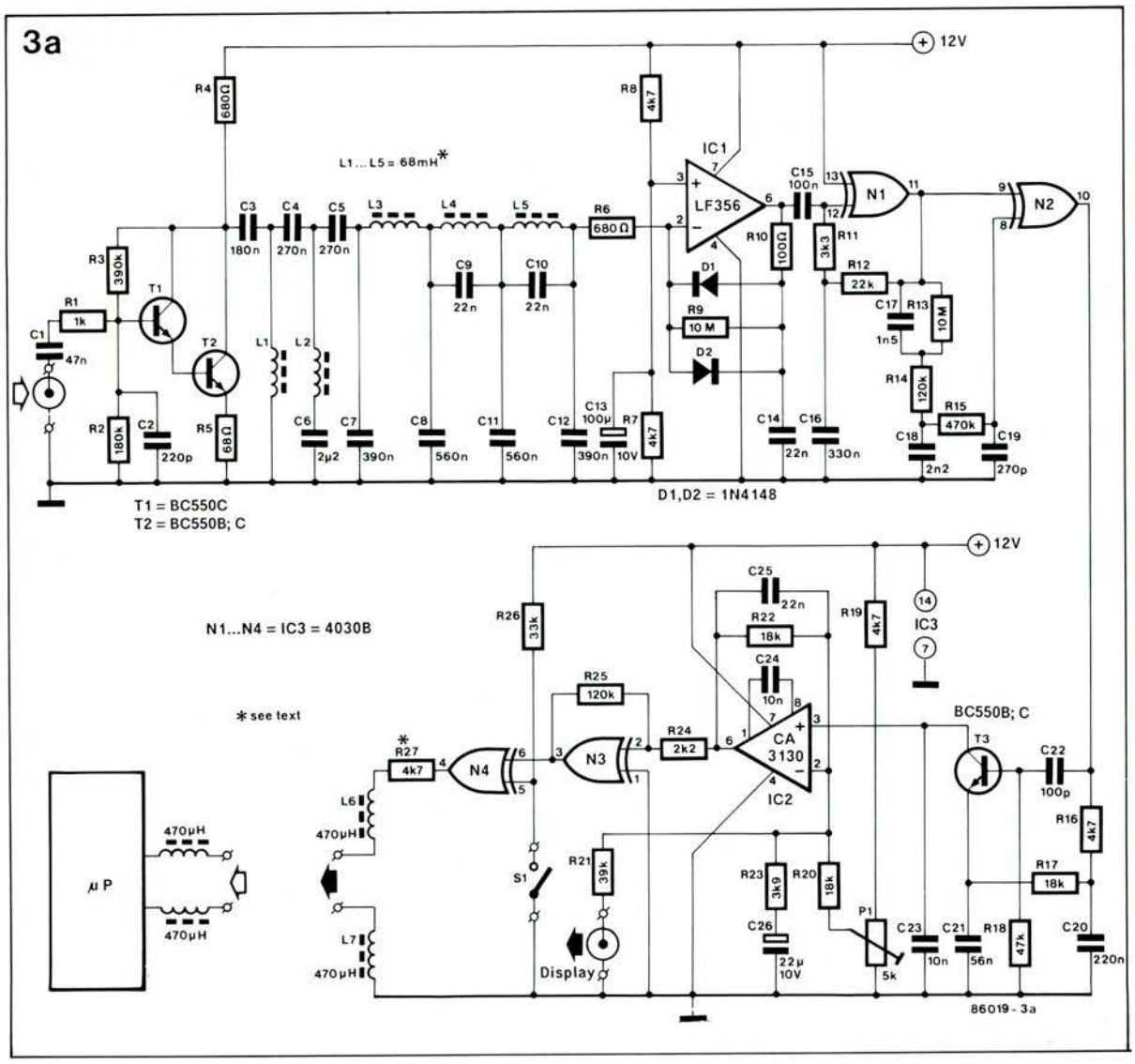
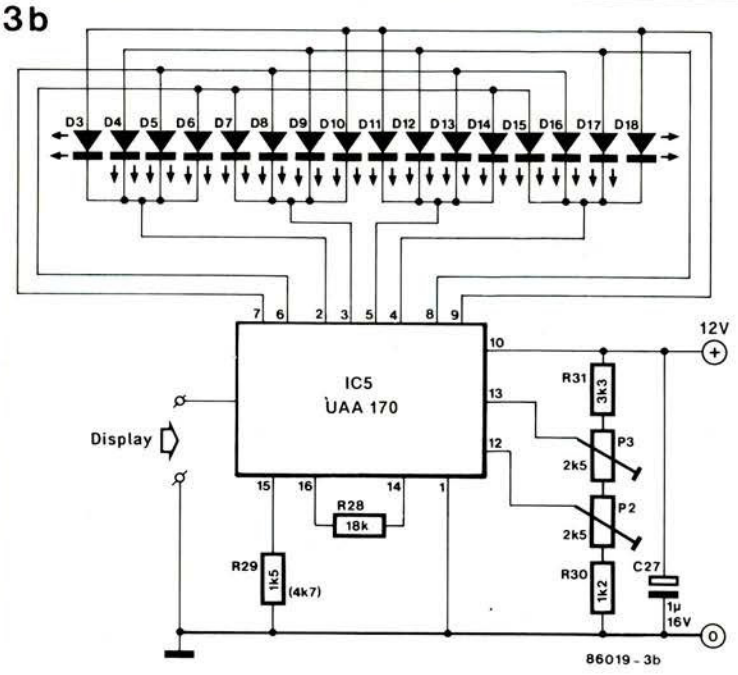
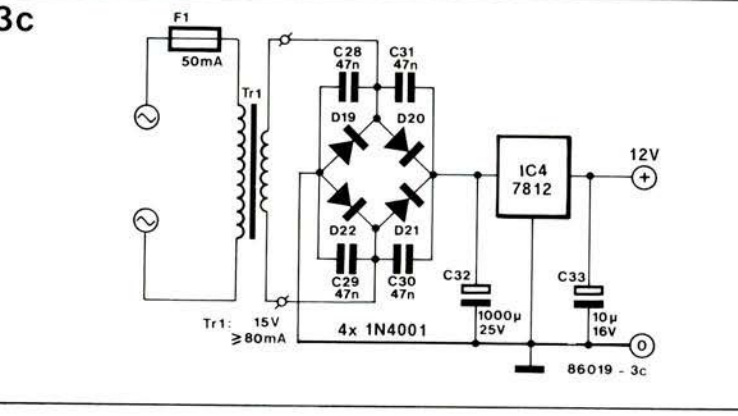


Fig. 3. As compared with the block schematic diagram of the RTTY decoder, the final implementation is not too complex a combination of circuits. Like the associated PCB, the circuit diagram has been split into three parts: decoder/interface (Fig. 3a); LED-bar display (Fig. 3b), and power supply (Fig. 3c).

3b



3c



criminator, that outputs a four-bit code to a LED-bar display which then takes the double function of centre-tuning meter and shift indicator. Furthermore, the proposed interface incorporates an accurately dimensioned bandfilter which enables the use of less stable (not necessarily older!) types of receiver, while operation of the unit is less easily affected by selective fading, thanks to an automatic threshold correction system.

Block diagram

Do not be put off by the apparent complexity of the block diagram shown in Fig. 2, since what looks a tangled network of functional blocks is in fact a straightforward, three-PCB project.

Mark and space signals output by the receiver are amplified (A = 10×) and sent through HPF (high-pass filter) and LPF (low-pass filter) sections with half-voltage (−6 dB) roll-off frequencies of 700 and 1300 Hz respectively. The resulting band-pass filter ensures good mark-space recognition, adequately suppresses interfering signals, and is able to handle shift levels up to 1000 Hz.

The signals are next amplified and limited (LIM: A>1000) before being applied to FM discriminator X. After a frequency-dependent delay T(f), decoded signals are multiplied with their phase-shifted equivalents. The 150 Hz LPF suppresses spurious discriminator output signals and drives sample-and-hold circuit S/H, which "stores" pulses in a capacitor. Tuning information is displayed on an LED-bar, driven by analogue-to-digital converter A/D; the function of the indication has already been discussed in the preceding section.

Amplifier A_{AC}/A_{DC} acts as an automatic threshold correction device in case received signals are less clearly defined owing to selective fading; whenever this occurs, the circuit promptly arranges for decoded signals to remain clear by providing higher AC than DC amplification.

The A/D converter, display, and output signal inverter (+1 −1) will be discussed in more detail in the following section.

Circuit description

The circuit diagram of the RTTY interface is shown in Fig. 3a. Proceding from input to output once more, it is seen that the input amplifier is composed of T_1 and T_2, and drives the 700 to 1300 Hz bandfilter. This is formed by capacitors $C_3 \ldots C_{12}$ and inductors $L_1 \ldots L_5$; skirt steepness of the filter as shown is more than 40 dB per octave.

The amplifier/limiter is based upon the use of fast opamp IC_1, diodes D_1-D_2 and gate N_1. XOR gate N_2 functions as FM discriminator, together with delay network $C_{17} \ldots C_{19}$ and $R_{13} \ldots R_{15}$. This simple, yet effective circuit arranges for changes in input frequency (mark/space) to be converted into a corresponding change in mark-space ratio of the rectangular output signal from N_2, which in turn drives sample & hold (S/H) transistor T_3 via LPF R_{16}-C_{20}.

Operation of the sample & hold circuit is based upon the use of capacitor C_{21}, which is charged by R_{17}; as soon as T_3 conducts, the pulse level is stored in C_{23}, which can keep its charge for a relatively long time as it is only very lightly loaded by the high resistance of the +input of IC_2. The display output may conveniently be taken from the −input of this opamp since the signal at that terminal is basically identical to the sample & hold output, which should be left as lightly loaded as possible.

In addition to buffering the S & H signal, IC_2 functions as the automatic threshold correction device, by offering AC and DC amplification factors of 5.6 times (R_{22}-R_{23}) and 2 times R_{22}-R_{20}) respectively.

Finally, the RTTY pulse train (12 V logic swing) can be taken from N_4, either in true or in inverted logic as selected with S_1 and depending on the computer type to be used with the interface. Digital noise suppression parts L_6-L_7-R_{27} have been included to prevent signal breakthrough and erroneous decoding owing to computer-generated pulses. Note that R_{27} may have to be adapted or even short-circuited in some applications.

The single-chip display driver circuit (Fig. 3b) as well as the power supply (Fig. 3c) to the interface are of conventional design which requires no further discussion.

Construction

To begin with, the ready-made PCB for the RTTY interface (see READERS SERVICES, elsewhere in this issue) may be cut in three parts: for the interface proper, power

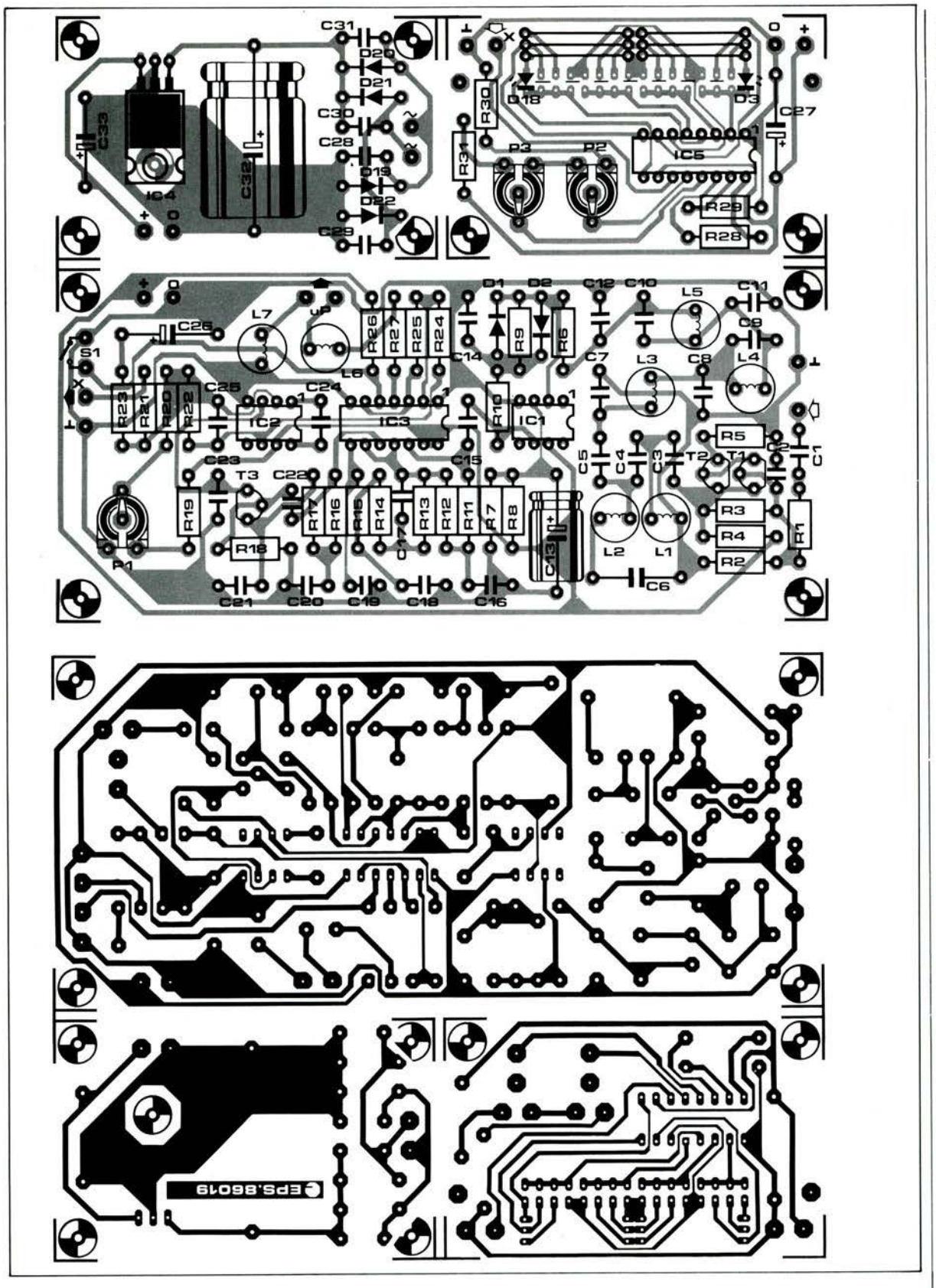


Fig. 4. Track pattern and component layout of the PCB for the RTTY interface. Note that the circuit board may be cut into three sections, depending on the type of enclosure selected for the project.

Parts list

Resistors:

$R_1 = 1$ k
$R_2 = 180$ k
$R_3 = 390$ k
$R_4; R_6 = 680\ \Omega$
$R_5 = 68\ \Omega$
$R_7; R_8; R_{16}; R_{19}; R_{27} = 4k7$
$R_9; R_{13} = 10$ M
$R_{10} = 100\ \Omega$
$R_{11}; R_{31} = 3k3$
$R_{12} = 22$ k
$R_{14}; R_{25} = 120$ k
$R_{15} = 470$ k
$R_{17}; R_{20}; R_{22}; R_{28} = 18$ k
$R_{18} = 47$ k
$R_{21} = 39$ k
$R_{23} = 3k9$
$R_{24} = 2k2$
$R_{26} = 33$ k
$R_{29} = 1k5$
$R_{30} = 1k2$
$P_1 = 5$ k preset
$P_2; P_3 = 2k5$ preset

Capacitors:

$C_1; C_{28} \ldots C_{31}$ incl. = 47 n
$C_2 = 220$ p
$C_3 = 180$ n
$C_4; C_5 = 270$ n
$C_6 = 2\mu2$; MKT
$C_7; C_{12} = 390$ n
$C_8; C_{11} = 560$ n
$C_9; C_{10}; C_{14}; C_{25} = 22$ n
$C_{13} = 100\ \mu$; 10 V
$C_{15} = 100$ n
$C_{16} = 330$ n
$C_{17} = 1n5$
$C_{18} = 2n2$
$C_{19} = 270$ p
$C_{20} = 220$ n
$C_{21} = 56$ n
$C_{22} = 100$ p
$C23; C_{24} = 10$ n
$C_{26} = 22\ \mu$; 10 V
$C_{27} = 1\ \mu$; 16 V; electrolytic
$C_{32} = 1000\ \mu$; 25 V
$C_{33} = 10\ \mu$; 16 V

Semiconductors:

$D_1; D_2 = 1N4148$
$D_3 \ldots D_{18}$ incl. = red panel-mount LED
$D_{19} \ldots D_{22}$ incl. = 1N4001
$T_1; T_2 = BC550B$
$IC_1 = LF356$
$IC_2 = CA3130$
$IC_3 = 4030B$
$IC_4 = 7812$
$IC_5 = UAA170$

Inductors:

$L_1 \ldots L_5$ incl. = 68 mH choke; Toko Type 181LY-683*
$L_6; L_7 = 470\ \mu$H choke; Toko Type 187LY-471*

Miscellaneous:

$Tr_1 = 15$ V; 150 mA
$S_1 =$ SPST switch
$F_1 = 50$ mA fast
Suitable metal enclosure
Suitable display bezel
PCB Type 86019 (see Readers Services)
Soldering pins as required

* Available from Cirkit Holdings plc; Telephone (0992) 444111.

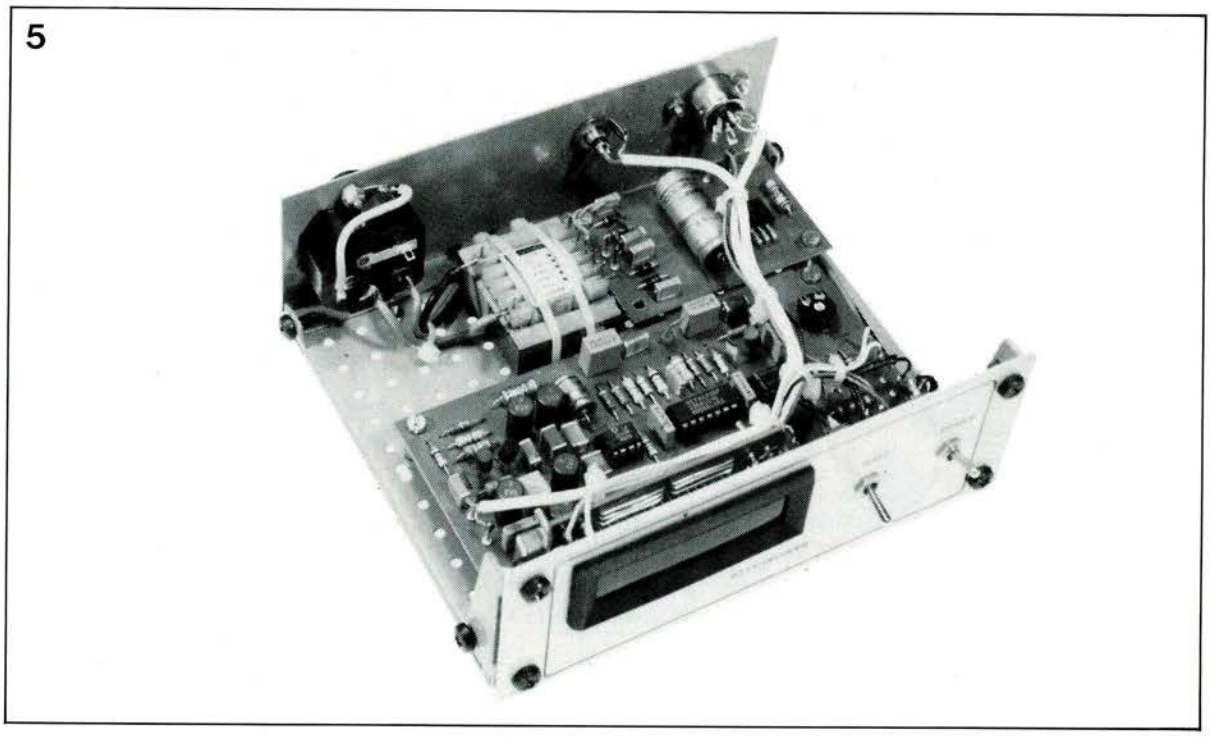


Fig. 5. Showing the completed RTTY interface mounted in a metal cabinet. Output polarity swich S_1 has been fitted right next to the bargraph tuning indicator.

supply, and display driver plus LED bar. The division into functional sections enables the unit to be neatly fitted into a **metal** enclosure with a clearance in its front panel to allow the LED-bar to protrude slightly.

Fitting the parts as shown in Fig. 4 is not expected to present serious difficulty, provided the job is done with some accuracy.

As to components for the project, these should be generally available from most retailers: $L_1 \ldots L_6$ inclusive should be good quality chokes with a series resistance of no more than about 50 Ω; in case of doubt about the specification in this respect, check the types you intend to use with an ohmmeter, or have the supplier do this in your presence. The circuit as shown will definitely not work properly if equipped with chokes with a series resistance of more than 300 Ω. As shown in Fig. 4, regulator IC_4 can do without a heat-sink.

Wiring the completed boards is straightforward, but do not forget the supply interconnections. Receiver, interface, and computer are best connected by short lengths of thin screened wire as used in audio applications. Where this is thought useful, plugs may be fitted to make for neat connections to existing equipment.

Setting up

Using an oscilloscope and an AF function generator, align the completed interface as follows:

1. Connect the generator to the interface input and the scope to junction L_5-R_6.
2. Tune the generator across the 0 to 2000 Hz frequency range to find the filter's —6 dB (half voltage) roll-off points; calculate its centre frequency, $f_c = \frac{1}{2}(f_L + f_H)$.
3. Set the generator to produce f_c and connect the scope to the interface output. Turn P_1 to find two points at which the output voltage is observed to toggle, and set the wiper of P_1 to a position exactly in between these points. This concludes the setting up procedure.

Those constructors who do not have an oscilloscope to hand may start aligning from step 3 onwards, assuming that the filter centre frequency is 1000 Hz. Use a voltmeter or a single-transistor LED interface to check if the output voltage toggles as indicated.

Presets P_2 and P_3 on the display board should be set to have the centre LEDs, D_{10} and D_{11}, light when 1000 Hz is applied to the interface. The full-scale readout of the LED-bar then corresponds to a shift of 850 to 1000 Hz, or about 50 Hz per LED. When a station whose shift is accurately known is received, P_2 and P_3 may be fine tuned to have the readout register the relevant value. It is also useful to know that many teletype stations in the 20-metre band utilize 170 Hz shift and can therefore be used as a reference in setting P_2 and P_3.

Use in practice

It is expected that the incorporation of the LED-based tuning system enables users to get stable reception of teletype messages fairly quickly. The maximum baud rate the interface can handle is about 100 baud, although 200 baud has been achieved when receiving a strong and interference-free signal, which, unfortunately, is something of a rarity on the SW bands nowadays.

There is one last, important, point to make about connecting the interface to the computer input: remember that the interface output swing is approximately 12 V_{pp}; this may require a level shifter to be used to step down to 5 V_{pp} for the computer input, which should be fitted with a pair of small chokes as shown in Fig. 3a.

(B)

Table 1.

Specifications:

- Decoded shift range: 30..1000 Hz.
- Input voltage: 300 μV_{rms}...300 mV_{rms}.
- Input impedance: 47 kΩ.
- Baud rate: up to 100.
- Current consumption: approx. 80 mA.
- Simple, three-preset alignment.
- LED-bar indicates shift and centre tuning.