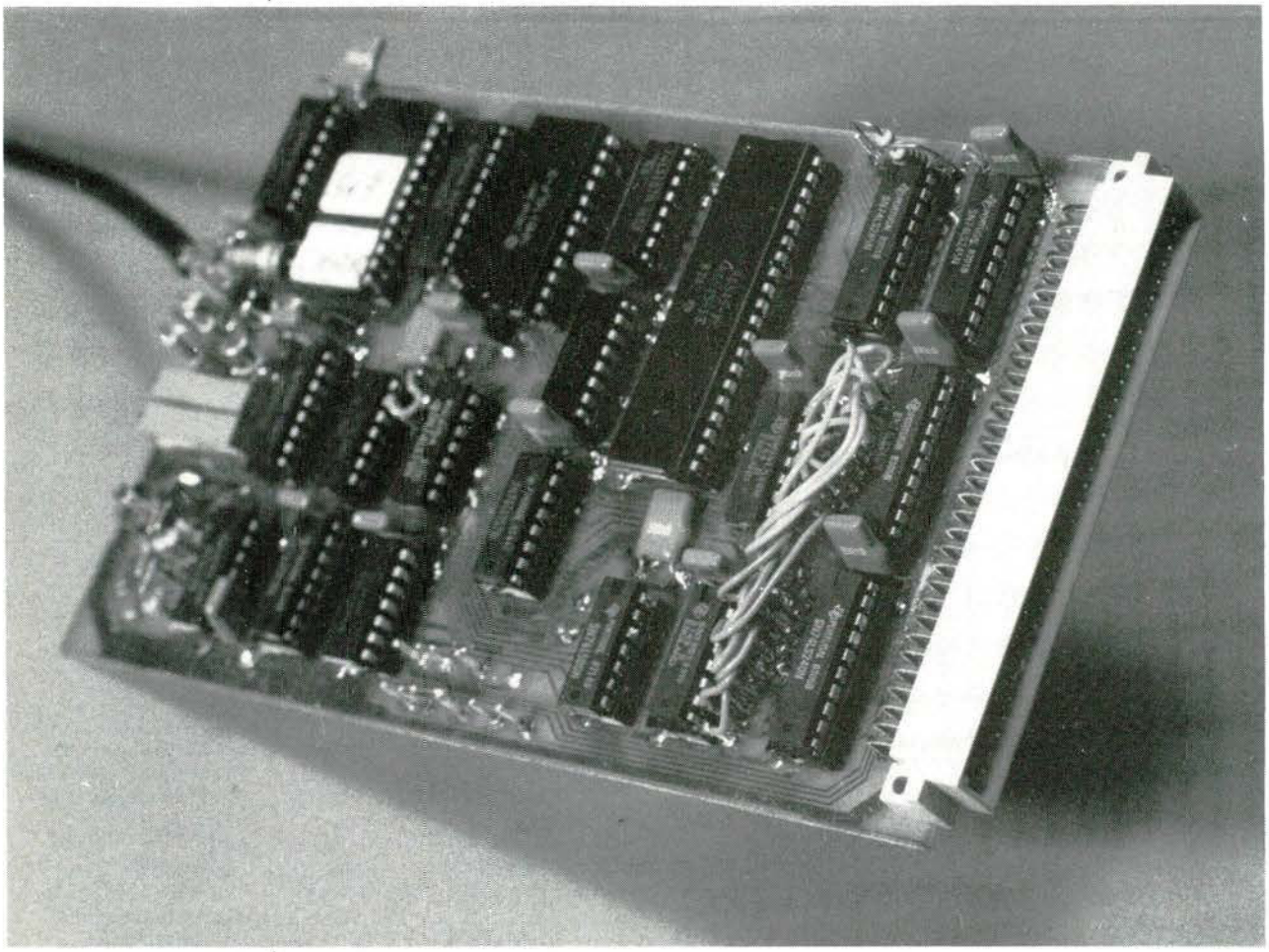
VDU card



In Elektor we like to keep up to date, and we feel that the time has come for a new video card. The VDU card described here is not simply a modern receiver for the old and still popular Elekterminal, rather it is a new design intended to use all the possibilities of a modern computer. It can display 24 lines of 80 characters on the screen, graphics are available, and there are several other possibilities. Numerous Junior Computer users have long been waiting to be able to equip their computer system with its own video card. However, this card is intended not only for the Junior but also for other processors, such as the 6800 family and the Z80.

video for computers

in conjunction with
H. Vermeulen

The accompanying article in this issue 'Video graphics' describes the principles of a VDU card and is good background material for anybody who is not totally familiar with the subject, so, rather than duplicate any of that here, we will simply describe the circuit for the VDU card. At the same time, we must explain what the further possibilities of this card are and this is where we will begin.

VDU card . . . and terminal?

Here we will consider the VDU card as an independent unit. In this form it can be connected directly to the expansion bus of the Junior Computer. The only extra component needed is a 2716 EPROM with a VDU output program in place of the printer monitor program.

Figure 1 shows the main components which make up the VDU. First is the actual VDU card, with the Cathode Ray Tube Controller (6845), a 2K video RAM (6116), and the character generator – the block diagram is shown in the descriptive article. The character generator consists of a 2732 EPROM in which all the ASCII and graphics symbols are stored in the appropriate dot-matrix

layout (incidentally, graphics are possible by means of 'poke' commands, but we will return to that later). The card can be connected via a 75 Ω video output to a monitor. A connection for a light pen is also included on the card but no software for this purpose has been given in this basic version. It will be a simple matter to incorporate this at a later date. The diagram also shows the 2716 which contains the video routines for the Junior.

The standard format on the screen is 24 lines of 80 characters and because of the bandwidth required, a proper monitor or a TV set with a video input (not the normal aerial input) is needed.

The card also has an interface to adapt the VDU board for a Z80 processor. Similarly, other 6502 computers can be connected to it, as can the 6800 family. Because complete address decoding is possible on the card it can be adapted to practically every modern computer with one of the processors mentioned; AIM 65, SYM, VIC 20, VIC 64 and so on. One thing to remember is that the VDU card uses the Elektor bus and if it is to be used with other systems, the user will have to work out the connections and video routines himself.

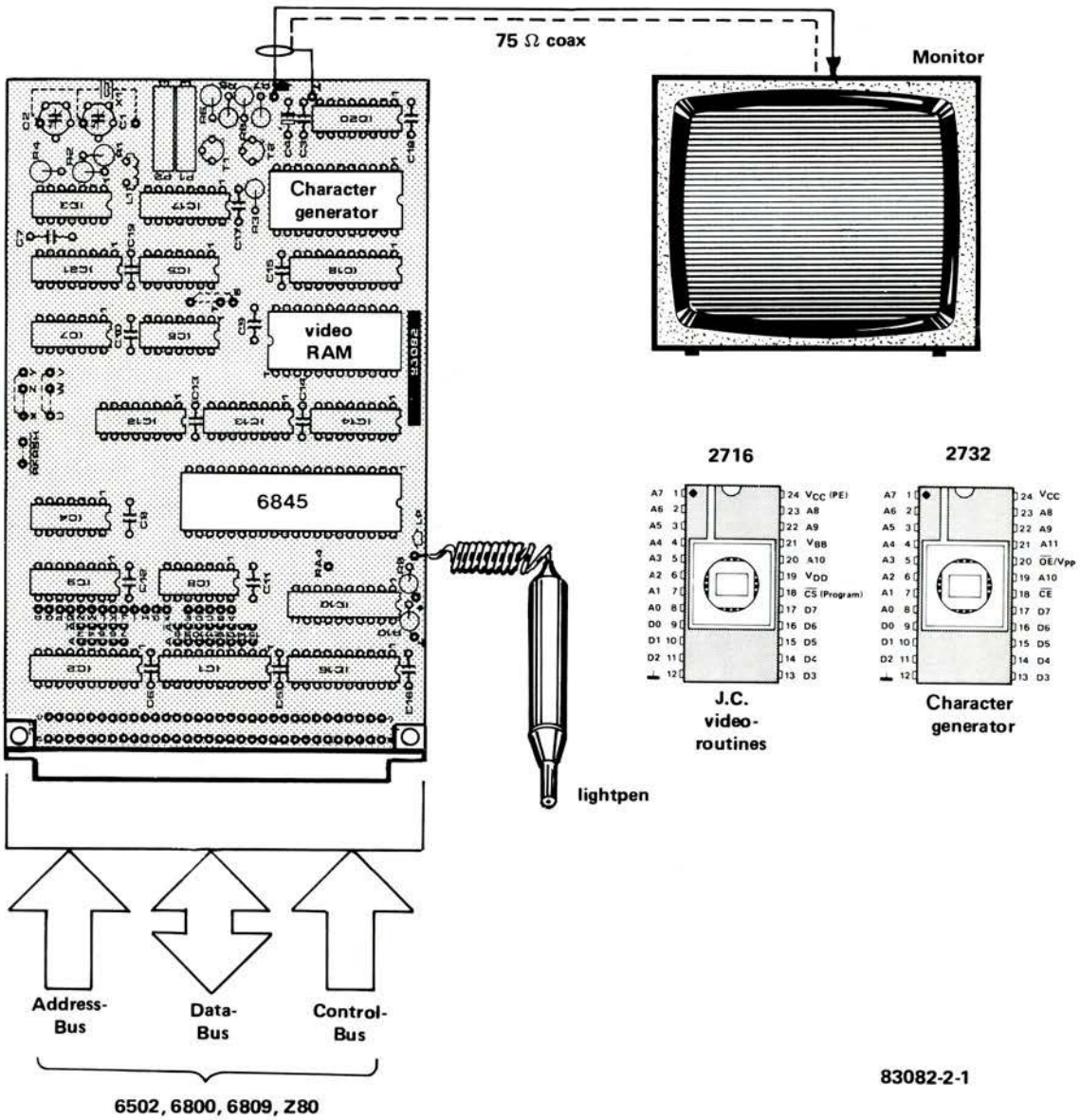
The composite video signal produced by the VDU card can be fed into any monitor. Both the synchronization pulses and the contrast can be adjusted. The whole image can also be inverted to provide black characters on a light background. The cursor can be made to flash or light continuously. The VDU card can be used with the oscillator containing C1, C2 and L1, or these components can be replaced by a 15 MHz crystal, as shown dotted in the circuit diagram. If this is done the image on the screen will be rock steady.

The card is slightly unusual in that all the timing on the card works with synchronously clocked TTL switching. The advantage of this is that no timing faults can occur, even with this high frequency.

As you can see there are already quite a few

Figure 1. This is a sketch of the major components of the VDU card.

1



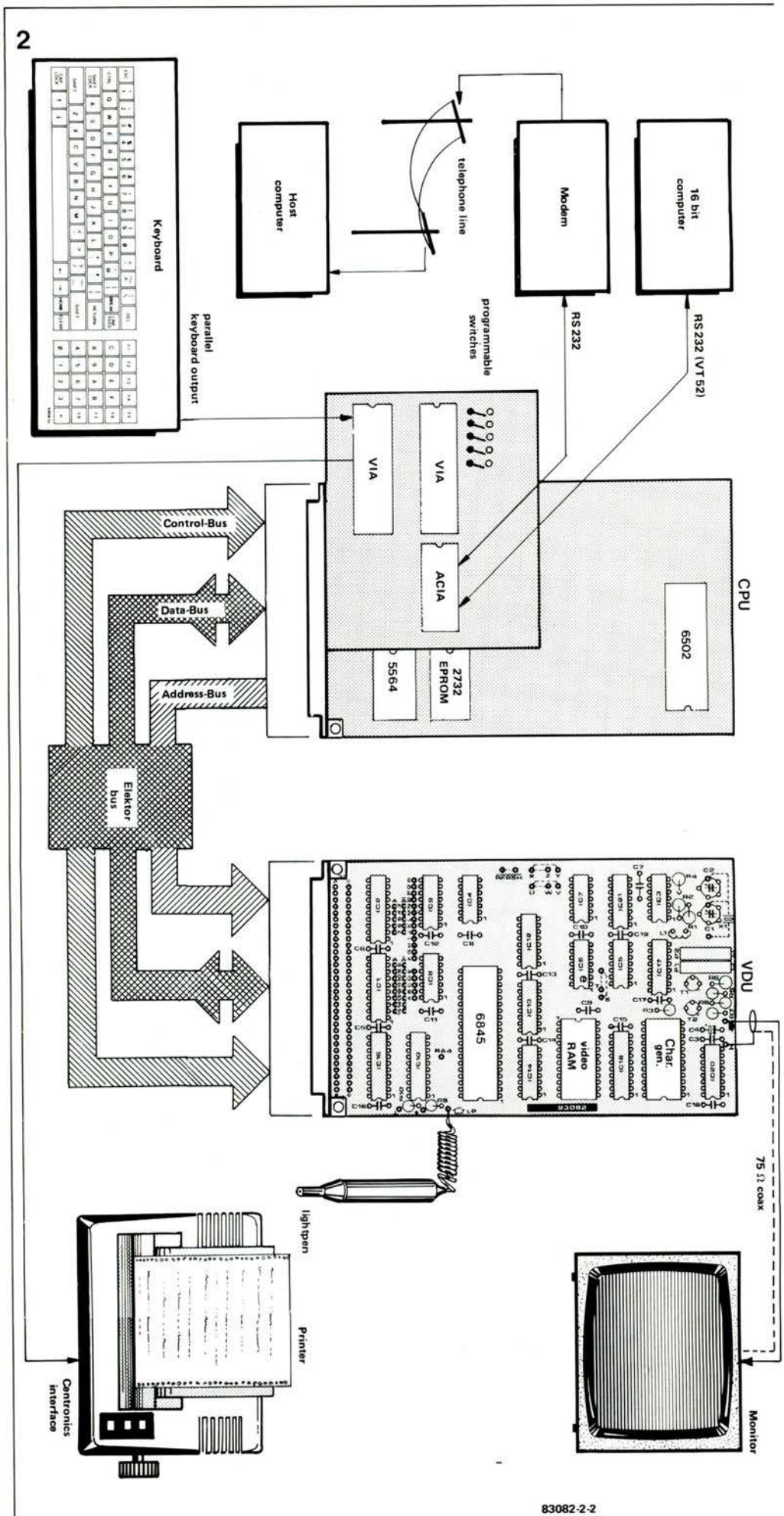


Figure 2. This shows what can ultimately be achieved with the universal terminal containing a VDU card and a CPU card. All the other equipment (computer, modem, printer, keyboard and so on) can be connected to this terminal.

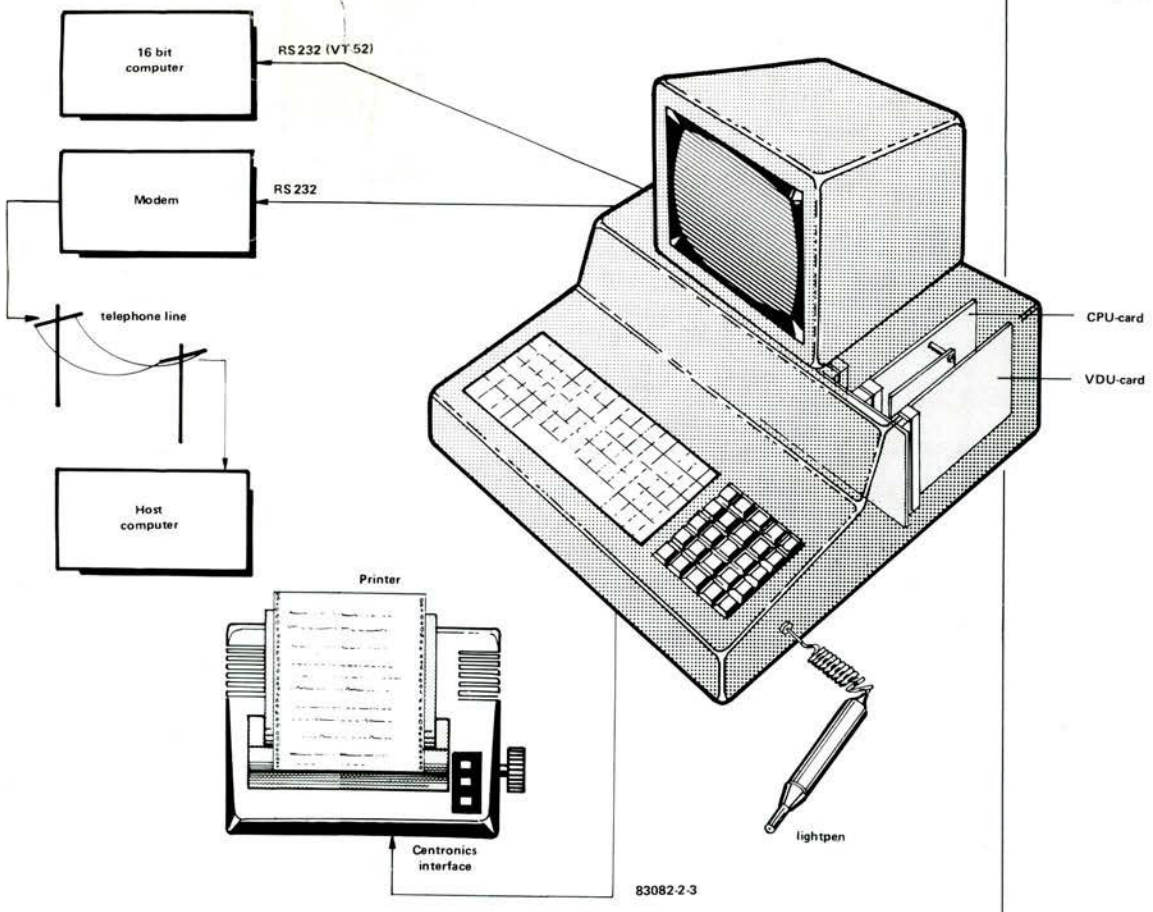
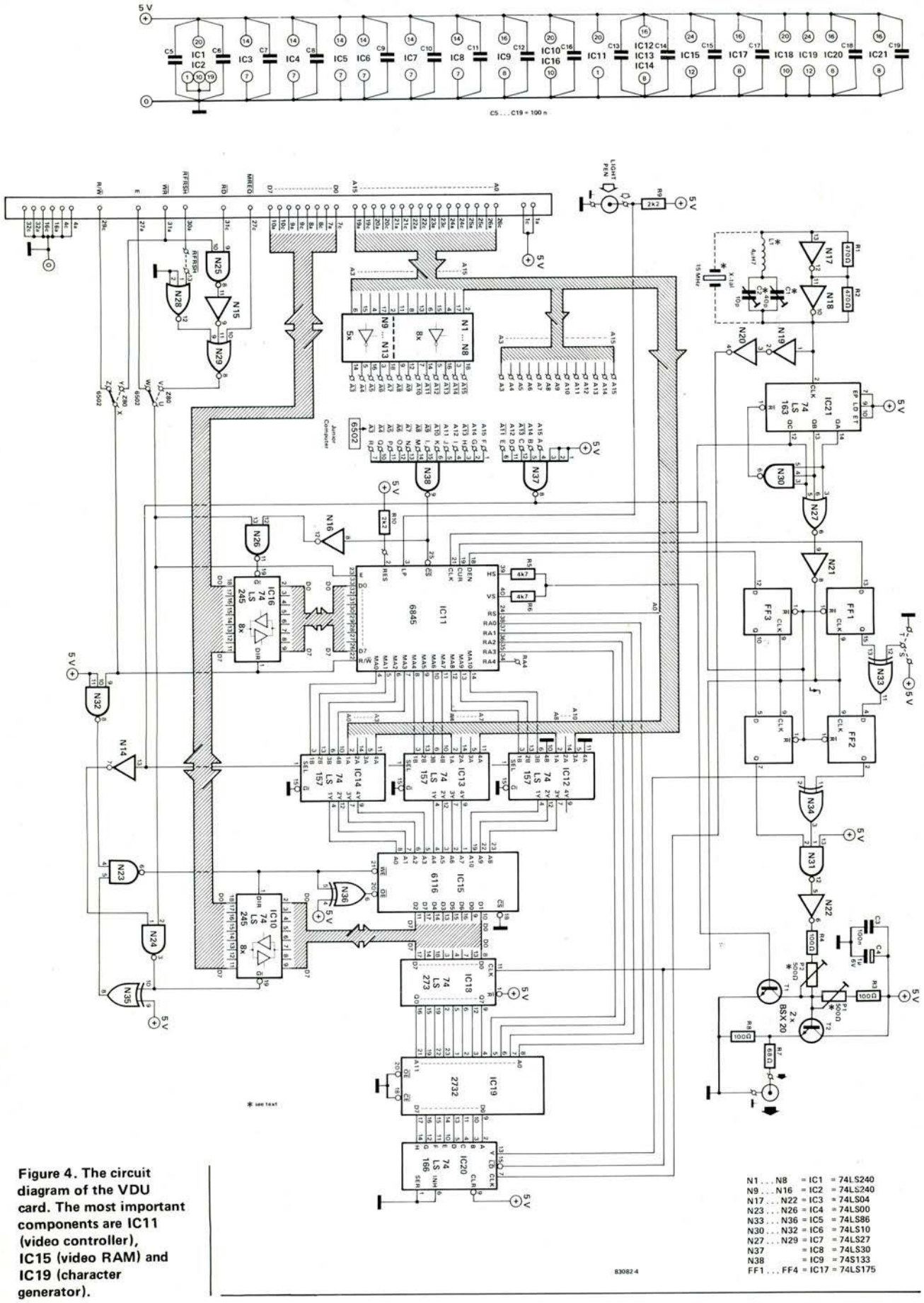


Figure 3. The combination of VDU and CPU cards can also be used as the basis of a complete computer system. The combination controls communication between the various parts of the system and displays information on the screen.

possibilities with the VDU card but there are even more to come. As a follow up to this VDU card we will shortly publish a CPU card especially developed to complement it. These two cards will together form the basis of a universal terminal with RS 232 interface and VT 52 protocol, so that it can be connected to virtually any computer. Figure 2 shows the main parts of this system and of course this terminal can be connected to any computer which has an RS 232 interface.
The CPU card contains a 6502 microprocessor, 2 VIAs (Versatile Interface Adapter), an ACIA (Asynchronous Communications Interface Adapter) an EPROM and a RAM. Thanks to a set of through connections on the board the transfer format, speed, number of start and stop bits and the type and number of control bits can be adapted to whatever computer is connected to the terminal. Similarly there is a choice of eight different screen-image formats.
All that is needed to make up a complete terminal is a VDU card, a CPU card, a monitor and a keyboard. The terminal could, for example, communicate over the telephone lines via a modem, with a computer in some other part of the globe, but because of its VT 52 protocol it could also be connected directly to a 16 bit computer. A connection for a printer is, of course, provided. It is also possible to use the CPU card and VDU card together as the basis for a complete computer system, as figure 3 shows. This example is connected to a 16 bitter but, in principle, that could be any type of computer.
The terminal software is located in a 2716 EPROM on the CPU card which can have a maximum of 8 K of random access memory and 16 K of read only memory.
Clearly there are already quite a few possibilities for this two-card combination and certainly there are more than we have mentioned. However we will leave it at that until the article on the CPU card.

The VDU card in a nutshell

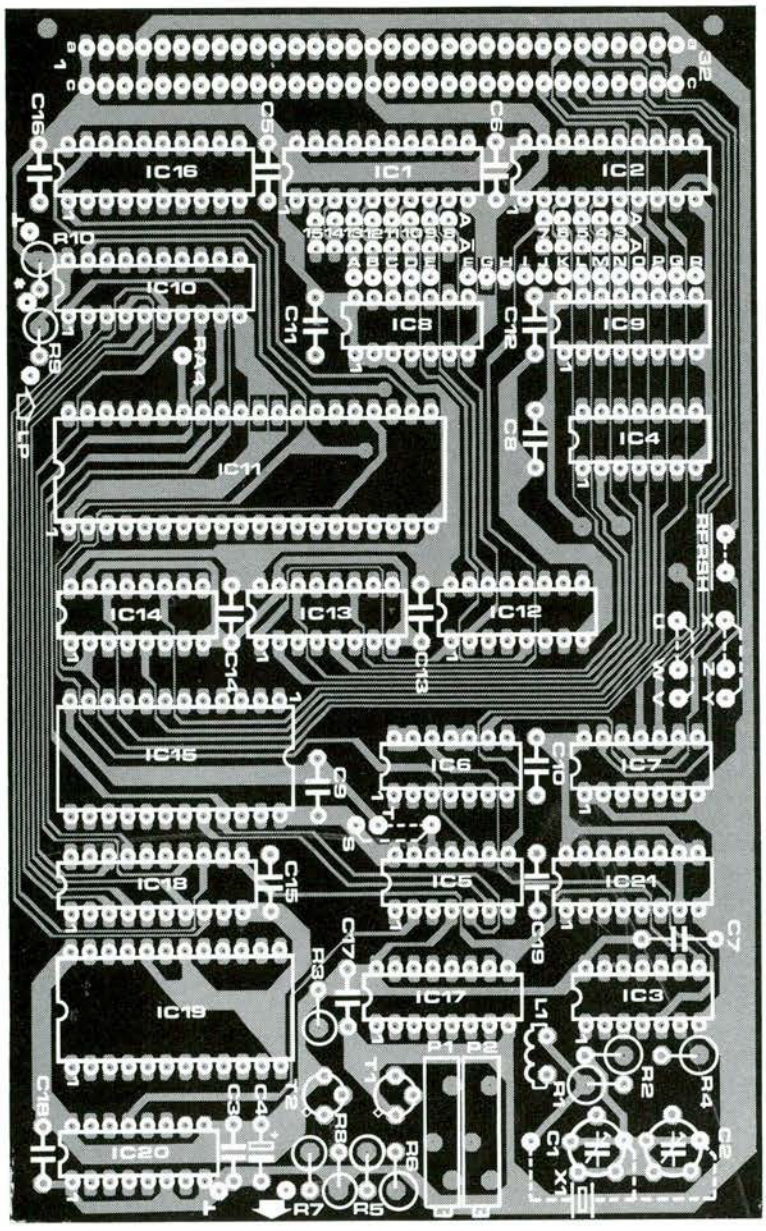
Figure 4 shows the circuit diagram for the VDU card. At the left is the system bus and here we see that address lines A0 . . . A10 are connected to the B inputs of the 2 into 1 multiplexers, IC12 . . . IC14. Also address lines A3 . . . A15 are inverted by N1 . . . N13. Complete address decoding is thus possible because the addresses are available either normally at points A3 . . . A15 or inverted at points $\overline{A3}$ . . . $\overline{A15}$. Address decoding for the video RAM is carried out via N37, and for the CRTC via N38. The numbers beside these two gates refer to those used with the Junior Computer. In this case the video RAM is in the range D000 . . . D7FF and the CRTC is between D800 and D80F.
When N37 gives a chip-select signal the video RAM (IC15) is addressed from the system bus by the microprocessor. By this the address inputs of the 6116 are connected to the address bus of the system via the A inputs of the multiplexers IC12 . . . IC14



N1 . . . N8 = IC1 = 74LS240
N9 . . . N16 = IC2 = 74LS240
N17 . . . N22 = IC3 = 74LS04
N23 . . . N26 = IC4 = 74LS00
N33 . . . N36 = IC5 = 74LS86
N30 . . . N32 = IC6 = 74LS10
N27 . . . N29 = IC7 = 74LS27
N37 = IC8 = 74LS30
N38 = IC9 = 74S133
FF1 . . . FF4 = IC17 = 74LS175

830824

Figure 4. The circuit diagram of the VDU card. The most important components are IC11 (video controller), IC15 (video RAM) and IC19 (character generator).



Parts list

Resistors:
R1,R2 = 470 Ω
R3,R4,R8 = 100 Ω
R5,R6 = 4k7
R7 = 68 Ω
R9,R10 = 2k2

Capacitors:
C1 = 40 p trimmer
C2 = 10 p trimmer
C3,C5 . . . C19 = 100 n
C4 = 1 μ/6 V

Semiconductors:
T1,T2 = BSX 20
IC1,IC2 = 74LS240
IC3 = 74LS04
IC4 = 74LS00
IC5 = 74LS86
IC6 = 74LS10
IC7 = 74LS27
IC8 = 74LS30
IC9 = 74S133
IC10,IC16 = 74LS245
IC11 = 6845
IC12,IC13,
IC14 = 74LS157
IC15 = 6116
IC17 = 74LS175
IC18 = 74LS273
IC19 = 2732
IC20 = 74LS166
IC21 = 74LS163

Miscellaneous:
X1 = 15 MHz crystal (for a display configuration of 80 x 24 characters; if this crystal is used C1, C2 and L1 are not needed).
L1 = 4.7 μH
64 pin male connector DIN, use the A and C rows

Figure 5. The component layout for the VDU card.

(select inputs of the multiplexers are logic zero). At the same time data bus buffer IC10 is enabled via N14 and N24. The logic level of the R/$\overline{W}$ line (pin 29c of the connector) ensures that IC15 is enabled via N32, N23 and the $\overline{WE}$ input.
If the CRTC is addressed from the system bus N38 gives a logic zero to the $\overline{CS}$ input. The processor then has access to the internal registers of the 6845 via the system bus. Data bus buffer IC16 is then also enabled via N16 and N26.
IC16 is really only needed of a light pen is to be used with the VDU card. If this is not the case, and data is only written from the bus to the CRTC, then IC16 is superfluous and the 6845 can be connected directly to the data lines with eight wire links.
Address decoder N37 resets flip-flops FF1 . . . FF4 so that no rubbish appears on the screen when the processor accesses the video RAM.

The timing of the VDU card is controlled by the oscillator based on N17 and N18. This supplies the so-called dot frequency, which is 15 MHz for the screen format used here. A coil is necessary to maintain stability of the oscillator at this relatively high frequency. For optimum performance, a 15 MHz crystal could be used in the oscillator in place of C1, C2 and L1. IC21 divides the oscillator signal by eight. This IC is a synchronous counter which is reset via N30 when the count reaches seven. Because the reset is only processed by the IC on the following clock pulse, the IC then effectively counts to eight. Output QC delivers the character frequency for the controller. The CRTC counts continuously from 000 to 7FF (the whole range of the video RAM) at the frequency of this signal. As the processor now has no access to the video RAM, the address outputs MA0 . . . MA10 of IC12 are connected to the address inputs of the 6116

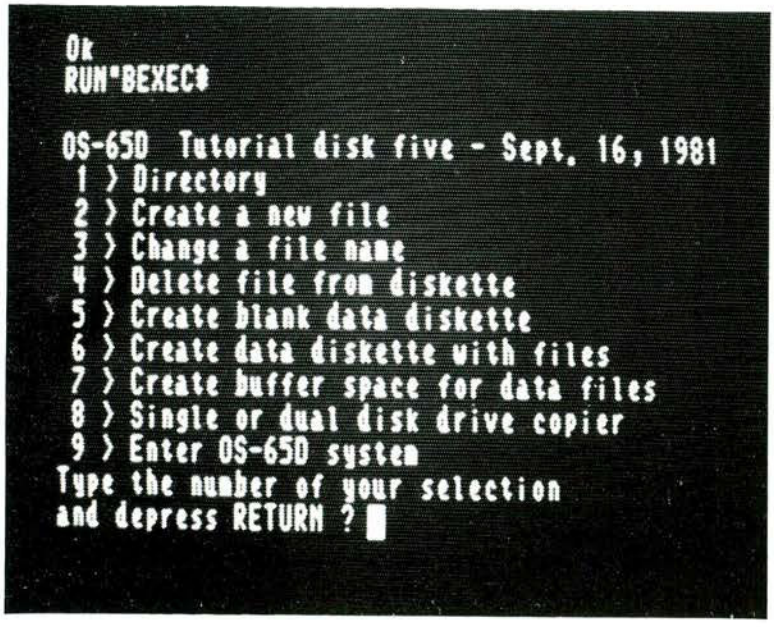
via the multiplexers, so that all the RAM addresses are continually accessed. The RAM then continuously supplies data which is placed into latch IC18. A latch is needed to enable the RAM to get all the data stable on the outputs, and it is not clocked until this condition is fulfilled. The output data of the latch can then be used while simultaneously another address is supplied to the RAM. The clock pulse for the latch is supplied via N21.

The information in the latch now acts as the address for the character generator, IC19. The CRTC simultaneously supplies to the 2732 the row addresses (RA0 . . . RA3) of every character to be displayed so that one row of dots is read out each time for the video line that is to be written on the screen at that time. IC20 converts the dot information from a parallel to serial format. In order to prevent timing faults from occurring with the high frequencies used the shift register is synchronous, and its clock signal is taken directly from the oscillator via N19 and N20. The serial dot information appears at output Y of the IC. The video mixing stage, consisting of N34, N31, N22 and the circuitry around T1 and T2, combines the Y signal from IC20 with the line and raster synchronization pulses supplied by the CRTC (pins 39 and 40). Presets P1 and P2 can be used to set the size of the synchronization pulses and the dot amplitude. It should be noted that each of the presets has an effect on the other and this will be seen when they are adjusted.

There are two other important signals of the CRTC which have to be dealt with separately. These are DEN and CUR. Output CUR(sor) gives the location of the cursor on the screen and output DEN (Display ENable) indicates when the CRTC is in the active range of the screen (see the section on 'image building' in the descriptive article). The latter signal is needed to keep the screen completely dark outside the active range. These two signals must now be combined with the video signal (via N34 and N31), but that cannot be done directly because of the time that elapses between an address being supplied to the RAM and the appearance of the dot information at the outputs of the EPROM. The delay time is a few hundred nanoseconds, and that would mean that the cursor and display enable signals would appear too early relative to the dot signal. To alleviate the problem, the DEN and CUR signals are delayed by the two whole character times before being mixed with the dot signal.

The links at pin 12 of N33 enable the user to select a bright (lit) or dark cursor on the screen. This in effect means that the whole image on the screen can be either normal or 'negative' (in the photographic sense of the word), because if we want to use a dark cursor then all the dot signals on the screen are also inverted by N34. Link 'T' is used for a normal image (dark background) and using link 'S' gives an inverted image (light background).

N15, N25, N28 and N29 make up the Z80 interface. These gates ensure that the signals supplied by the Z80 are compatible with the R/W and enable signals from the 6502. If using a Z80, links U-V and X-Y must be used. The dotted link at pin 13 of N28 is made if the refresh ($\overline{RFSH}$) of the Z80 is used, or alternatively an external refresh signal can be supplied to this pin. For 6502 and 6800 family processors U-W and X-Z must be linked.



Construction

Any hobbyist who has already constructed other computer projects (for the Junior Computer, for example) will have no problem building the video card, especially if the Elektor printed circuit board as shown in figure 5 is used. This figure only shows the component overlay for this double sided board.

It is recommended that all the ICs should be mounted in good quality sockets. This is quite important for IC3 and IC20 but these ICs should preferably be soldered directly to the printed circuit board as they deal with high frequency signals. T1 is given in the parts list as BSX 20 but a BC 547B is also suitable. It is important to remember to connect the various wire links (in the Z80 interface and the one to select normal or inverted image), and the same applies for the address decoder connections.

If a crystal is used in the oscillator then L1, C1 and C2 can be omitted from the board.

Three EPROMs are needed if the VDU card is to be used with the expanded Junior. These are one 2732 containing the character generator and two 2716s, TMV and PMV, with the video routines. These last two replace the TM and PME EPROMs and, as they contain the TM and PM software, the Junior is none the worse for it.

With the DOS Junior a 2732 with the character generator and one 2716 containing the video routines (DOSVT) are used. The 2716 is mounted in the socket for IC5 on the interface card. A CMOS RAM 6116 is also needed for the DOS Junior and is put in the IC4 socket on the interface card. This interface card requires a few modifications

for correct operation with the VDU card, so:

- pin 18 of IC4 is joined to pin 20
- the following connections are made: M-J, G-I, I'-G', J'-L', O'-M'.

The DOS Junior (unlike the expanded JC) requires a few software changes in order to work correctly with the VDU card.
For this a V 3.3 diskette suitable for the Junior and an Elekterminal or another serial I/O device are needed.
First of all a copy of the diskette is made via Utility 8 and this copy is placed in drive A. Now the modifications given in table 1 are made and the following is entered on the Junior keyboard:

<RST>
<AD> A2Ø0
<DA>

and the bootstrap modifications from table 2 are given. This is followed by:

<AD> A311
<DA> FFFF (video output 1)
FFFF (video output 2)
A2FE (serial output 1)
E1F3 (Centronics output 1)

and then carry on with table 3. When that is done we then have a new V 3.3 diskette adapted to the VDU card.
If there is sufficient interest, we will possibly publish a Paperware to deal with this subject in greater depth, especially as regards the operation of the CRTC and the associated software.
The EPROMs are available as a pre-programmed set from Technomatic Ltd-ESS 522 is for the expanded Junior and ESS 521 for the Junior with DOS.
The circuit works from a single supply of 5 V and draws a current of about 450 mA. When the power is switched on the system must be initialized by pressing the reset button. To set P1 and P2, these two presets are first put to their mid positions. Then they are adjusted to get a clear image on the screen. If a TV set is used instead of a monitor the contrast control must be turned back completely as the bandwidth is generally too large. Trimmers C1 and C2 are used to set the frequency so that the image remains stable on the screen. If a 15 MHz crystal is used in the oscillator this last adjustment is unnecessary. ◀

Table 1.

```
AXCA Ø2ØØ = 39,1

AXCA 2ØØØ = 39,2

AXGO Ø2ØØ

– DISKETTE UTILITIES –

SELECT ONE:
1) COMPAR
2) TRACK Ø READ/WRITE
? 2

– TRACK ZERO READ/WRITE UTILITY –

COMMANDS:
Rnnnn – READ INTO LOCATION nnnn
Wnnnn/9999,P – WRITE FROM nnnn FOR p PAGES
                WITH 9999 AS THE LOAD VECTOR
3 – EXIT TO OS-65D

COMMAND: RA 2ØØ

– TRACK ZERO READ/WRITE UTILITY

COMMANDS:
Rnnnn – READ INTO LOCATION nnnn.
Wnnnn/9999,P – WRITE FROM nnnn FOR p PAGES
                WITH 9999 AS THE LOAD VECTOR
E – EXIT TO OS-65D

COMMAND? E

AXCA AAØØ = Ø1,1

AX
```

Table 1. This is how track Ø of the floppy disk is transferred to the RAM memory starting at address $A2ØØ and track 1 to RAM starting at address $AAØØ.

Table 2.

	Ø	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
A2ØØ :	A9	Ø1	8D	5E	26	2Ø	BC	26	A9	2A	85	FF	2Ø	54	27	86
A21Ø :	FE	2Ø	67	29	2Ø	79	2E	AØ	BF	2Ø	EC	22	FØ	Ø3	88	DØ
A22Ø :	F8	8C	ØØ	23	A2	Ø1	8E	C6	2A	4C	41	22	EA	EA	EA	EA
A23Ø :	EA	EA	EA	EA	EA	EA	EA	EA	EA	EA	EA	EA	EA	EA	EA	EA
A24Ø :	EA	A9	ØØ	8D	F7	EF	8D	D2	EF	2Ø	35	F4	2Ø	3Ø	F3	2Ø
A25Ø :	61	27	2Ø	73	2D	ØD	ØA	ØA	2A	44	4F	53	2Ø	4A	55	4E
A26Ø :	49	4F	52	2Ø	43	4F	4D	5Ø	55	54	45	52	2Ø	2Ø	56	32
A27Ø :	2E	3Ø	2A	ØD	ØA	ØA	43	4F	5Ø	59	52	49	47	48	54	2Ø
A28Ø :	42	59	2Ø	45	4C	45	4B	54	4F	52	ØØ	A9	2E	8D	7C	FA
A29Ø :	A9	FF	8D	7D	FA	A9	ØØ	8D	7A	FA	A9	FC	8D	7B	FA	4C
A2AØ:	E6	2A														

Table 2. This is the data needed to modify the bootstrap section.

Table 3.

```
AXGO Ø2ØØ

– DISKETTE UTILITIES –

SELECT ONE:
1) COMPAR
2) TRACK Ø READ/WRITE
? 2

– TRACK ZERO READ/WRITE UTILITY –

COMMANDS:
Rnnnn – READ INTO LOCATION nnnn.
Wnnnn/9999,P – WRITE FROM nnnn FOR p PAGES
                WITH 9999 AS THE LOAD VECTOR
E – EXIT TO OS-65D

COMMAND? WA 2ØØ/22ØØ,8

– TRACK ZERO READ/WRITE UTILITY –

COMMANDS:
Rnnnn – READ INTO LOCATION nnnn.
Wnnnn/9999,P – WRITE FROM nnnn FOR p PAGES
                WITH 9999 AS THE LOAD VECTOR
E – EXIT TO OS-65D

COMMAND? E

AXSA Ø1,1 = AAØØ/8

AX
```

Table 3. Here we see how the modified bootstrap is written back to the floppy disk.