It has been more than a year since we published the dynamic RAM card (April 1982, Elektor No. 84), but it is proving to be very popular. Many readers have asked about the possibility of replacing the eight 16 k memory ICs with 64 k chips. Many people suggested how this could be done and all these ideas prompted us to investigate the feasibility. What we came up with is a sort of check list of modifications, which you can tick as you go along.

64 k on the 16 k Dynamic RAM card

524 288 bits = (8 x 64 k) – (8 x 16 k)

We have often thought that we are rather fortunate since electronic components are one of the very few commodities that actually decrease in price. This is currently the situation with the 64 k dynamic RAM ICs, which are also, incidentally, becoming more readily available from a number of different sources. Considering the fact that the majority of 4164s (the first two digits vary from manufacturer to manufacturer) require only a single 5 volt supply, the dynamic RAM card could use 64 k RAMs. Some of the advantages to be gained are, more 'bits per pound', the connectors on the bus card can still be used (an 8 x 64 k card is enough for all the memory space addressable by an 8 bit microprocessor) and the current consumption will be less. The only drawback is the need for 'surgery' to the existing circuitry. Basically, to quadruple the capacity of the memory card all that is needed is to cut a few tracks and make a few new connections.

1

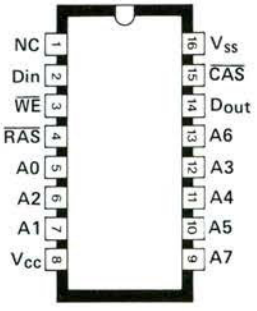


Figure 1. This is the pin designation for a 4164 dynamic RAM IC. Comparison with a 4116 shows that they are pin compatible except for pins 1, 8 and 9: an extra address line is added (A7) and the –5 V and +12 V supplies are removed.

A0-A7	Address Inputs
$\overline{CAS}$	Column Address Strobe
Din	Data In
Dout	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Read/$\overline{Write}$ Input
Vcc	Power (+5 V)
Vss	Ground

Deletions

Rather than leave anything to chance we have drawn up a list of everything that has to be done, starting with 'demolition' and finishing with 'reconstruction'. All modifications are shown in figures 2 and 3 which are the circuit diagram and printed circuit board layout respectively.

- Remove IC11 . . . 19 from their sockets.
- Take out capacitors C3, C12 . . . C15, C19 and C20.
- Remove the strap parallel to IC9. We mean the first strap to the right, between the IC and the connector. It connects pin 9 of the 4116s to +5 V.
- Cut the tracks joining:

– pin 2 of IC4 (N18) to ground
– pin 2 of IC5 (N19) to ground (remember to remake the connection to ground that this breaks)
– pin 8 of IC12 . . . 19 to +12 V
– pin 1 of IC12 . . . 19 to –5 V
– pin 6 of IC7 (N29) to pin 5 of IC2 (N47)
– pin 5 of IC2 to pin 10 of IC8 (N31)
– pin 2 of IC10 to ground
– pin 3 of IC10 to ground
– pin 2 of IC10 to pin 3 of IC10.

Check the breaks with a (lack of !) continuity tester.

New connections

The next stage consists of making connections between

from an idea by
K. D. Lorig

- pin 8 of IC12 . . . 19 and pins 1a/1c of the connector (+5 volt supply)
- pin 6 of IC7 (N29) and pin 10 of IC8 (N31)
- pin 8 of IC8 (N31) and pin 5 of IC2 (N47)
- pin 8 of IC6 and pin 2 of IC5 (N19)
- pin 4 of IC10 and pin 2 of IC4 (N18)
- pin 2 of IC10 and pin 19c of the connector (A14)
- pin 3 of IC10 and pin 19a of the connector (A15)
- pin 18 of IC4, pin 18 of IC5 and pin 9 of IC12 . . . 19 (A7)
- pin 9 and pin 10 of IC7 (V-W)
- pin 12 and pin 13 of IC7 (X-Y).

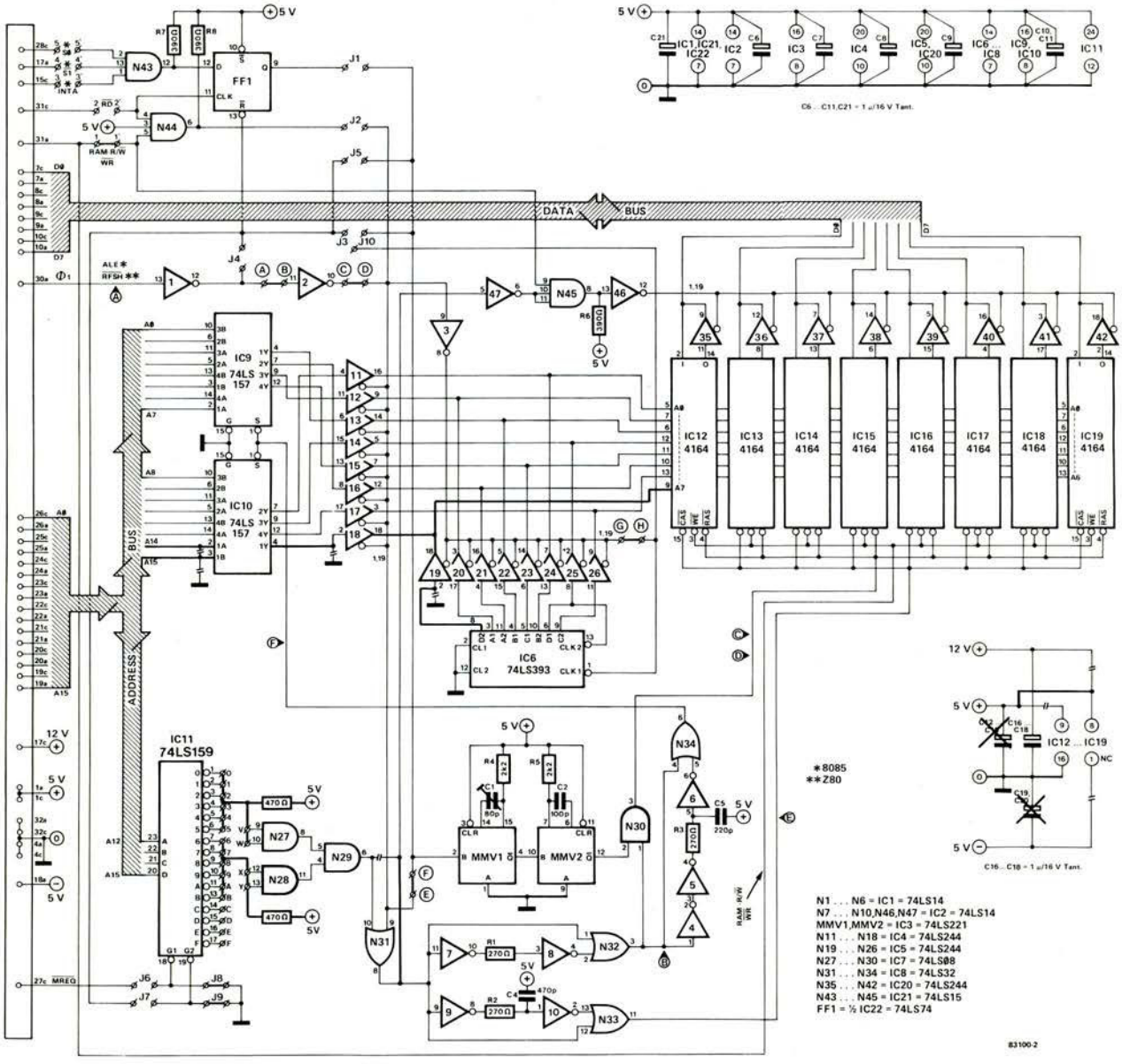
Except for decoding the desired addresses the output pins of the address decoder IC11 leave in two groups, one connected to the V/W input of IC7 and the other to the X/Y input and each is connected to the high logic line via a 470 Ω resistor. If it is decoded as indicated in the diagram the card will be addressed between $0000 and $BFFF without interruption. This is the configuration used for the Junior Computer with DOS. Make the connections shown in figure 3 as two lines from ground to pins 4a and 4c of the connector.

Additional components

When all the modifications mentioned above have been made most of the work is done. All that remains is to substitute a 74LS159

Figure 2. Most of the circuit diagram for the 16 k card remains the same. The modifications consist of adding two address lines (A14 and A15) to enable all of the memory to be addressed, and replacing the address decoder (74154) by its counterpart with open collector outputs, which may be shorted together.

2



3

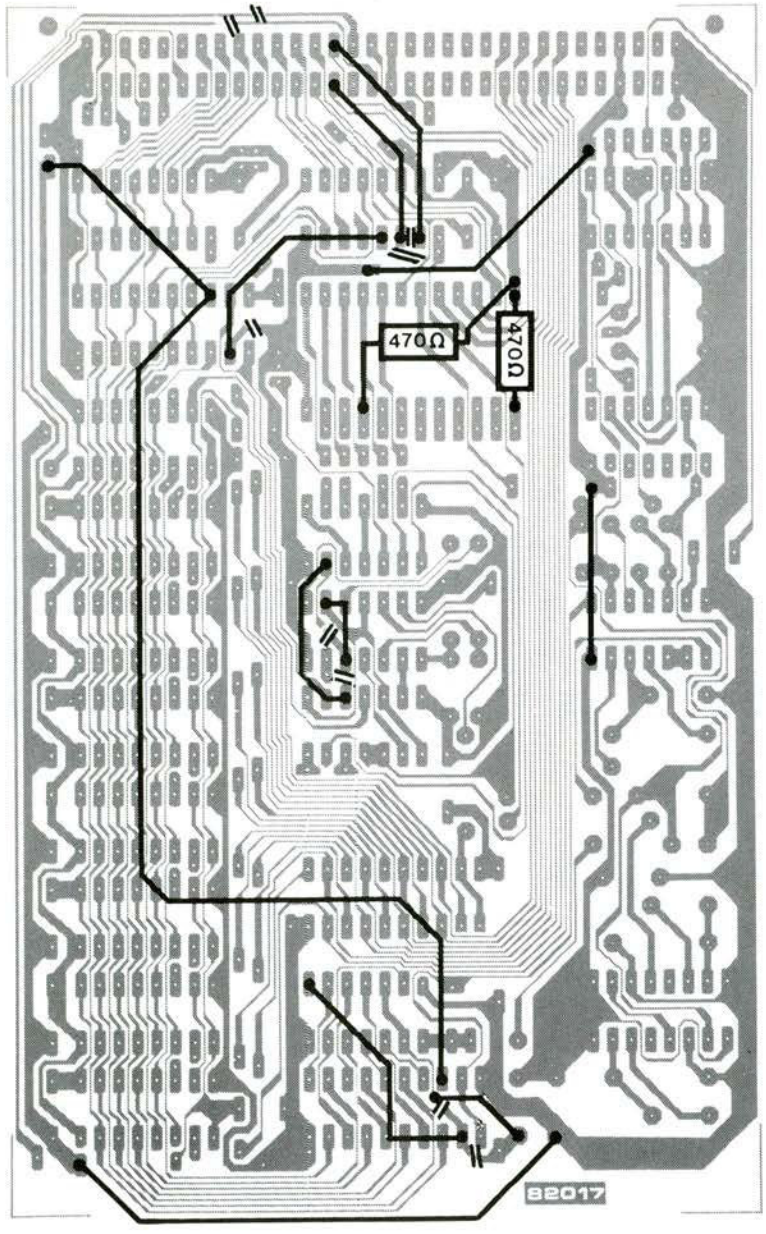
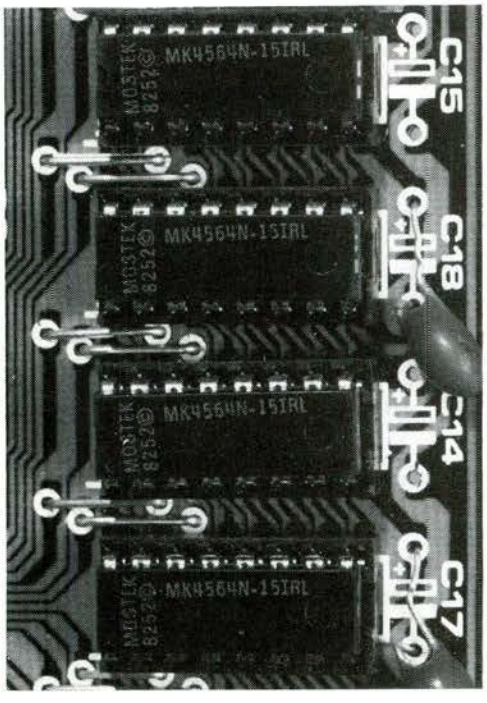


Figure 3. This layout of the printed circuit board clearly shows the tracks that have to be cut and the new connections that are to be made. Note that some ground lines are too narrow for this application and therefore need to be reinforced. And don't forget to remove the strap beside IC9.



(open collector outputs) for the 74LS154 (IC11). If it has not already been done C1 can be replaced by an 80 pF variable capacitor. This is to enable the timing relationship between the triggering of MMV1 and the start of the refresh pulse to be set to prevent the refresh from occurring too soon.
It is a good idea at this stage to run through everything done so far just to check that all is as it should be. Then the last thing to do is to inert all the new memory ICs in their sockets. They are available from a number of different manufacturers, most of whom are Japanese, and have different 'names', except that the last two digits are always '64'. Some possible examples are F 4164 (Fairchild), MB 8264 (Fujitsu), HM 4864 (Hitachi), ITT 4164, MSK 4164 (Mitsubishi), MK 4564 (Mostek), NMC 4164 (National Semiconductor), UPD 4164 C/D and so on . . . the choice is yours. In the article on the 16 k DRAM card the principle of the refresh was described in detail and a program was given for checking the memory, so as a final check it is worthwhile to run this program to check the 524 288 bits of your 'new' card. ⏹