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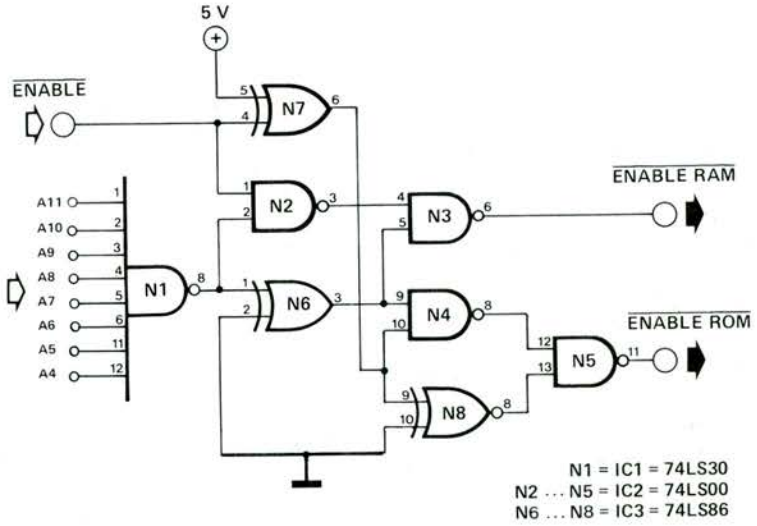
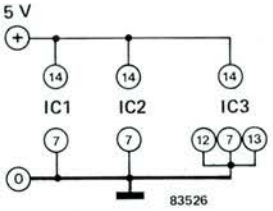
vector control for the Junior Computer



The circuit described in this article makes it possible to read out the necessary vector data from the standard EPROM of the Junior Computer, without having to give up a considerable part of the address range and/or requiring an additional ROM. The vectors for NMI, RES and IRQ are located at the addresses FFFA . . . FFFF. The complete memory range of F000 . . . FFFF would be 'sacrificed' for 6 bytes if the above vectors were to be read out of the standard EPROM according to the method described in the Junior Computer Book 3. This means a loss of 4 K memory location. With the solution described here, only 16 bytes are reserved to read out these 6 bytes. Obviously, this circuit is only needed if the constructor



wants to put RAM in the upper memory range of F000 . . . FFFF, for example if the mini EPROM card (Elektor April 1982) is used.
The circuit only consists of 8 gates. It generates two separate enable signals out of an 'ordinary' enable signal, for this highest 4 K range. A new $\overline{\text{ENABLE RAM}}$ signal is given at addresses F000 . . . FFFF. However no $\overline{\text{ENABLE RAM}}$ signal is given at addresses FFF0 . . . FFFF, but an $\overline{\text{ENABLE ROM}}$ signal is sent to the standard EPROM of the Junior Computer.
The complete circuit can be mounted onto the corresponding RAM card because it only consists of three ICs. The old $\overline{\text{ENABLE}}$ line for the range F000 . . . FFFF of the address decoder on the RAM card (which is output F of IC11 on the dynamic RAM card) is connected to the 'supplement/additional' circuit and the eight inputs of N1 are connected to the address lines A4 . . . A11. A new $\overline{\text{ENABLE RAM}}$ signal will therefore go to the RAM card, which means that this line is attached to one of the points V, W, X or Y of the dynamic RAM card. The $\overline{\text{ENABLE ROM}}$ line must be linked to K7 (pin 14a) of the connector.