JOLT

SUPER JOLT

CP110

First Edition

Microcomputer Associates Inc.
Santa Clara, California

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SECTION 1

SUPER JOLT START-UP

HOOKING UP THE POWER SUPPLY

The proper power supply is an important part of your SUPER JOLT system. Be sure to check your power source and have identified the proper connections and have tested the power supply to be certain that all voltages are proper and that none have overvoltage surges when TURNING ON power.

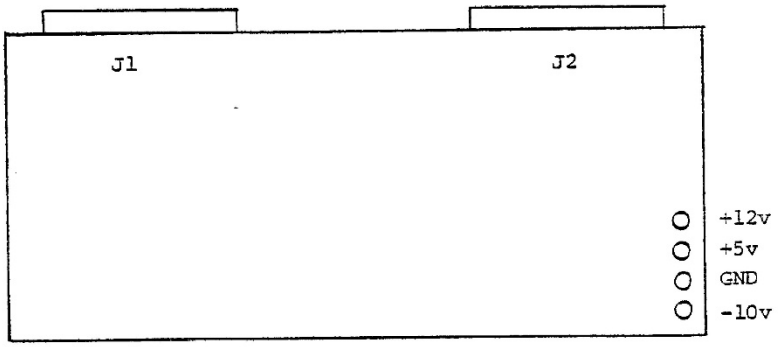
Your SUPER JOLT card requires a minimum of two voltages and one ground connection. The card, as delivered will perform with +5v, GND, and -10v if you are using the TTY current loop. If you plan to use the EIA terminal connection or 2708 PROMS you will need to add the +12v supply. Power supply requirements are listed below.

POWER SUPPLY REQUIREMENTS

	TYPICAL		MAXIMUM	
Voltage	W/ROMs*	W/O ROMs*	W/ROMs	W/O ROMs
+12v±5%	70 ma	4.4 ma	110 ma	6 ma
+5v±5%	550 ma	520 ma	880 ma	850 ma
-10v±5%	30 ma	30 ma	40 ma	40 ma

* SW101 TINY BASIC/Resident Assembler ROMs

All power connections are hooked up as indicated below and as marked on the P.C. card.



HOOKING UP A TERMINAL TO THE JOLT

Types of Terminals: The following is a list of qualifications a terminal must have to run on a SUPER JOLT system with DEMON™ installed:

A. Character Set: Must transmit and receive the standard ASCII character set. (64, 96, or 128 character).

B. Mode: Mode of transmission is bit serial full duplex (full duplex is where the keyboard sends only to the computer and the computer sends only to the printer).

C. Transmission Rate: Transmission rate can be anything from 110 to 300 baud (10 to 30 characters per second) the SUPER JOLT will synchronize to the baud rate of the terminal.

D. Bit Serial Format: Start bit, seven data bits, one parity bit (this bit is ignored by DEMON™ on receive and set to a "1" on transmit), and one, one and a half, or two stop bits.

E. Electrical Interface: Any one of three types of electrical interfaces can be used with the SUPER JOLT

1. RS-232C (EIA)
2. 20 milliamp current loop interface
3. TTL logic interface

HOOKING UP THAT ELECTRICAL INTERFACE

E.I.A.: The first type of interface we will discuss is the E.I.A. or RS-232C standard, here after refered to as E.I.A.. Table 1 shows the complete standard for signal assignment on the 25 Pin Cannon connector which is the standard connector for terminal-modem computer hookup with E.I.A.. Figure 1 shows the connection of a typical E.I.A. terminal to the SUPER JOLT CPU. When using the SUPER JOLT with an E.I.A. interface equipped terminal, connections should be made in this fashion. Note that the D.S.R. signal from the CPU is required only on some terminals.

TTY CURRENT LOOP

The most common example of a current loop interfaced terminal is the model ASR33 Teletype™. Before hooking up your Teletype™ or other current loop type terminal

RS-232 STANDARD SIGNALS AT THE TERMINAL

* Signals Commonly Used

PIN	FUNCTION
*1	Protective ground
*2	Transmitted data
*3	Received data
4	Request to send
5	Clear to send
6	Data set ready
*7	Signal ground
8	Data carrier detector
9	Reserved for data set testing
10	Reserved for data set testing
11	Unassigned
12	Unassigned
13	Unassigned
14	Unassigned
15	Unassigned
16	Unassigned
17	Unassigned
18	Unassigned
19	Unassigned
20	Data terminal ready
21	Unassigned
22	Ring indicator
23	Unassigned
24	Unassigned
25	Unassigned

TABLE 1

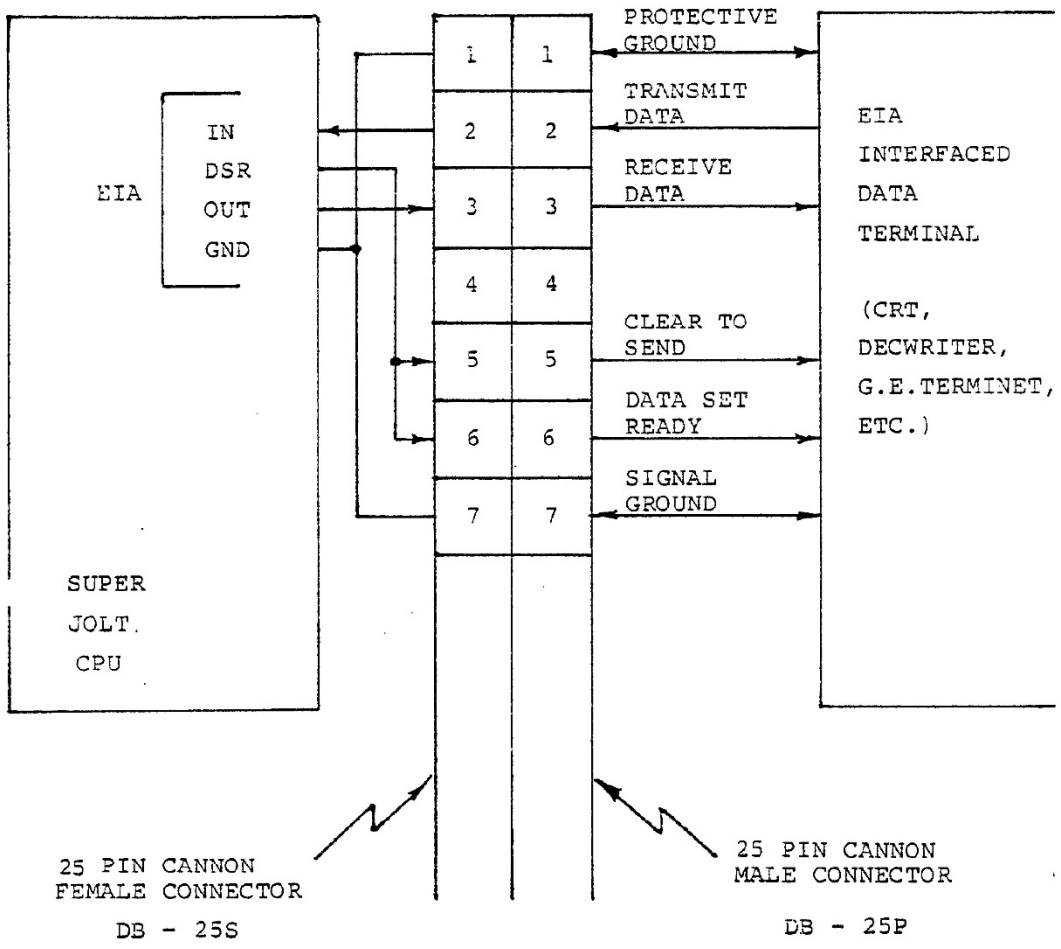


FIGURE 1. SUPER JOLT HOOKED TO AN EIA EQUIPPED TERMINAL

refer to its maintanence manual and be certain that it is set up for 20 milliamp current loop operation and identify the four interface wires shown in Figure 2 for the Teletype™. If your Teletype™ also has a paper tape reader, then check to see that it is an automatic reader as SUPER JOLT does not supply a "reader run" relay control circuit.

Unlike RS-232C, the 20 milliamp current loop interface has no standard connector. Every computer and terminal manufacturer has their own type of connector. For interfacing the SUPER JOLT you should select a connector that mates with the one on your particular model Teletype™.

Figure 2 shows a typical teletype hookup to SUPER JOLT using the 20 milliamp current loop interface.

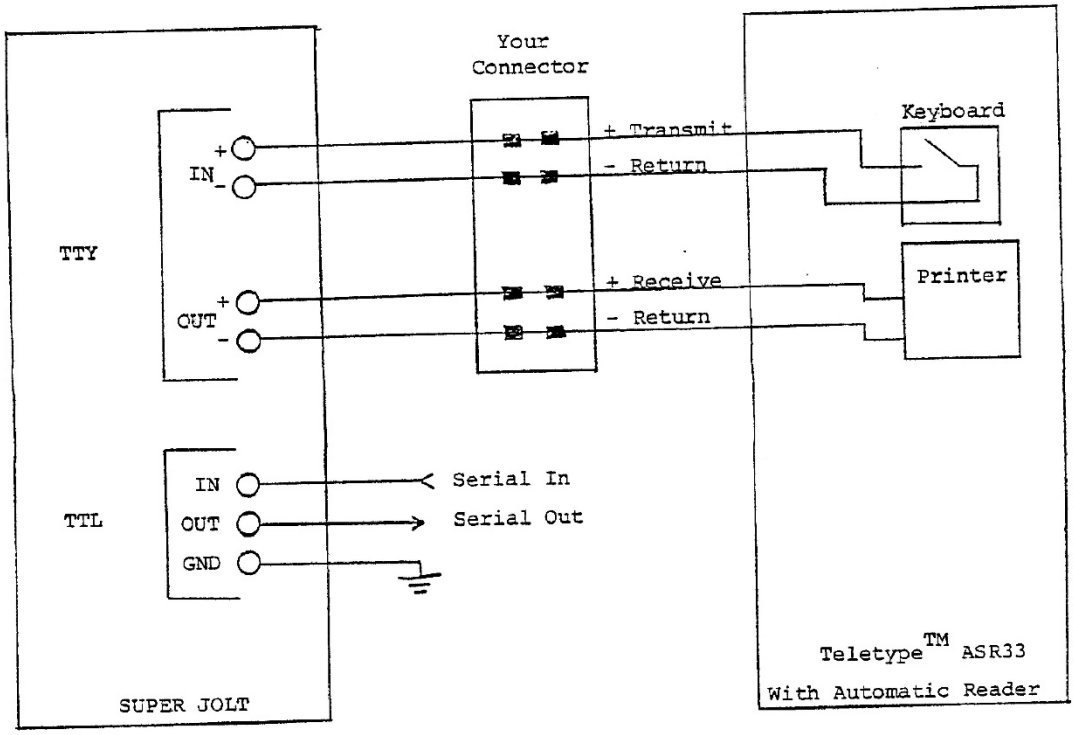


FIGURE 2. SUPER JOLT HOOKED TO A 20 ma CURRENT LOOP TELETYPE™ OR TTL INTERFACE

TTL

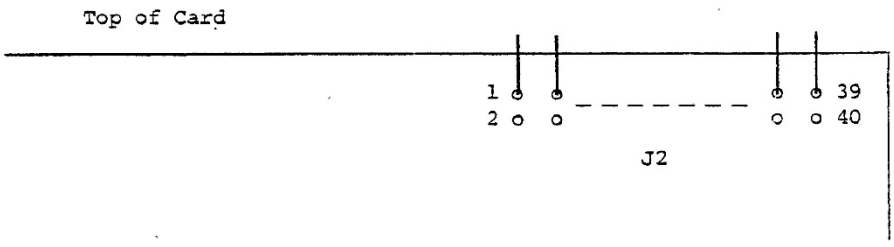
The third type of serial interface to the SUPER JOLT is "TTL" which is a direct logic level interface. Most commercial terminals do not use this type of interface, however some homemade terminals and inexpensive terminals use this method to save costs in interfacing (i.e. the T.V. typewriter). Interfacing this type of equipment to the SUPER JOLT CPU is provided for. See figure 2 for the proper connections.

READY TO RUN?

Your SUPER JOLT card comes ready to power-up automatically to the on-board debugger-monitor DEMON™ using a TTY. Refer to section 4 on using DEMON™. If you wish to power-up to your application program in 2708 PROM refer to section 3 for selection of the proper on-board jumpers. Many other jumper options are available concerning negative power input, 6530 on-board RAM, terminal input and address line tristate control. The user should become very familiar with the function of each option in order to most effectively use the SUPER JOLT card. Again, if you have a TTY (20 ma current loop) and a power supply your SUPER JOLT is ready-to-use with no jumper changes. Power-up or reset will cause the 6502 CPU to execute the DEbug MONitor.

HOOKING UP THE I/O

SUPER JOLT is designed with two types of connectors. The first, called J1, is on the upper left and is used mainly for system expansion such as RAM, PROM, I/O etc. J1 should only be used to expand to other available SUPER JOLT cards or for your own special card designs. The second, called J2, is on the upper right and contains all on-board I/O lines. Table 2 list J2 I/O pin #'s and software address assignments and Table 3 list available mating connectors. Pin numbering on both connectors is illustrated as follows:



PART #1	Bit #	NAME	PIN #	ADDRESS
	0	PA0-1	31	
	1	PA1-1	32	6520 PIA
	2	PA2-1	30	4600 Direction/Data
	3	PA3-1	29	4601 Control
	4	PA4-1	28	
	5	PA5-1	27	
	6	PA6-1	33	
	7	PA7-1	34	
	Interrupt input	CA1-1	38	
	Output Control	CA2-1	39	

PORT #2	BIT #	NAME	PIN #	
	0	PB0-1	35	
	1	PB1-1	36	6520 PIA
	2	PB2-1	37	4602 Direction/Data
	3	PB3-1	26	4603 Control
	4	PB4-1	25	
	5	PB5-1	24	
	6	PB6-1	23	
	7	PB7-1	22	
	Interrupt Input	CB1-1	21	
	Output Control	CB2-1	20	

PORT #3	BIT #	NAME	PIN #	
	0	PA0-2	10	
	1	PA1-2	15	6530 I/O
	2	PA2-2	16	6E00 Data
	3	PA3-2	17	6E01 Direction
	4	PA4-2	18	
	5	PA5-2	19	
	6	PA6-2	14	
	7	PA7-2	13	

PORT #4	BIT #	NAME	PIN #	
	2	PB2-2	12	6E02 Data
	3	PB3-2	11	6E03 Direction

TABLE 2. SUPER JOLT I/O ASSIGNMENTS ON J2

FOR FLAT CABLE CONNECTIONS

T & B ANSLEY P/N: 609-4000

SPECTRA-STRIP P/N: 802-140

3M P/N: 3417-0000

FOR P.C. MOUNTING

AMP P/N: 86418-2

FLAT CABLING

T & B ANSLEY P/N: 171-40

SPECTRA-STRIP: Many Types

3M P/N: 3302/40, 3365/40, 3469/40, 3476/40

TABLE 3. J1 & J2 MATING CONNECTOR

SECTION 2

SUPER JOLT MODULE

General

The SUPER JOLT CPU card is a complete microcomputer on a single printed circuit board. When connected to a terminal, the CPU card provides everything necessary to begin writing, debugging and executing microcomputer programs. The salient features of the SUPER JOLT CPU card are:

- A MOS Technology MCS6502 NMOS microprocessor
- 1024 bytes of program RAM, and 64 bytes of interrupt vector RAM
- 1024 bytes of mask programmed ROM containing DEMON™, a powerful debug monitor
- Sockets for 2048 bytes PROM memory
- 28 programmable I/O lines
- Crystal controlled clock
- Serial I/O ports for use with a teleprinter current loop drive/receiver, EIA standard driver/receiver, or TTL
- Expandable address and data buses
- Buffered CPU address and data lines
- Hardware interrupts
- Control panel interface lines available on card connector
- Optional ROM resident TINY BASIC and Assembler

The CPU card was designed to be a general purpose microcomputer with provisions for expanding memory and interfacing to serial or parallel I/O devices. System expansion may be accomplished through the use of standard SUPER JOLT support cards.

CPU

The MCS6502 CPU chip is a parallel 8-bit NMOS microprocessor with 16 address lines and an internal oscillator. The data bus (D0-D7) is bi-directional and will drive one TTL (1.6 ma, 130 pf) load directly. The 64K byte (2^{16}) address space is used to address program memory and to select I/O devices for communication with the CPU. The address will also drive one TTL (1.6 ma, 130 pf) load directly. On-board address and data buffers expand the drive capability to 48 ma.

The internal oscillator operates in a "free run" mode based on a crystal oscillator frequency of 1 MHZ. The crystal provides a very stable clock which allows for accurate and repeatable programmed timing loops.

The RESET input to the CPU is pulled to logic ground by a 555 timer circuit on the printed circuit board. The CPU normally fetches a new program count vector from hex locations FFFC and FFFD upon activation of the RESET line, but these locations are in the interrupt vector RAM and therefore volatile. Hardware on the CPU board causes the CPU to begin executing the monitor program by forcing the effective sixteenth bit of the address bus (A15) to a logic ZERO during reset. As a result, the RESET function on the SUPER JOLT CPU card cause the debug monitor (DEMON™) to begin executing. This can be altered by changing the various on-board jumpers. (see section 3)

There are two interrupt inputs to the CPU. One interrupt is maskable under program control ($\overline{IRQ}$) and the other ($\overline{NMI}$) is not.

A READY control line provides for asynchronous operation with slow memory or I/O devices.

The address bus (A0-A15), the data bus (D0-D7), the two phase clock (PIT,P2T), the reset line (*RESET), the interrupt lines (*IRZ, and *NMI) and the ready line (RDY) are all available at the edge connector of the CPU card.

A more detailed description of the CPU inputs and outputs may be found in the MCS6500 hardware manual available from MOS Technology Inc.

PROGRAM RAM

There are 1024 bytes of program RAM provided on the CPU card. The program RAM is hardwired addressed as the first 1024 bytes of the CPU's 64K of memory address space. It may become necessory to remove these RAM's from their sockets if a 4K memory card is also hardwired in this address space. The program RAM on the CPU card uses 2114 4K static RAMs.

MONITOR ROM AND INTERRUPT VECTOR RAM

The monitor ROM is located in the last 1K bytes of the lower half of memory space (first 32K bytes). The interrupt vector RAM is located in the last 64 bytes of the 64K memory address space.

The monitor ROM and interrupt vector RAM as well as additional I/O are implemented with a single MPS6530 chip.

PROGRAMMABLE USER I/O

The programmable I/O lines available from the CPU card are provided by a Peripheral Interface Adapter (PIA) and the 6530 multi-function chip.

The PIA has two 8-bit I/O ports with two interrupt-causing control lines each. A data direction register for each port determines whether each I/O line is an input or an output. A detailed description of the PIA chip may be found in the MCS6500 microcomputer family Hardware Manual.

The 6530 ROM chip provides 10 additional I/O lines that may also be specified as input or output lines under program control. There are eight I/O lines from one port on the 6530 and two lines from the second port. These I/O lines may be used in conjunction with DEMON™ for interfacing a high speed paper tape reader to the CPU card. In the paper tape reader application, the eight I/O lines from the second port are used to accomplish the handshake control between the reader and the CPU card.

The PIA is hardwired addressed as location 4600_{16} to 4603_{16} in the memory address space. Memory addresses from 4000_{16} to $5C03_{16}$ are allocated for PIA devices so that the SUPER JOLT system may be easily expanded to accomodate up to eight PIA chips. For a complete illustration of memory allocation refer to section 3.

STANDARD INTERFACE CIRCUITS

The SUPER JOLT CPU card provides direct interfacing with a 20 ma current loop RS232C interface requires +12v and -10v. Both interfaces are wired in parallel on the input and output thereby allowing both interfaces to be used simultaniously. The TTL input must be jumpered as an option in place of the EIA input. For further assistance in connecting the SUPER JOLT CPU to a terminal refer to section 1.

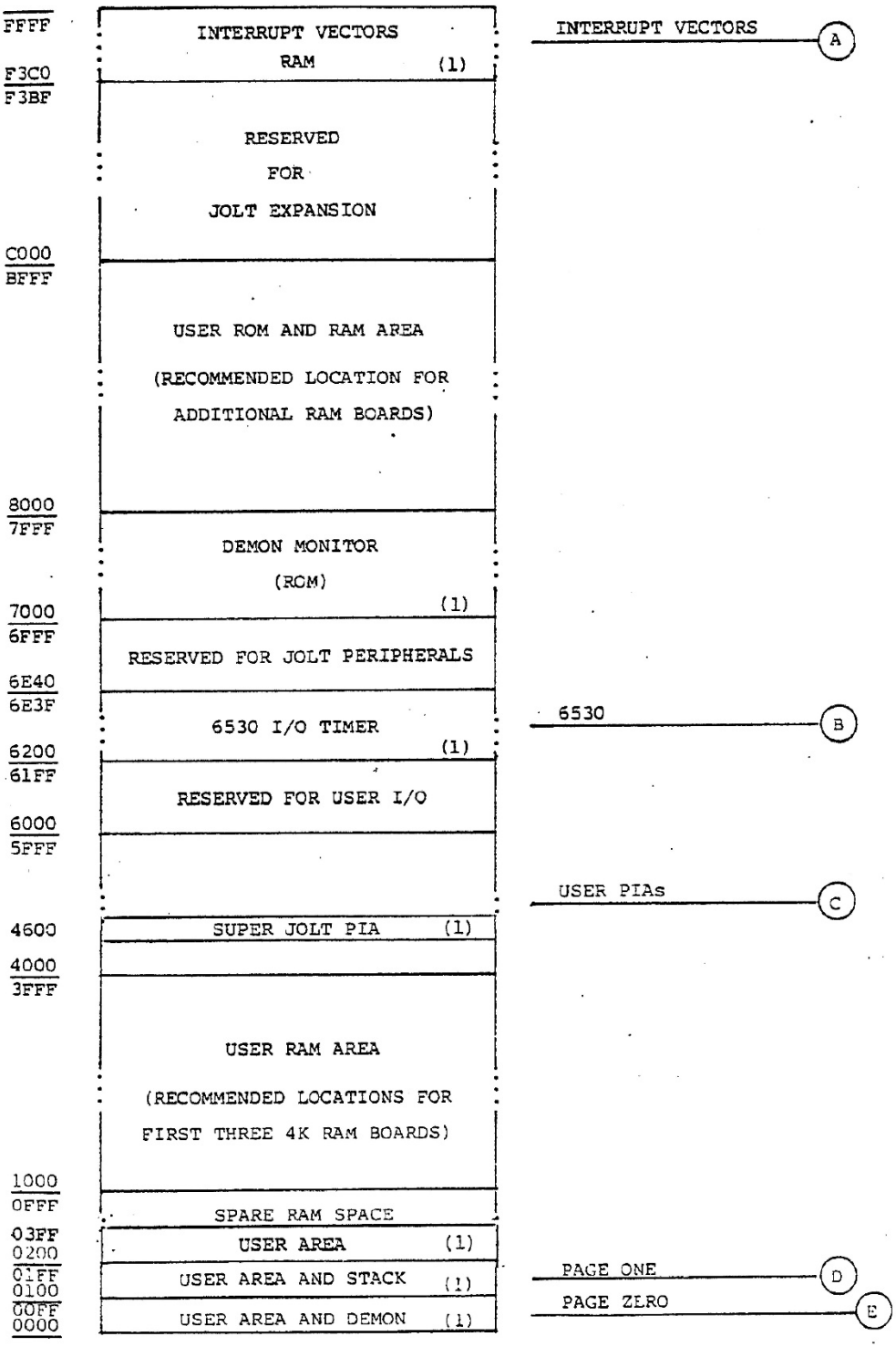
SECTION 3

MEMORY MAP AND ON-BOARD JUMPER OPTIONS

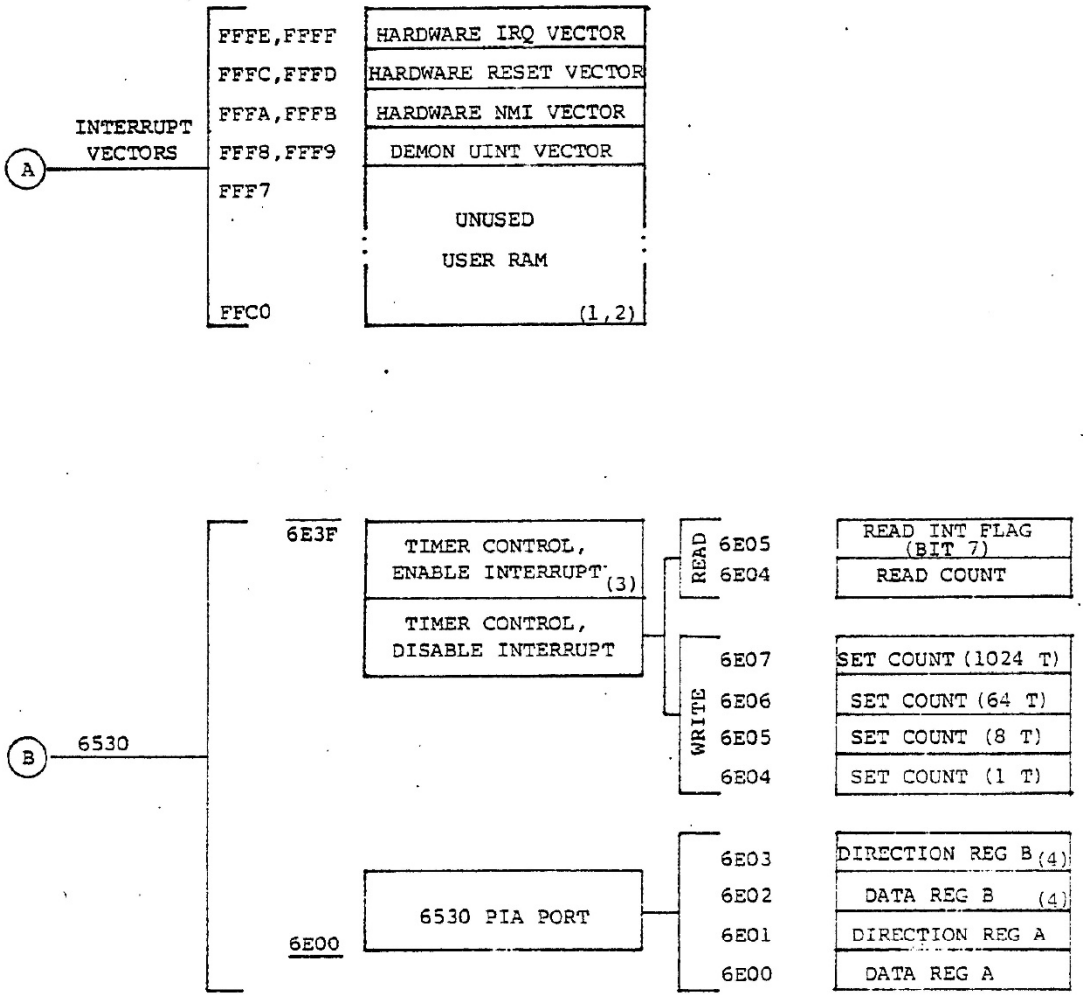
SUPER JOLT SYSTEM MEMORY MAP

The memory map on the following pages explains what functions have been assigned to each segment of the SUPER JOLT address space. It is recommended that users respect this space allocation when adding memory and peripherals to their SUPER JOLT systems. Space has been reserved for 32K bytes of user RAM or ROM, seven additional PIA devices, and up to 512 user I/O devices registers. Other areas are reserved for JOLT expansion, i.e., new SUPER JOLT peripherals and memory options will use these spaces. Users are advised to not use SUPER JOLT expansion space unless absolutely necessary.

Note that some areas used by the SUPER JOLT CPU board and PIA boards have more space indicated than there are registers or locations in the device occupying them. This is because these devices do not decode all address bits, or use some of the address bits for special functions. For example, the 6530 timer determines the time scale and interrupt enable/disable by the address used to access it. Thus, these "partly filled" areas are actually entirely used and are not available for other uses.



(1) Standard on SUPER JOLT CPU Card

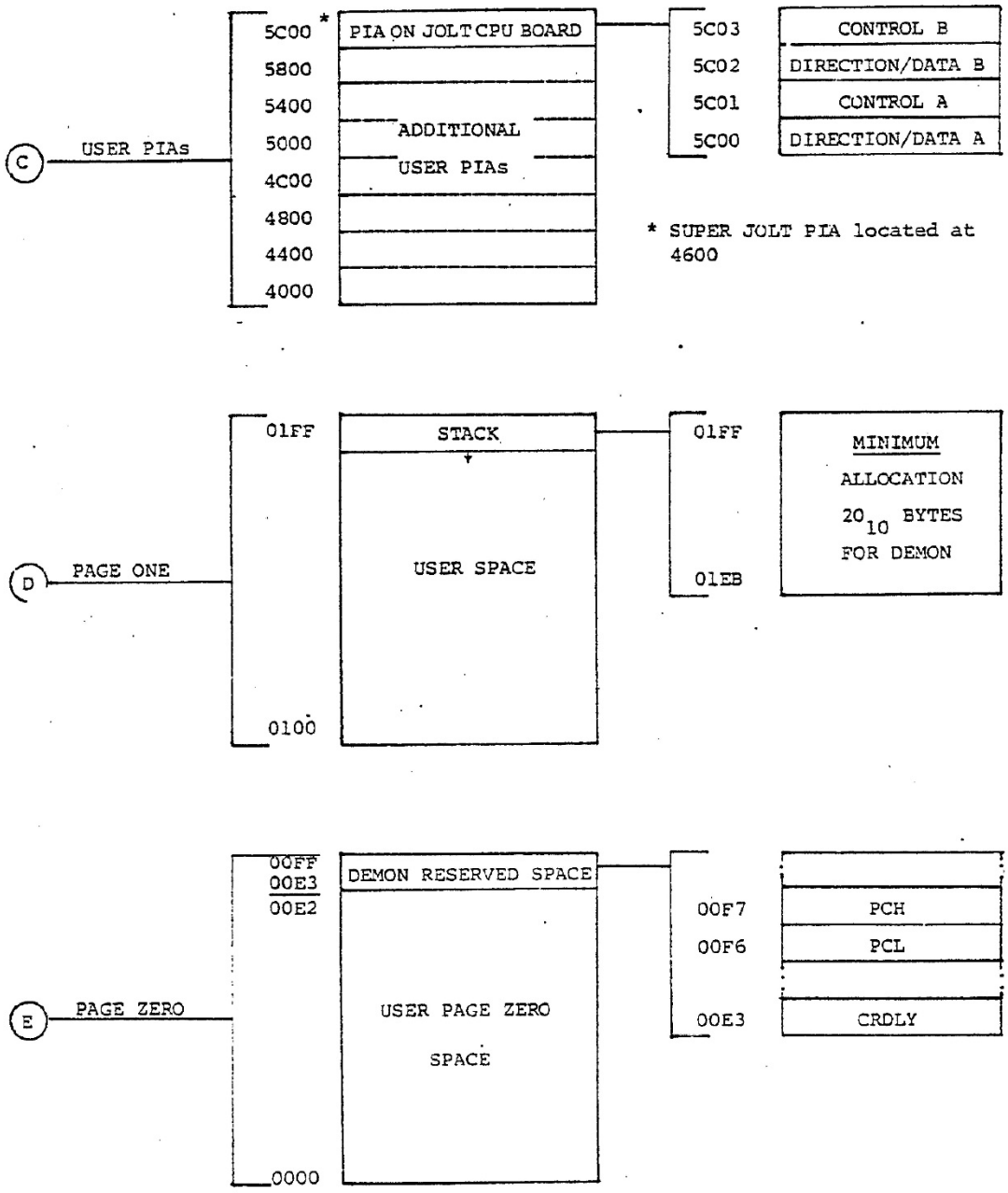


(1) Standard on JOLT CPU board.

(2) Available to user—not used by DEMON.

(3) To get enable-interrupt address, add 0008_{16} to disable-interrupt address with corresponding functions.

(4) Reserved for DEMON use—TTY control and reset functions.


C
USER PIAs
5C00 *
5800
5400
5000
4C00
4800
4400
4000
PIA ON JOLT CPU BOARD
ADDITIONAL
USER PIAs
5C03
5C02
5C01
5C00
CONTROL B
DIRECTION/DATA B
CONTROL A
DIRECTION/DATA A
* SUPER JOLT PIA located at 4600
D
PAGE ONE
01FF
0100
STACK
USER SPACE
01FF
01EB
MINIMUM
ALLOCATION
20_{10} BYTES
FOR DEMON
E
PAGE ZERO
00FF
00E3
00E2
0000
DEMON RESERVED SPACE
USER PAGE ZERO
SPACE
00F7
00F6
00E3
PCH
PCL
CRDLY

JUMPER	POSITION	APPLICABLE ADDRESS OPTION	DESCRIPTION
A	1 2		ADDRESS BUFFERS ALWAYS ENABLED ADDRESS BUFFERS TRI-STATE EXTERNALLY CONTROLLED
B	3 4		-10v POWER INPUT (ON-BOARD REGULATED TO -5v) -5v POWER INPUT (BY-PASSES REGULATOR)
C (1)	5 6		AUTO POWER-ON TO "DEMON" - ENABLED AUTO POWER-ON TO "DEMON" - DISABLED
D	7 8	E,F,G,H A,B,C,D	A11 CONTROL'S ROM SOCKET SELECTION A10 CONTROL'S PROM SOCKET SELECTION
E	9 10	E,F,G,H A,B,C,D	A15 ROM ADDRESS ENABLE A11 PROM ADDRESS ENABLE
F	11 12	C,D,G,H A,B,C,D	$\overline{\text{A13}}$ PROM/ROM ADDRESS ENABLE A13 PROM/ROM ADDRESS ENABLE
G	13 14	E,F,G,H A,B,C,D	A10 ROM ADDRESS ENABLE -5v PROM ADDRESS ENABLE
H (1)	15 16	 A,E	ENABLES 16 BYTE RAM ON 6530 DISABLES 64 BYTE RAM ON 6530
J	17 18	B,D,F,H A,C,E,G	A12 PROM/ROM ADDRESS ENABLE A12 PROM/ROM ADDRESS ENABLE
K	19 20		EIA INPUT TTL INPUT

NOTE: (1) - The purpose of option H-16 is to allow PROM or RAM memory to exist at high address locations (such as F---) while still using the 6530 I/O - timer and "DEMON" subroutines, however, use of this option disables the Auto Power-On to "DEMON" (Jumper C must be in position 6)

EXAMPLES		FUNCTION
C-6	H-16	PWR. ON TO PROM/ROM MEMORY AT RESET VECTOR
C-6	H-15	PWR. on to 6530 RAM (not useful)
C-5	H-16	AUTO PWR.-ON DISABLED, 6530 RAM DISABLED
C-5	H-15	AUTO PWR.-ON, 6530 RAM ENABLED

SUPER JOLT ON-BOARD JUMPER OPTIONS

ADDRESS BITS →	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			ADDRESS OPTION
START ADDRESS																			
F800	1	1	1	1	1	0	-	-	-	-	-	-	-	-	-	-	(1Kx8)	2708 PROM-1	A
FC00	1	1	1	1	1	1	-	-	-	-	-	-	-	-	-	-		2708 PROM-2	
E800	1	1	1	0	1	0	-	-	-	-	-	-	-	-	-	-		2708 PROM-1	B
EC00	1	1	1	0	1	1	-	-	-	-	-	-	-	-	-	-		2708 PROM-2	
D800	1	1	0	1	1	0	-	-	-	-	-	-	-	-	-	-		2708 PROM-1	C
DC00	1	1	0	1	1	1	-	-	-	-	-	-	-	-	-	-		2708 PROM-2	
C800	1	1	0	0	1	0	-	-	-	-	-	-	-	-	-	-		2708 PROM-1	D
CC00	1	1	0	0	1	1	-	-	-	-	-	-	-	-	-	-		2708 PROM-2	
F000	1	1	1	1	0	-	-	-	-	-	-	-	-	-	-	-	(2Kx8)	9216 ROM-1	E
F800	1	1	1	1	1	-	-	-	-	-	-	-	-	-	-	-		9216 ROM-2	
E000	1	1	1	0	0	-	-	-	-	-	-	-	-	-	-	-		9216 ROM-1	F
E800	1	1	1	0	1	-	-	-	-	-	-	-	-	-	-	-		9216 ROM-2	
D000	1	1	0	1	0	-	-	-	-	-	-	-	-	-	-	-		9216 ROM-1	G
D800	1	1	0	1	1	-	-	-	-	-	-	-	-	-	-	-		9216 ROM-2	
C000	1	1	0	0	0	-	-	-	-	-	-	-	-	-	-	-		9216 ROM-1	H
C800	1	1	0	0	1	-	-	-	-	-	-	-	-	-	-	-		9216 ROM-2	
7000	0	1	1	1	X	X	-	-	-	-	-	-	-	-	-	-	1Kx8 6530 "DEMON" ROM		
0000	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-		1Kx8 RAM	
FFC0	1	1	1	1	X	X	1	1	1	1	-	-	-	-	-	-		64x8 6530 RAM	
4600	0	1	0	0	0	1	1	X	X	X	X	X	X	X	-	-		6520/6820 PIA	
6E00	0	1	1	0	X	X	1	0	0	0	-	-	-	-	-	-		6530 I/O TIMER	

(1) Legend for Above:

- Address lines decoded inside memory or I/O chip
0 Address line logic state for valid enable
1 Address line logic state for valid enable
X Indicates address line not used in decoding

(2) How to use: Select one (1) address option from A-H, then use jumper option chart to determine the required on-board jumpers.

(3) Address Decoding equations on-board (inside) 6530 Chip

RSO = PIN 4 CSI = PIN 18 CS2 = PIN 19

ROM ENABLE = $\overline{RSO}$·CSI·CS2
= $\overline{A15}$·$\overline{A14}$·A13·A12 (for Super Jolt)

RAM ENABLE = RSO·CSI·CS2·A9·A8·A7·A6
= $\overline{A15}$·A14·A13·A12·$\overline{A9}$·$\overline{A8}$·$\overline{A7}$·A6

I-O/TIMER ENABLE = $\overline{RSO}$·CSI·CS2·$\overline{A9}$·$\overline{A8}$·$\overline{A7}$·$\overline{A6}$
= $\overline{A15 \cdot A14 \cdot A13 \cdot A12 \cdot A9 \cdot A8 \cdot A7 \cdot A6}$

SUPER JOLT MEMORY - I/O DECODING MAP

SECTION 4

DEMON™ SOFTWARE MANUAL

NOTE

The DEMON™ software manual is currently offered as a separate manual.

SECTION 5

ROM RESIDENT SOFTWARE (OPTIONAL)

Resident software is available for your SUPER JOLT card in the form of two mask-programmed ready-only memories (ROMs).

ROM OPERATION INSTRUCTIONS

These two proprietary 2Kx8 mask ROMs (AM9216's) contain the 6502 Resident Assembler Program (RAP) and JOLT TINY BASIC. These ROMs are designed for immediate use on the CP110 SUPER JOLT Card.

Program Location:

TINY BASIC	C000 - C8FF
RAP	C900 - CFFF

Ram Requirements:

Both TINY BASIC and RAP assume RAM at page 0 and 1 (0000 - 01FF). Both programs will, upon execution, determine the extent of RAM memory, beginning at 0200 and continuing to write/read memory until the read fails, indicating the end of RAM memory. This RAM address space information is used by the programs as the total extent of RAM available.

Page 0 Vector Initialization:

Prior to running either TINY BASIC or RAP, two branch vectors must be entered at location 0000. Use DEMON™ to first desplay, then alter these locations as follows:

```
.M 0000 XX XX XX XX XX XX XX XX
.: 0000 4C E9 72 4C C6 72
```

The branch at 0000 (4CE972) is a JMP to the DEMON™ read character routine (RDT). The branch at 0003 (4CC672) is a JMP to the DEMON™ write character routine (WRT).

Start Addresses:

TINY BASIC	C000
RAP	C900

High Speed Paper Tape Input Option (TINY BASIC Only):

TINY BASIC may be made to run using the high speed paper tape input option. First use DEMON™ to initialize page 0 as follows:

```
.: 0000 4C 06 00 4C C6 72 A6 E8
.: 0008 86 E7 20 1D 73 4C E9 72
```

Use DEMON's™ "H" command, to set the high-speed reader mode. Then transfer control to TINY BASIC at C000. Input will be read in from the high speed reader

source, but will not be echoed on the printer device. Following completion of the read-in, if control is not returned to the terminal, restart BASIC at C003, (warm start) to preserve the data in memory.

Resident Assembler Test Program:

Users should note that the .ORG $1000 on the RAP test program should be changed to .ORG $200 for SUPER JOLT usage. This can be done dynamically by stopping the test run just prior to the read-in of the .ORG $1000, typing in the .ORG $200, skipping past the .ORG $1000 on the paper tape, and continuing.

JOLT TINY BASIC

The JOLT TINY BASIC interpretive program is a subset of Dartmouth BASIC that resides in 2,304 bytes of program memory. The language consists of 12 statements, four expressions and two machine language subroutine calls.

PRINT: print-list

This statement prints values of the expressions and/or the contents of the strings in the print-list. The items may be expressions or alphanumeric strings enclosed in quotation marks.

INPUT: input-list

This statement checks to see if the current line is exhausted. If it is, a question mark is prompted with an X-ON control character, and a new line is read in. Then or otherwise, the input list is scanned for an expression which is evaluated. The value thus derived is stored in the first variable in the input-list.

LET variable = expression:

This statement assigns the value of the expression to the variable. The long form of this statement executes slightly faster than the short form (variable = expression).

GOTO expression:

The GOTO statement premits changes in the sequence of program execution to the line number derived by the evaluation of the expression in the GOTO statement. This permits one to compute the line number of the next statement on the basis of program parameters during program execution.

GOSUB expression:

The GOSUB statement is like the GOTO statement, except that TINY BASIC remembers the line number of the GOSUB statement, so that the next occurrence of a RETURN statement will result in execution proceeding from the starement following the GOSUB. Subroutines called by GOSUB statements may be nested to any depth.

RETURN:

The RETURN statement transfers execution control to the line following the most recent unRETURNed GOSUB.

IF expression rel expression THEN statement:

The IF statement compares the expressions according to one of six relational operators. If the relationship is TRUE, the statement is executed; if FALSE, the associated statement is skipped. The six relational operators are:

"=","<",">","<=",">=","> <".

END:

The END statement must be the last executable statement to terminate a problem at any time or to clear out any saved GOSUB line numbers.

REM comments:

The REM statement permits comments to be interspersed in the program.

CLEAR:

The CLEAR statement formats the user program space, deleting any previous programs.

RUN:

The RUN statement is used to begin program execution at the first (lowest) line number.

LIST:

The LIST statement causes part or all of the user program to be listed. If no parameters are given, the whole program is listed.

EXPRESSIONS:

An expression is the combination of one or more numbers or variables joined by operators, and possibly grouped by parentheses. There are four operators:

+(add), - (sub), *(multiply), and /(divide).

RESIDENT ASSEMBLER PROGRAM

The JOLT Resident Assembler Program (RAP) is a 1.75K byte program designed for use on CP100 JOLT and CP110 SUPER JOLT systems equipped with at least 4K bytes of RAM memory. RAP processes source statements producing an output listing on teletype-like like devices. The assembly process is performed in one pass, reading source input, printing the listing and generation object code continuously until all processing is complete. Source input is accepted by the assembler either by directly typing input at the keyboard or by reading a previously prepared punched paper tape.

The assembler stores the generated object code directly into JOLT memory. There it can be executed immediately after assembly or punched out in hex format using

the DEMON™ monitor.

RAP is compatible with the MOS Technology Cross Assembler with the following exceptions:

- o Expressions and *(used for current program counter) are not allowed.
- o The OPT and PAGE pseudo operations are not implemented.
- o Octal and binary numbers are not implemented.
- o ORG is used instead of *= to origin program.
- o RES is used for reserving storage.

Input Line Format

Source input is free format where each statement can be composed of the following optional fields:

- o Label - If present, must begin in column one and be terminated by a space.
- o Operation - If present, must be preceded by a space and must be one of the MOS 65XX mnemonics defined in the RAP manual.
- o Operands - If present, must be preceded by a space and follow one of the forms found in the RAP manual.
- o Comments - if present, must have as its first character a semicolon (;) and if not in column one, must be preceded by a space.
- o Carriage return - All lines are terminated by a carriage return.
- o Expressions and * (used for current program counter) are not allowed.

A name is any alphanumeric symbol. Names are used as labels or in operand fields.

The first character of a name can be any assembler recognized name character or a letter. The second and following characters of a name can include numbers. A name is terminated by a blank or a carriage return. Names have no restrictions on length other than they must fit on one line.

Numbers are an unsigned string of hexaadecimal or decimal characters. Hexidecimal numbers are preceded by a $ and can contain the numbers 0 through 9 and the hex characters A through F. Decimal numbers contain only the decimal characters 0 through 9.

ASCII strings have two forms. The short form is used in conjunction with immediate operands and consists of a single quote followed by a single ASCII character. The long form is used to define large strings of ASCII data. This form is only valid in the BYTE Pseudo operation. Carriage returns are not allowed within the string.

All symbols that are intended to be used as an 8-bit immediate operand must be

defined (appear in a label field) before they are used. Sixteen bit operands and forward relative branches are inserted at the time of their definition by the assembler. This means that the value appearing in the assembly listing of previously undefined symbols is not the ultimate value used at the time the assembly is complete.

The assembler detects errors during the assembly process and outputs an appropriate error code after the printed hex output on the listing. Recognized errors include: Branch address out of range, undefined operation code, size of operand value exceed 8-bits, multiple appearances of the symbol in the label field, and improper format in the operand field. Additionally, the location field is offset in the table dump for undefined symbols.

The reverse-slash character may be used to delete the current source line during an assembly run. Reverse-slash is obtained by the Shift and L key combination. When used, the delete line causes the current line to be ignored and terminated, a carriage return will be effected and the assembler will position the carriage to accept the next line of source data.

The user may at any time, reorigin the assembler to correct areas of code already assembled. For example, if half way through an assembly, the user realized that an instruction was omitted, say five lines ahead of its current position, he may stop the assembler, reorigin back to the location at which the instruction should be inserted, insert the instruction and then repeat the assembly process from that point forward.

AM9216 ROM DESCRIPTION

Am9216

2048 x 8 Read Only Memory

DISTINCTIVE CHARACTERISTICS

- 2048 x 8 organization
- High speed – 300ns access time
- Fully capacitive inputs – simplified driving
- 2 fully programmable chip selects – increased flexibility
- Logic voltage levels compatible with TTL
- Three-state output buffers – simplified expansion
- Standard supply voltages – +12V, +5.0V
- No V_{BB} supply required
- N-channel silicon gate MOS technology
- 100% MIL-STD-883 reliability assurance testing

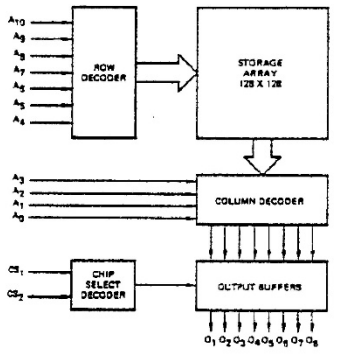
FUNCTIONAL DESCRIPTION

The Am9216 devices are high performance, 16384-bit, static, mask programmed, read only memories. Each memory is implemented as 2048 words by 8 bits per word. This organization simplifies the design of small memory systems and permits incremental memory sizes as small as 2048 words. The fast access times provided allow the ROM to service high performance microcomputer applications without stalling the processor.

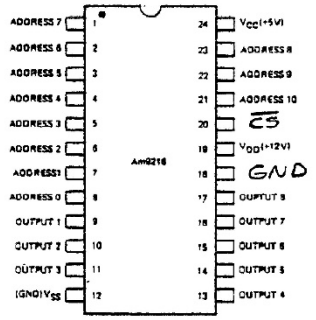
Two Chip Select input signals are logically ANDed together to provide control of the output buffers. Each Chip Select polarity may be specified by the customer thus allowing the addressing of 4 memory chips without external gating. The outputs of unselected chips are turned off and assume a high impedance state. This permits wire-ORing with additional Am9216 devices and other three-state components.

These memories are fully static and require no clock signals of any kind. A selected chip will output data from a location specified by whatever address is present on the address input lines. The Am9216 is pin compatible with the Am9208 which is an 8k-bit mask programmed ROM. Input and output voltage levels are compatible with TTL specifications.

BLOCK DIAGRAM



CONNECTION DIAGRAM
Top View



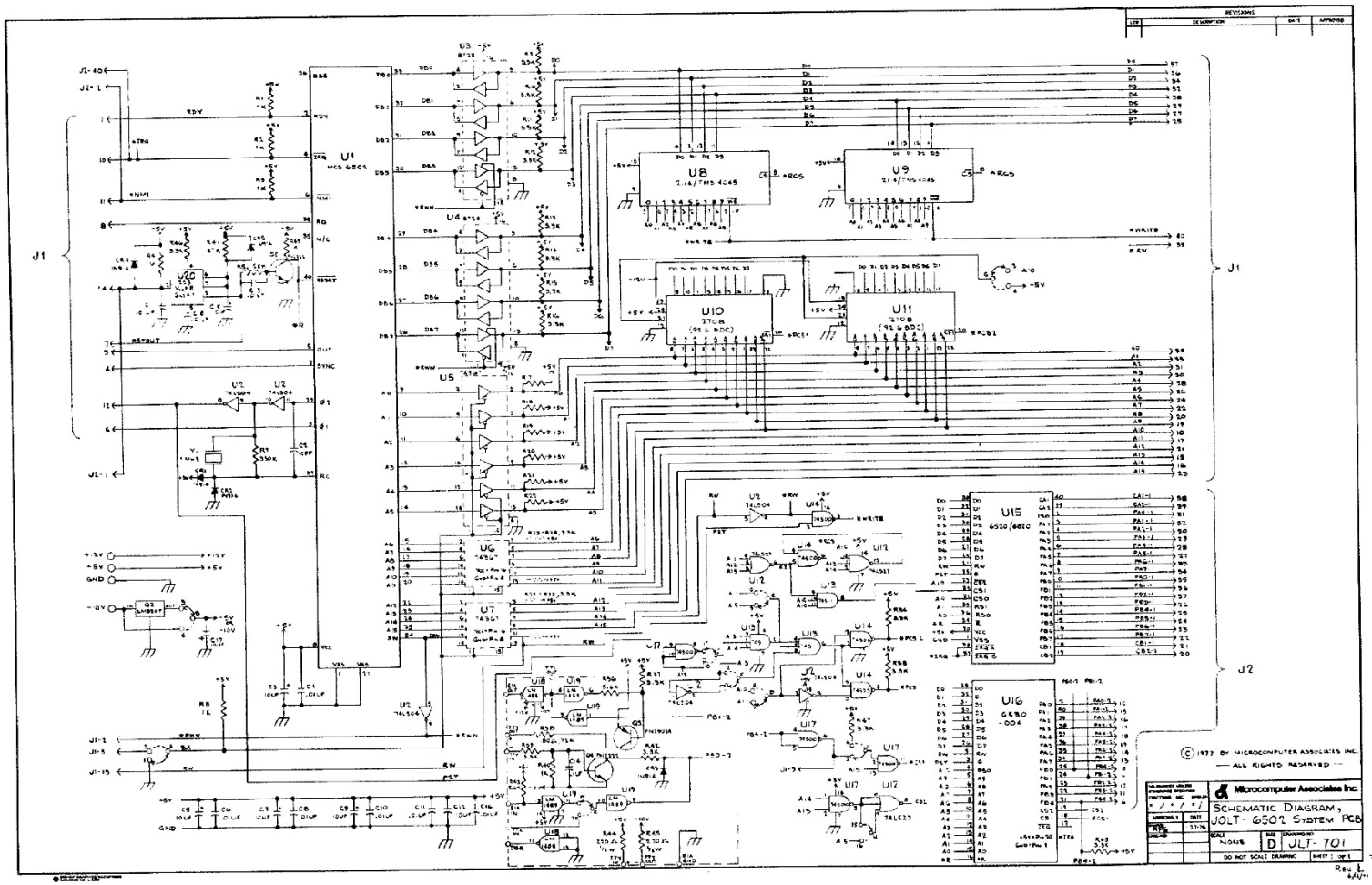
Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Ambient Temperature Specifications	Access Time	
		400ns	300ns
Hermetic DIP	$0°C \leq T_A \leq 70°C$	AM9216BDC	AM9216CDC
	$-55°C \leq T_A \leq 125°C$	AM9216BDM	

SECTION 6

SUPER JOLT SCHEMATIC & ASSEMBLY DRAWING


REVISIONS
LTR DESCRIPTION DATE APPROVED
U1 MCS 6501
U2 74LS04
U3 8T28
U4 8T26
U5 74S51
U6 74S04
U7 74S51
U8 2114/TMS 4045
U9 2114/TMS 4045
U10 2708 (9L & RDC)
U11 2708 (9L & RDC)
U15 6520/6820
U16 6530 -004
U17 74LS27
J1
J2
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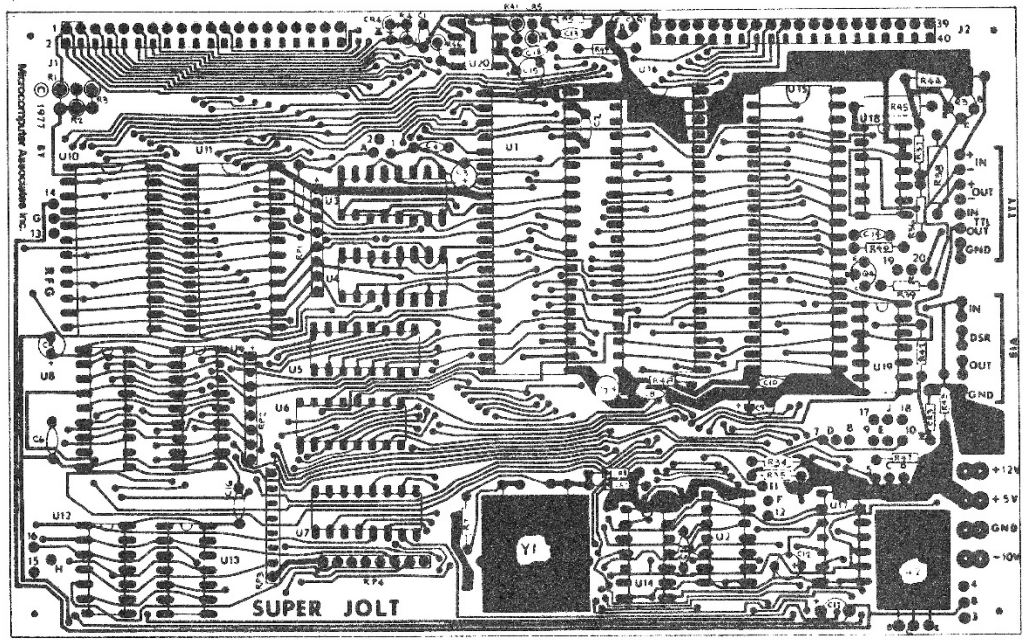
Microcomputer Associates Inc.
SCHEMATIC DIAGRAM, JOLT-6502 SYSTEM PCB
SIZE D
JLT-701
SCALE NONE
DO NOT SCALE DRAWING
SHEET 1 OF 1
REV L 6/4/77

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES		Microcomputer Associates Inc.	
		ASSEMBLY DRAWING, 6502 (SUPER JOLT) P.C. BD.	
APPROVALS	DATE		
DRAWN	1/29/76		
CHECKED		SCALE 2/1	SIZE C / DRAWING NO JLT-703
		DO NOT SCALE DRAWING	SHEET

Rev. L 6-14-77