McSHANE
INCORPORATED

7/76

You are probably aware of the fact that expansion memory will be available for your KIM-1 beginning August 16. This will be in the form of a KIM-2 (4K) at $179.00 or a KIM-3 (8K) at $298.00. We understand the KIM-2 and KIM-3 boards will be slightly smaller than the KIM-1 board. They will connect directly to the KIM-1 via ribbon cable.

If you intend to purchase one of these boards we would very much appreciate your order being placed with McShane. We have ordered a large quantity therefore delivery should be faster from us. If you intent to order later, please drop us a note or a card so that we can be sure the board is available when you are ready.

These boards will move fast and we would like to plan ahead.

P.S. The KIM-4 mother board will be available in September allowing you to add additional memory boards up to 64K on one mother board.

Also - software for the KIM-1 is becoming available through a "KIM-1 Users Club" now being formed. The initial offering is a subscription of 6 issues for $5.00. You may order subscriptions with McShane.

Phil Johnson

P. O. BOX 523 MEDINA, OHIO 44256 TELEPHONE (216) 725-4568

McSHANE
INCORPORATED

KIM-1 ASSEMBLER/EDITOR

The DATA-1K ASSEMBLER/EDITOR is a software resident assembler for the MOS TECHNOLOGY MCS 6500 SERIES microprocessor family using a KIM-1 with expansion memory. 4K of memory is used to store the assembler/editor program which is available in paper tape (or cassette on request).

8K of memory is recommended to allow space for the users source file and finished program. The price of $250.00 includes a one year warranty plus updates and maintenance for one year.

Delivery is from stock.

Please make out purchase orders to:

McShane, Inc.
P. O. Box 523
Medina, Ohio 44256

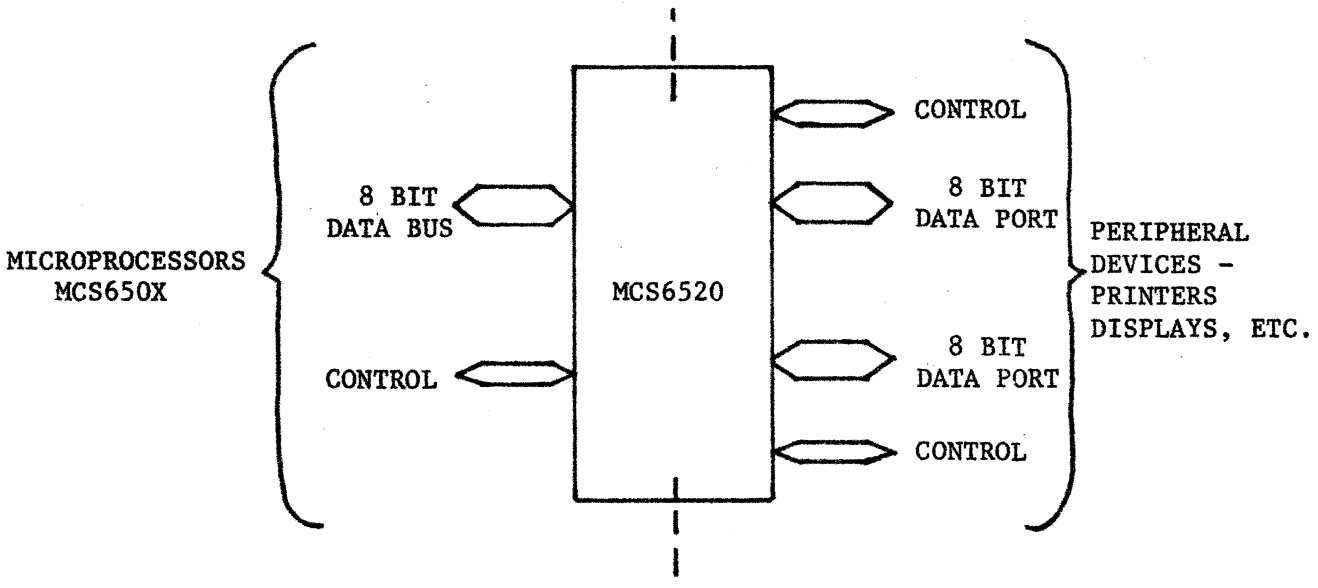
McSHANE INCORPORATED

MCS6520 PERIPHERAL INTERFACE DEVICE

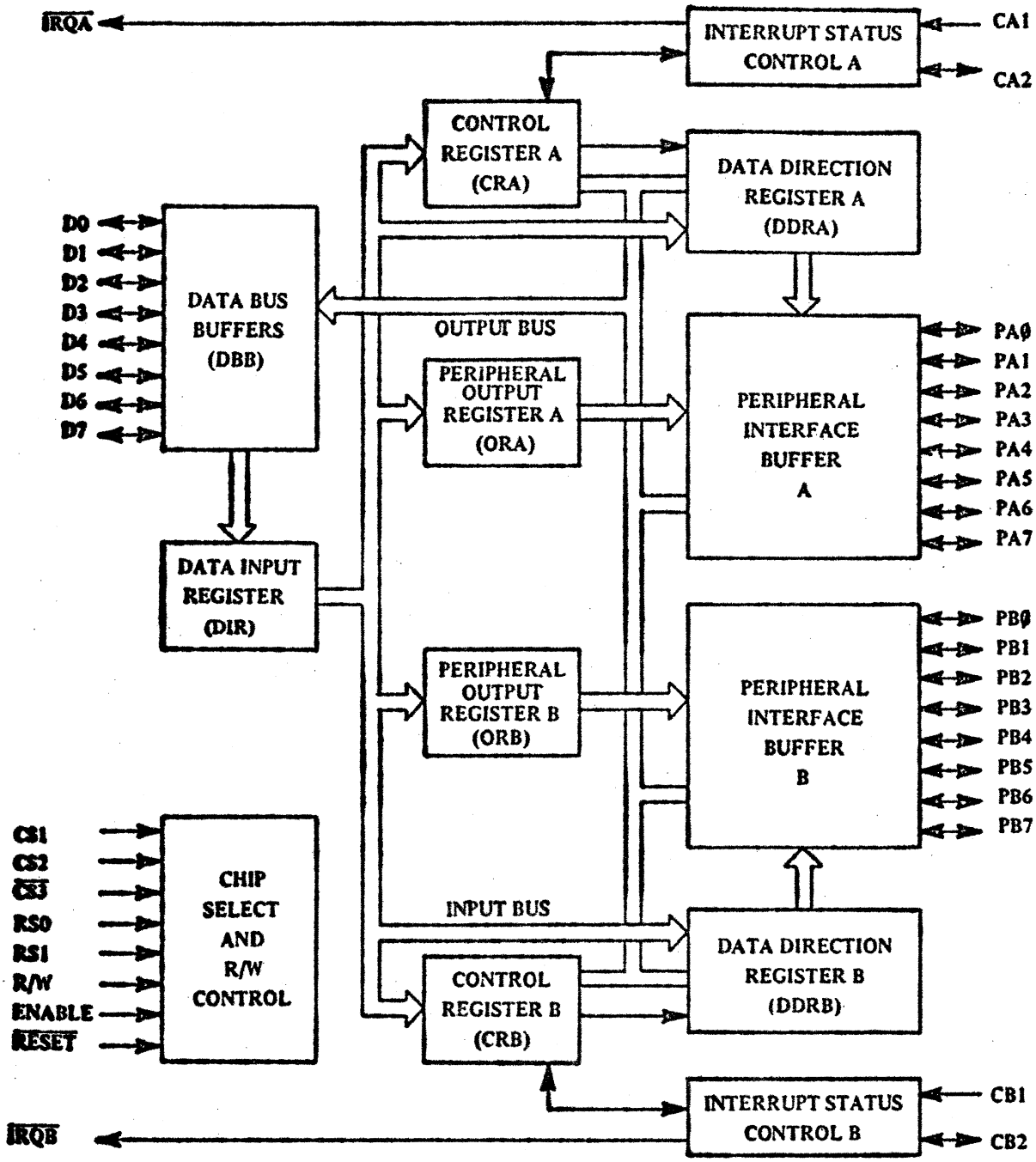
The functional configuration of the MCS6520 is programmed by the microprocessor during systems initialization. Each of the peripheral data lines is programmed to act as an input or output and each of the four control/interrupt lines may be programmed for one of four possible control modes. This allows a high degree of flexibility in the overall operation of the interface.

Some of the more important features of the MCS6520 are the following:

* Compatibility with the MCS650X microprocessors.
* Eight-bit bi-directional data bus for communication with the microprocessor.
* Two eight-bit bi-directional ports for interface to peripherals.
* Two programmable control registers.
* Two programmable Data Direction Registers.
* Four individual controlled interrupt input lines - two usable as peripheral control outputs.
* Handshake control logic for input and output peripheral operation.
* Direct transistor drive peripheral lines.
* Program controlled interrupt and interrupt mask capability.



Basic MCS6520 Interface Diagram



MCS6520 Internal Architecture

PRELIMINARY

INFORMATION

SHEET

MCS6522

McSHANE INCORPORATED

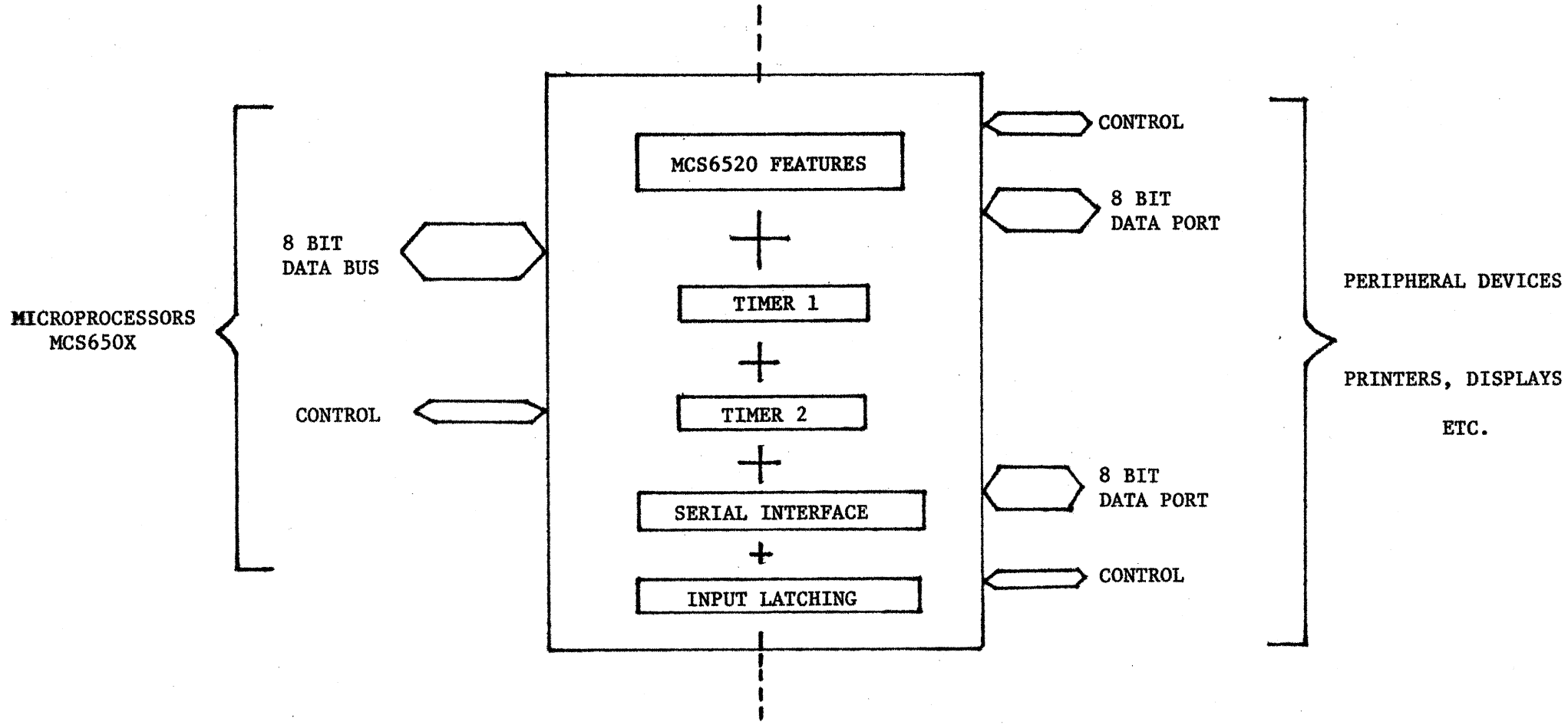
MCS6522 VERSATILE INTERFACE DEVICE

(SAME FEATURES AS THE MCS6520 WITH TIMERS, LATCHING AND SHIFT REGISTER ADDED)

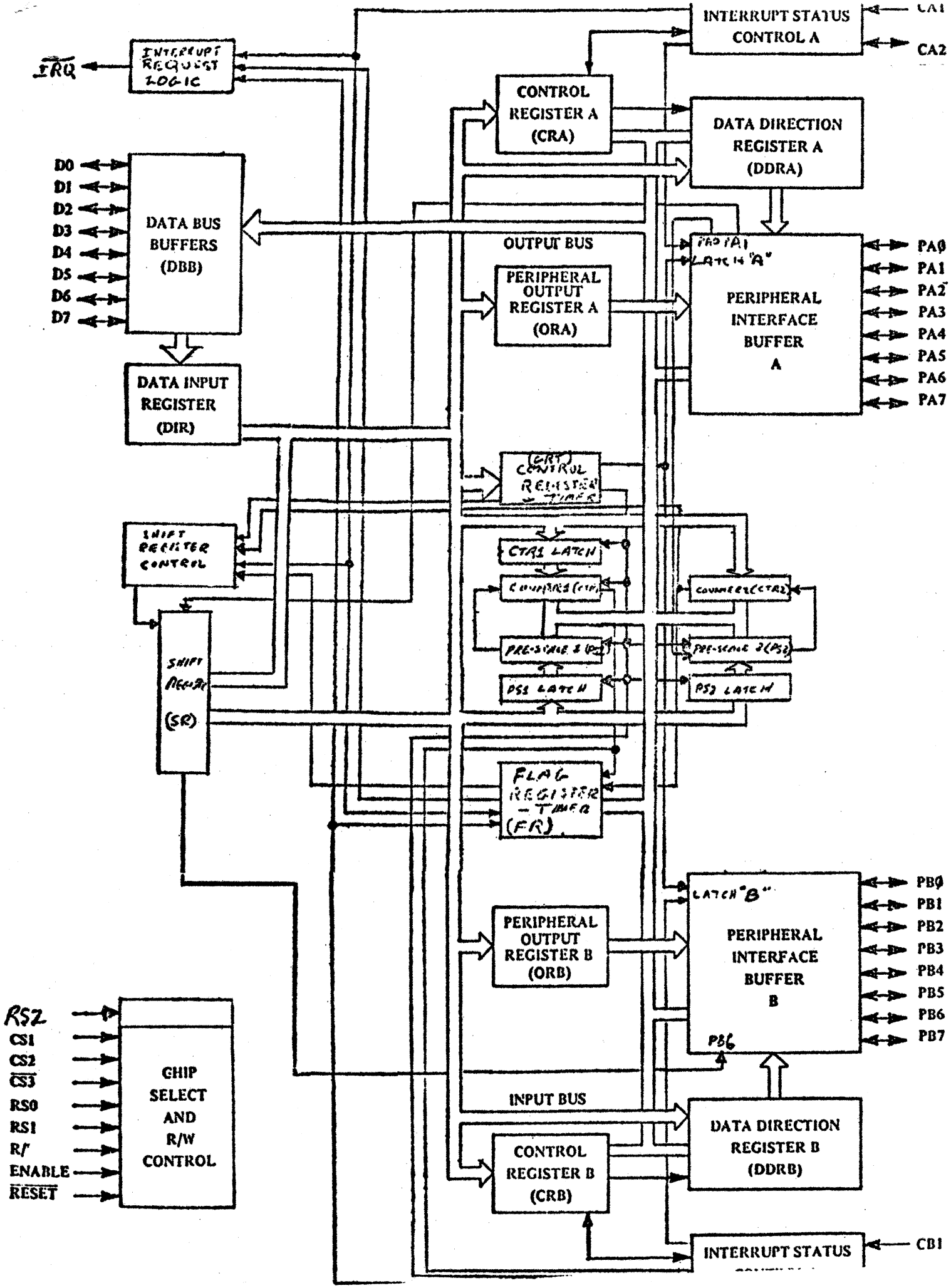
The functional configuration of the MCS6522 is programmed by the microprocessor during systems initialization. Each of the peripheral data lines is programmed to act as an input or output and each of the four control/interrupt lines may be programmed for one of four possible control modes. This allows a high degree of flexibility in the overall operation of the interface.

Some of the more important features of the MCS6522 are the following:

* Total Electrical Compatibility with the MCS6500 Bus Structure;
* Compatibility with the MCS650X microprocessors;
* Eight-bit bi-directional data bus for communication with the microprocessor;
* Two eight-bit bi-directional ports for interface to peripherals;
* Two programmable control registers;
* Two programmable Data Direction Registers;
* Four individual controlled interrupt input lines - two usable as peripheral control outputs.
* Handshake control logic for input and output peripheral operation;
* Direct transistor drive peripheral lines;
* CMOS compatible - "A" and "B" side outputs;
* Program controlled interrupt and interrupt mask capability;
* Data Latching on peripheral ports;
* Two fully programmable timers with latches;
* One timer/shift register control register;
* One parallel to serial/serial to parallel 8 bit shift register for serial interface, with programmable shift rate capability;
* Interrupt detection capability;
* Address and R/W latched. Allows addresses and R/W to change during Ø2.



BASIC MCS6522 INTERFACE DIAGRAM


IRQ
INTERRUPT REQUEST LOGIC
INTERRUPT STATUS CONTROL A
CA1
CA2
CONTROL REGISTER A (CRA)
DATA DIRECTION REGISTER A (DDRA)
D0
D1
D2
D3
D4
D5
D6
D7
DATA BUS BUFFERS (DBB)
OUTPUT BUS
PERIPHERAL OUTPUT REGISTER A (ORA)
PERIPHERAL INTERFACE BUFFER A
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
DATA INPUT REGISTER (DIR)
CONTROL REGISTER - TIMER
SHIFT REGISTER CONTROL
CTR1 LATCH
PRE-SCALE 2 (PS2)
PS1 LATCH
PS2 LATCH
SHIFT REGISTER (SR)
FLAG REGISTER - TIMER (FR)
LATCH "B"
PERIPHERAL OUTPUT REGISTER B (ORB)
PERIPHERAL INTERFACE BUFFER B
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
INPUT BUS
DATA DIRECTION REGISTER B (DDRB)
RS2
CS1
CS2
CS3
RS0
RS1
R/W
ENABLE
RESET
CHIP SELECT AND R/W CONTROL
CONTROL REGISTER B (CRB)
INTERRUPT STATUS
CB1

JOHNSON COMPUTER

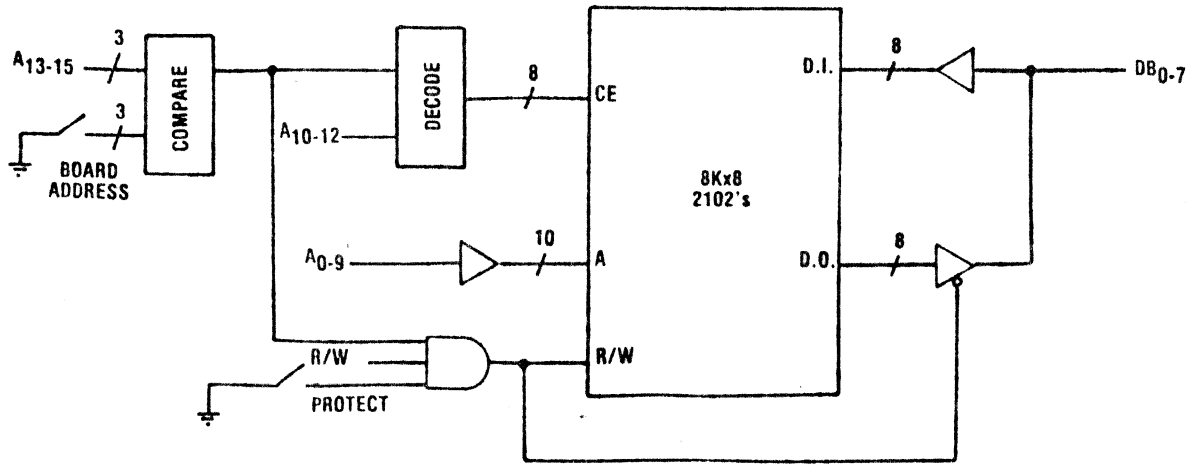
P. O. BOX 523 MEDINA, OHIO 44256

PH: 216/725-4560

KM8B

8K KIM STATIC RAM

ADDRESSING: Selectable in any 8K boundary.
BUFFERING: Data and Address lines fully buffered.
INTERFACE: With KIM-1, which allows for a bussed system.
P.C. BOARD: Hi-grade glass epoxy with plated-thru holes.
SOLDER MASK: Gold plating over nickel contact fingers for long term reliability.
MEMORY PROTECT: Writing may be inhibited for the entire board by activating a DIP switch.
MEMORY I.C.'S: 2102 1K x 1 Static RAM's. Low power.
SUPPORT CHIPS: Low power schottky (where applicable).
SOCKETS: All I.C.'s mounted in low profile sockets.
POWER: Power may be supplied from unregulated 8V to an on board regulator or directly from a 5V external power supply.
TESTING: Factory tested and burned-in.
KIM-4 COMPATIBLE: May be directly plugged into the KIM-4 mother board.



PRELIMINARY

INFORMATION

SHEET

MCS6532

McSHANE INCORPORATED

MCS6532 (MEMORY, I/O, TIMER ARRAY)

The MCS6532 is designed to operate in conjunction with the MCS650X Microprocessor Family. It is comprised of a 128 x 8 static RAM, two software controlled 8 bit bi-directional data ports allowing direct interfacing between the microprocessor unit and peripheral devices, and a software programmable interval timer with interrupt, capable of timing in various intervals from 1 to 262,144 clock periods, and a programmable edge detect circuit.

* 8 bit bi-directional Data Bus for direct communication with the microprocessor;
* Edge Sense Interrupt (Positive or Negative Edge; Programmable);
* 128 x 8 static RAM;
* Two 8 bit bi-directional data ports for interface to peripherals;
* Two programmable I/O Peripheral Data Direction Registers;
* Programmable Interval Timer;
* Programmable Interval Timer Interrupt;
* TTL & CMOS compatible peripheral lines;
* Peripheral pins with Direct Transistor Drive Capability;
* High Impedence Three-State Data Pins

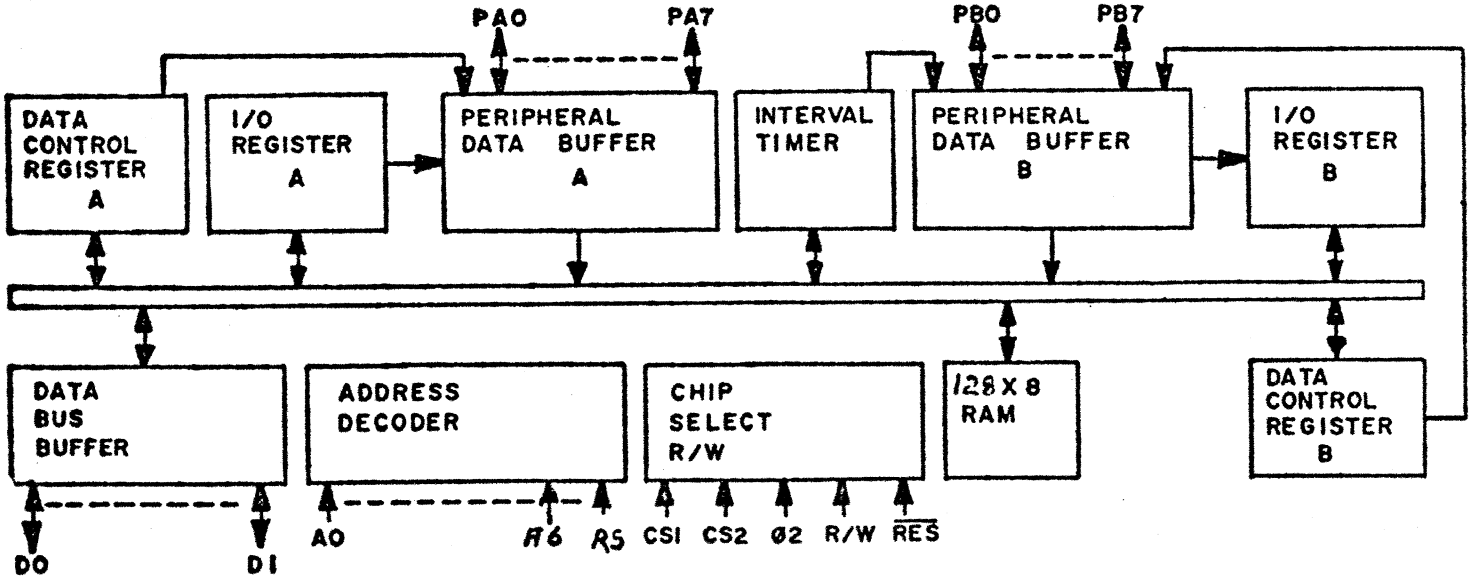


Figure 1, MCS6532 Block Diagram