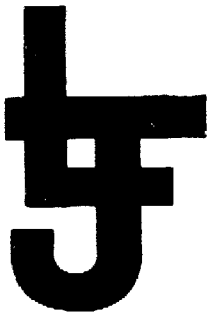


L.J. ELECTRONICS

'EMMA' HARDWARE MANUAL

.... Electronics Limited,
.. Francis Way,
Enterprise Industrial Estate,
Norwich.
NR6 5.J

C O N T E N T S

NOTE:- EMMA's delivered after 1st January, 1982 have the 512-byte monitor in EPROM. The information given in Chapter 4 refers to the PROMs used prior to 1982. With an EPROM providing the monitor, the information given in Chapter 5 also refers to the monitor EPROM.

CHAPTER 1

INTRODUCTION TO THE 'EMMA' SYSTEM

The 'Emma' microcomputer is based on the 6502 microprocessor. To form a computing system, the 6502 will need additional memory locations. On the 'Emma' board, these locations are provided by the devices identified in figure 1.1.:-

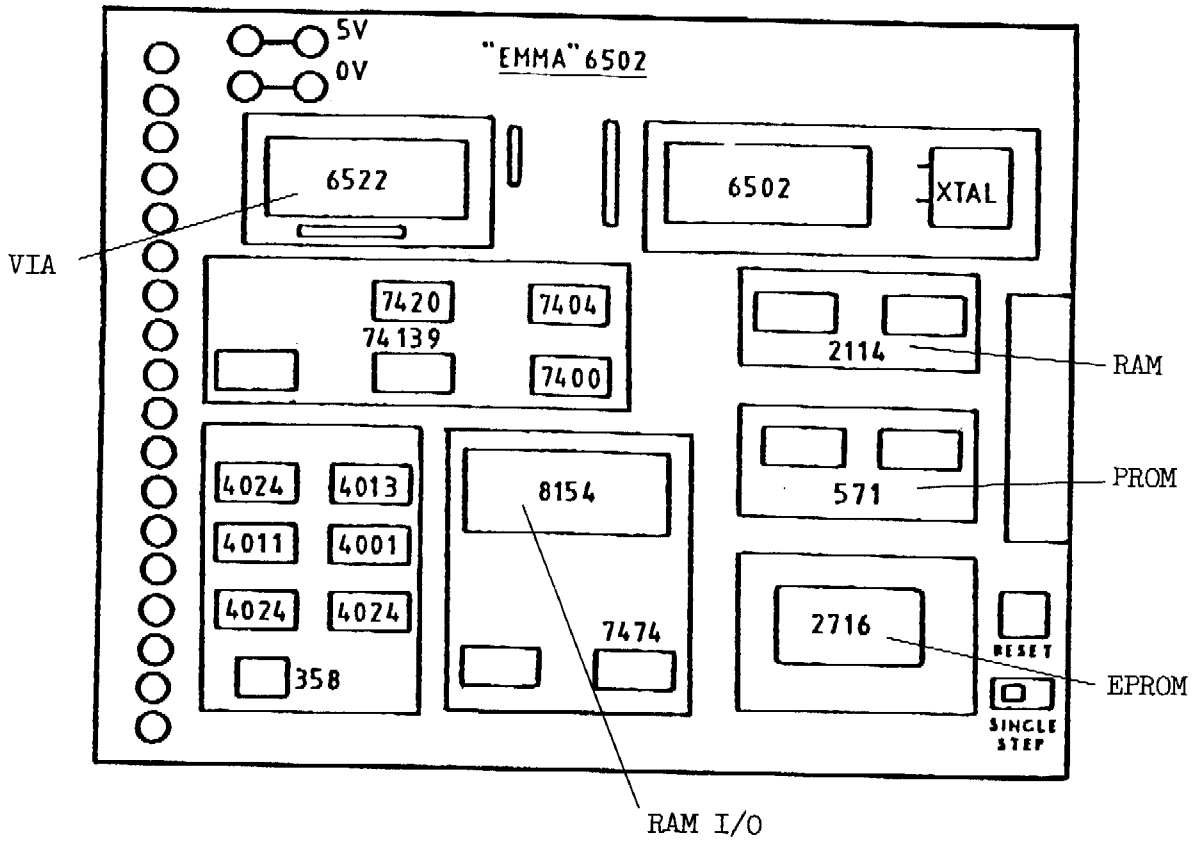


Fig 1.1

6502 Microprocessor: - a 40-pin i.c., requiring an external crystal to determine its operating speed. The 'Emma' uses a 1 MHz crystal, giving a basic microprocessor cycle time of 1μs

Random Access Memory (RAM): - 1024 bytes of memory are provided by 2 x 2114 i.c.s.

Read Only Memory (ROM): - 512 bytes of read only memory are provided by 2 x 745571 fusible link programmable read-only memories. These i.c.s are programmed to provide the system monitor routines.

Erasable Programmable Read Only Memory (EPROM): - An expansion socket provides for one 2716 u/v erasable PROM. The 2716 is a 2048 byte memory.

Keyboard/Display Interface: - An 8154 i.c. provides 16 latch circuits which appear as two 8-bit memory locations to the microprocessor. These latches provide two programmable input/output ports. 14 bits of the ports are used for the keyboard/display unit which plugs into a 16-pin i.c. socket. The remaining 2-bits of I/O port are used for serial data input and output through the cassette interface.

The 8154 also provides 128-bytes of RAM.

Located next to the 8154 is a 7474 bistable i.c. which provides the signals required to interrupt the microprocessor for single-step operation.

Input/Output Port - Timer: - A 6522 versatile interface adapter is the buffer between the user ports, PA_0-PA_7 and PB_0-PB_7, and the microprocessor. These two ports are seen as memory locations by the 6502, each bit of both ports being programmable as input or output. The 6522 also provides two programmable timers and a serial input/output mode.

Address Decoding: - The address bus lines, A_7-A_{15}, are partially decoded, to provide the chip select signals for all the 'Emma' board memory. Further system expansion will require additional address decoding.

Cassette Interface: - The 'Emma' provides a two-way interface for the recording and reading of programs on an unmodified commercial cassette tape recorder. This interface converts output level '1' signals into a tone of

2.4 kHz approximately, and level '0' signals into a tone of 1.2 kHz approximately. The interface also converts these playback tones into the respective '1' and '0' levels.

Expansion Connector: - The 6502 bus lines and control signals are made accessible via a 34-way expansion connector. This is, primarily, provided for future system expansion, but it does also facilitate monitoring of system signals.

Additional 0.1" p.c.b connectors provided around the 'Emma' board enable rapid access to control and bus signals as may be required for oscilloscope and logic analyser monitoring.

CHAPTER 2

THE 6502 MICROPROCESSOR

The 6502 is a 40-pin integrated circuit, the pin connections being as shown in figure 2.1:-

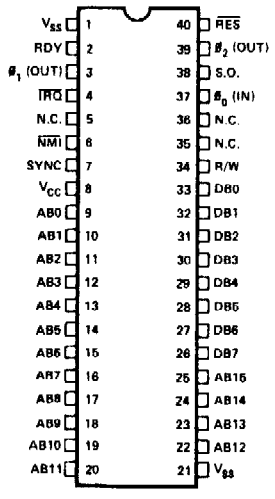


Fig. 2.1

CLOCK (ϕ_0, ϕ_1, ϕ_2):

The 6502 clock circuits can be driven from a single TTL level square wave, or with the internal oscillator. The 'Emma' uses a 1 MHz crystal to control the internal oscillator, giving a stable 1μs cycle time.

ADDRESS BUS (A_0-A_{15}):

The 16-bit address bus is used to transfer the address generated by the processor to the address inputs of all memory and peripheral interface devices. The address is always provided by the 6502, thus the address bus is unidirectional. The bus lines are TTL compatible, capable of driving one standard TTL load and 130 pF.

DATA BUS (DB_0-DB_7):

The 8-bit data bus is bi-directional, providing a two-way transfer path between the microprocessor and the memory and interface circuits. The data bus is tri-state and is capable of driving one standard TTL load and 130 pF.

READY (RDY):

This input signal is provided to allow the user to halt the 6502 on all cycles except write cycles. This feature is of use when low speed PROMS are used, or when fast direct memory access (DMA) transfers are to be performed. The ready signal is disabled (held high), on the 'Emma' board.

INTERRUPT REQUEST ($\overline{IRQ}$):

When this input is in the low state (logic '0'), the microprocessor is requested to begin an interrupt sequence. The microprocessor will not acknowledge this request until it has completed the current instruction being executed. Then, provided the interrupt mask bit (interrupt disable, within the status register), is not set, the microprocessor will begin an interrupt sequence.

The interrupt sequence is:-

(i) store Program Counter high byte (PCH) on the stack,
(ii) store Program Counter low byte (PCL) on the stack,
(iii) store status register contents on the stack,
(iv) load PCL from address FFFE,
(v) load PCH from address FFFF,
(vi) normal program execution sequences now continue from the memory vector held at FFFF and FFFE.

On the 'Emma' board, the $\overline{IRQ}$ input is returned to +5V. through a 4.7 kΩ resistor to facilitate wired - OR operation.

NON-MASKABLE INTERRUPT ($\overline{NMI}$):

A negative going transition on this input requests that a non-maskable interrupt sequence is begun by the microprocessor. This interrupt is not conditional and will always be actioned following completion of

the current instruction. The sequence of steps for a $\overline{NMI}$ is the same as for $\overline{IRQ}$, except that the vector address will be loaded to PCL and PCH from locations FFFA and FFFB respectively.

The 6502 has an internal latch which is set by a '1' to '0' transition on the $\overline{NMI}$ input. Thus a single, short duration, negative going pulse may be used to provide an $\overline{NMI}$, unlike $\overline{IRQ}$, which has no latch and requires $\overline{IRQ}$ to remain low until the interrupt is actioned. $\overline{NMI}$ will take priority over $\overline{IRQ}$.

Wired - OR inputs to the $\overline{NMI}$ are facilitated by a 4.7 kΩ resistor returned to +5V.

SET OVERFLOW FLAG (S.O.):

A negative going edge on this input sets the overflow flag within the status register. This facility is not required for any of the current 6500 family circuits and the S.O. input is returned to +5V. on the 'Emma' board.

SYNC:

This output line identifies those cycles in which the microprocessor is doing a fetch instruction operation. The SYNC line goes high during ϕ_1 of a fetch operation and stays high for the remainder of that cycle.

The SYNC signal is used on the 'Emma' board for the generation of an interrupt signal required for single step operation. To avoid a timing hazard with the PROM chip select signal, the SYNC pulses are stretched by a CR circuit giving exponential rising and falling edges on the observed pulses.

RESET ($\overline{RES}$):

This input is used to reset or start the microprocessor from a power down condition. During the time that this line is held low, writing to or from the microprocessor is inhibited. When a positive edge occurs on the input the microprocessor will immediately begin the reset sequence.

Reset (continued)

After a system initialisation time of six clock cycles, the mask interrupt flag will be set and the microprocessor will load the program counter from the memory vector locations FFFC and FFFD. This is the start location for program control (FEF3 in the 'Emma' monitor).

On the 'Emma' board, $\overline{RES}$ is held high through a 4.7 kΩ resistor, it is pulled low when the push-button reset switch is depressed.

READ/WRITE (R/$\overline{W}$):

This output signal is used to control the direction of data transfers between the processor and other memory circuits on the data bus. R/$\overline{W}$ high signifies data transfer into the 6502, R/$\overline{W}$ low signifies data transfer out of the 6502.

SUPPLY VOLTAGES:

The 'Emma' requires a 5v. regulated supply, able to provide 700 mA approximately. The 6502 has a maximum V_{cc} rating of +7V.

It is strongly recommended that a fixed 5v. d.c. supply should be used for the 'Emma'. Some variable supplies generate a short duration positive going spike when switched on, which may damage circuits in the 6500 family.

Full manufacturers characteristics and specifications are given in Appendix A.

CHAPTER 3

RANDOM ACCESS MEMORY

The 'Emma' has 1024 bytes of random access memory, RAM, provided by two 2114, 1024 x 4 bit static RAM integrated circuits.

The 2114 is a MOS RAM, fabricated using N-channel silicon-gate technology. All internal circuits are fully static and therefore require no clocks or refreshing for operation. The data is read out non-destructively and has the same polarity as the input data. Common input/output pins are provided, with tri-state capability for direct bus interface.

Connections for the 18-pin RAM i.c. are given in the figure 3.1.

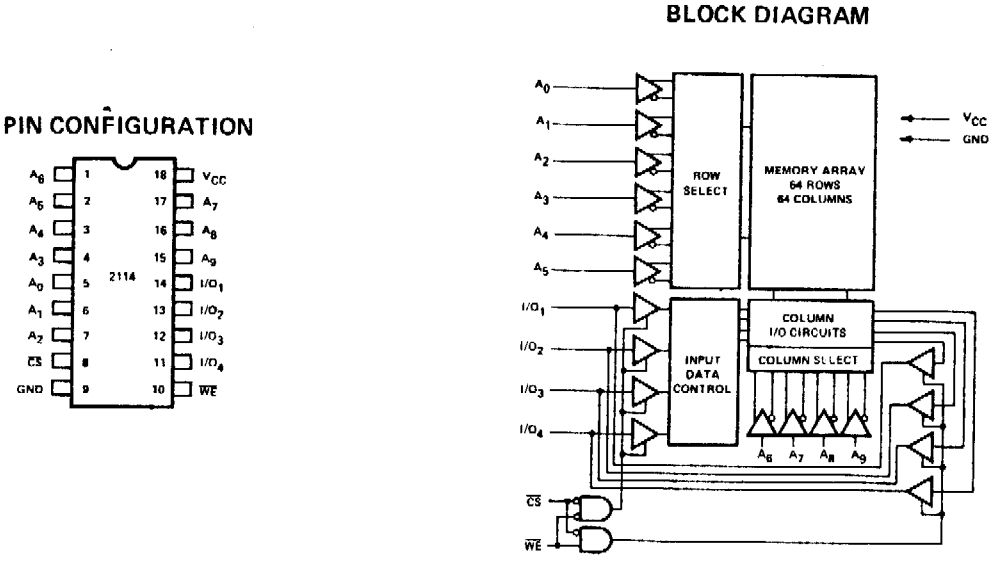


Fig 3.1

Any 1 of the 1024 locations is selected by the address code on the ten address input lines, A_0-A_9, provided that the chip select signal, $\overline{CS}$, is low. With $\overline{CS}$ high, the input/output pins are in their high impedance, tri-state, condition. In the 'Emma' system, the decoding logic provides RAM $\overline{CS}$ low when address lines A_{10}-A_{15} are low, placing the RAM at hexadecimal addresses; 0000 to 03FF.

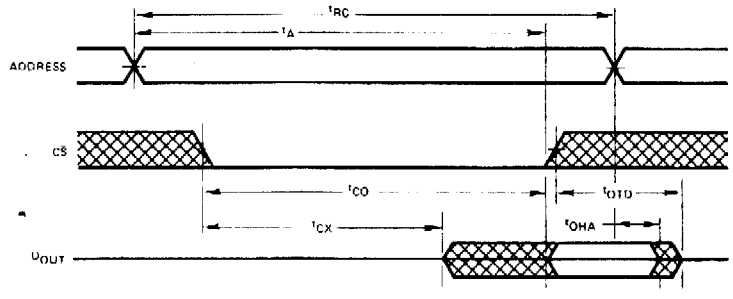
The requirements of the write enable signal, $\overline{WE}$, are not totally compatible with the microprocessor R/$\bar{W}$ signal. The RAM uses the not write data strobe, NWDS, for $\overline{WE}$. The NWDS is formed by gating the 6502 R/$\bar{W}$ signal with the $\emptyset_2$ clock, as described in chapter 7.

The 2114 memories used have a maximum access time, for read or write, of 450 µs.

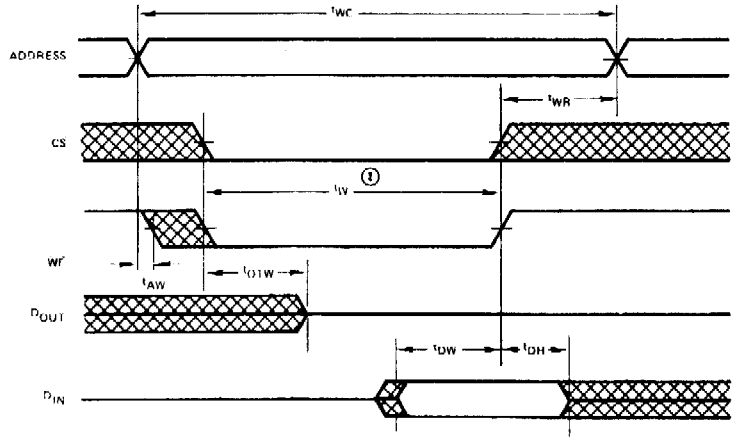
Manufacturers ratings and device timing waveforms are given in figures 3.2 and 3.3 respectively.

TIMING DIAGRAMS

Read Cycle ①



Write Cycle



NOTES:

① $\overline{WE}$ is high for a Read Cycle

② t_W is measured from the latter of $\overline{CS}$ or $\overline{WE}$ going low to the earlier of $\overline{CS}$ or $\overline{WE}$ going high.

Fig 3.3

CHAPTER 4

PROGRAMMED READ ONLY MEMORY

The 'Emma' has 512 bytes of programmed read only memory, PROM, provided by two 74S571, 512 x 4 bipolar PROM integrated circuits.

Connections for the 16-pin PROM i.c. are given in figure 4.1.

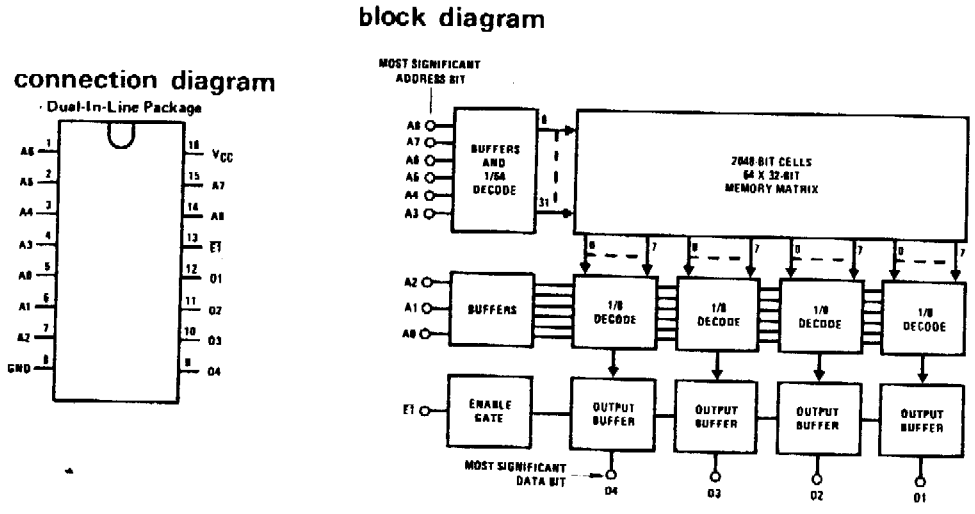


Fig. 4.1

Any of 512 locations is selected by the code on the nine address input lines, A_0-A_8, provided that the chip select signal, $\overline{ET}$, is low. The output pins are tri-state and with $\overline{ET}$ high these outputs are in their high impedance condition.

These programmable ROMS are received from the manufacturer with low outputs in all locations. Internal titanium-tungsten fuses are blown at our factory to provide the coding for the 'Emma' monitor.

Address lines A_{11}-A_{15} are decoded to provide PROM enable, $\overline{ET}$, low at addresses F800 to FFFF. Thus, the 512-byte monitor is located at FE00-FFFF, with the same data repeated at locationa; F800-F9FF, FA00-FBFF, FC00-FDFF. The reason for providing a 2K decoded block is so that the EPROM could be selected at addresses F800-FFFF, thus enabling an expanded monitor to be provided.

Manufacturers characteristics and device timing waveforms are given in figures 4.2 and 4.3 respectively.

Note: The detail given in this chapter refers to the National Semiconductor 74S571 PROM. A number of pin compatible PROMS are available from different manufacturers and we may provide alternative devices on the 'Emma' board.

PROM alternatives include:-

Fairchild,	93446
Harris,	HMI-7621
Intel,	3622
Intersil,	IM 5624
Signatics,	82S131

All these devices have similar electrical performances, but slight differences in programming procedures occur.

Please note that the fusible link PROMS will run warm when operating normally and they will feel considerably warmer than any other integrated circuits on the 'Emma' board.

CHAPTER 5

ERASABLE PROGRAMMABLE READ ONLY MEMORY

A socket is provided on the 'Emma' for a 2K byte 2716 EPROM. This 16,384 - bit electrically programmable, ultra-violet erasable read-only memory, is organised as 2048 eight bit words.

The 2716 requires only a single 5V power supply with a current requirement of approximately 100 mA. Pin connections for the 2716 are given in figure 5.1:-

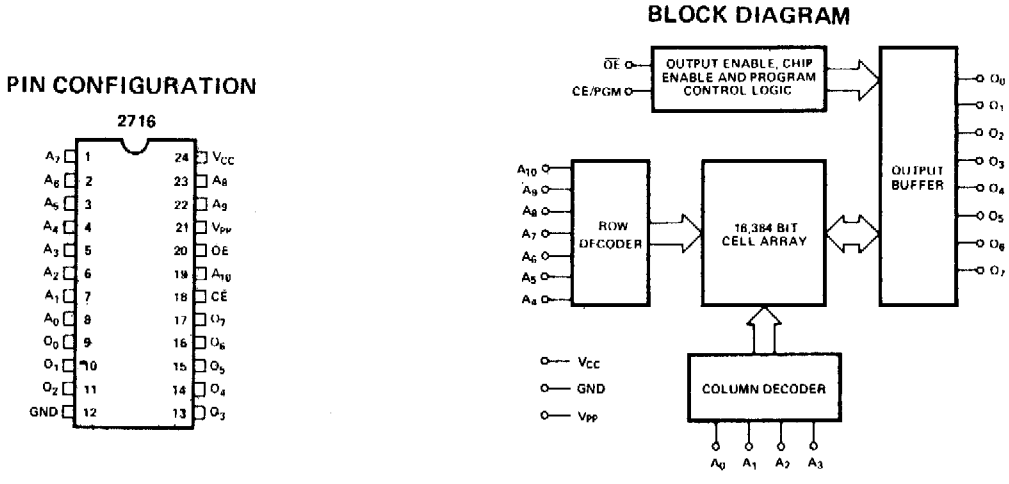


Figure 5.1

The 2048 locations are accessed by an address placed on the eleven lines, A_0 - A_{10}. Data from the accessed location is output on the eight data lines, O_0 - O_7, if the two control signals, $\overline{OE}$ and $\overline{CE}$ are low. Both $\overline{OE}$ and $\overline{CE}$ are high during programming. The decoding on the 'Emma' places the Eprom at address F000 to F7FF

EPROM erasure:-

Erasure of the 2716 begins to occur when exposed to light with wavelengths shorter than 4,000 angstroms. Certain types of light contain wavelengths in this range. Although exposure to sunlight or fluorescent light for a relatively long time is required to cause erasure, it is advised to avoid exposure to light for extended periods.

If operated whilst exposed to ambient light, the minute photo-electric currents generated may cause the EPROM to malfunction. Covering the EPROM 'window' with some opaque material is strongly advised.

Deliberate erasure of the 2716 is accomplished by exposing the device to ultra violet light with a wavelength of 2,537 angstroms. A 12 mW/cm^2 u-v lamp placed one inch from the 2716 will require approximately 20 minutes for complete erasure. Over-erasure is not thought by EPROM manufacturers to be a problem, but it is advised that erasure times greater than 10 times the necessary period should be avoided. Under-erasure will result in programming errors. When erased all bits are in the '1' state.

EPROM programming:-

Unprogrammed EPROMs will have all locations in the logic '1' state. Logic '0's are programmed electrically, logic '1's are obtained by u-v erasure. Programming is accomplished by applying a 50m sec TTL pulse to the $\overline{CE}$ / PGM pin, with 25V $\pm$ IV applied to Vpp and a TTL logic '1' applied to the $\overline{OE}$ input. The specific word to be programmed is selected with the address inputs, and the data to be programmed is applied to the data output pins.

Manufacturers characterisitics and timing waveforms, for the 2716 are given in figures 5.2 and 5.3 respectively.

CHAPTER 6

6522, VERSATILE INTERFACE ADAPTER

The 6522 provides:-

(a) two 8-bit programmable input/output ports.
(b) two 16-bit programmable timer/counters.
(c) one 8-bit serial transfer register.

The 6522 block diagram is shown in figure 6.1.

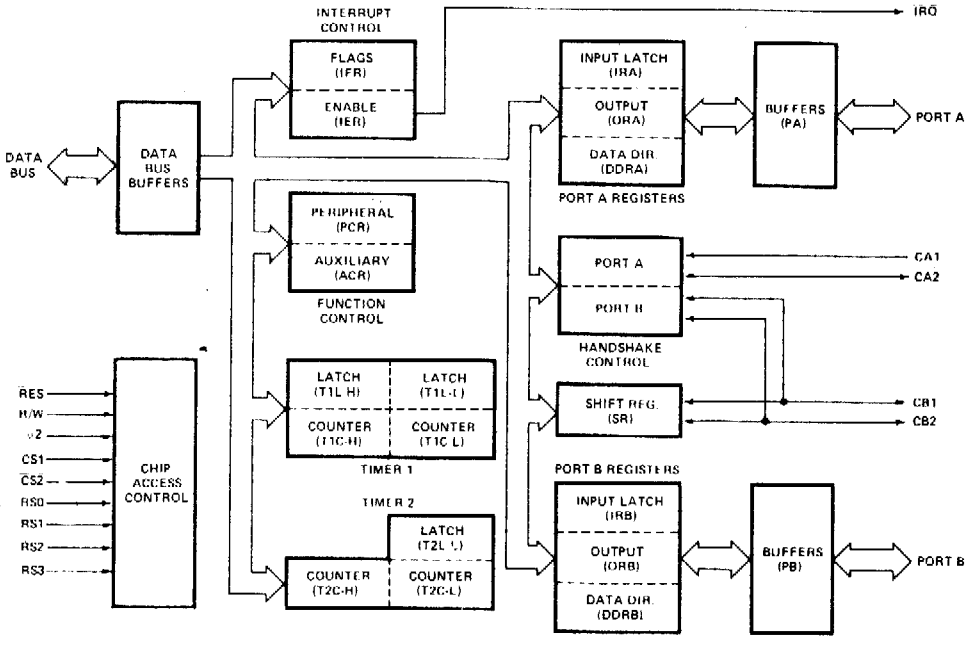


Figure 6.1

6522 pin configuration is shown in figure 6.2:-

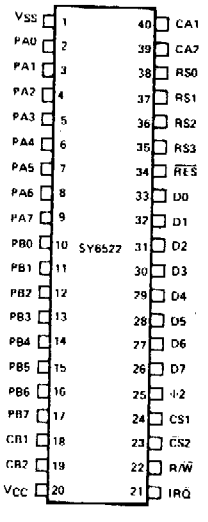


Figure 6.2

Pin functions:-

$\overline{RES}$ (Reset)

The reset input clears all internal registers to logic 0 (except T1 and T2 latches and counters and the Shift Register). This places all peripheral interface lines in the input state, disables the timers, shift register, etc., and disables interrupting from the chip.

Ø2 (Input Clock)

The input clock is the system Ø2 clock and is used to trigger all data transfers between the system processor and the 6522.

R/$\bar{W}$ (Read/Write)

The direction of the data transfers between the 6522 and the system processor is controlled by the R/$\bar{W}$ line. If R/W is low, data will be transferred out of the processor into the selected 6522 register (write operation). If R/W is high and the chip is selected, data will be transferred out of the 6522 (read operation).

DB0-DB7 (Data Bus)

The eight bi-directional data bus lines are used to transfer data between the 6522 and the system processor. During read cycles, the contents of the selected 6522 register are placed on the data bus lines and transferred into the processor. During write cycles, these lines are high-impedance inputs and data is transferred from the processor into the selected register. When the 6522 is unselected, the data bus lines are high-impedance.

CS1, $\overline{CS2}$ (Chip Selects)

The two chip select inputs are normally connected to processor address lines either directly or through decoding. The selected 6522 register will be accessed when CS1 is high and $\overline{CS2}$ is low.

On the 'Emma' board, the address decoding provides $\overline{CS2}$ low when memory pages 08 to 0B are selected. CS1 is connected to address line A_8, thus the 6522 can be accessed on page 09 or page 0B.

RS0-RS3 (Register Selects)

The four Register Select inputs permit the system processor to select one of the 16 internal registers of the 6522.

The 'Emma' board has the register lines RS0-RS3 connected to address lines A_0-A_3 respectively. Thus, the memory locations for the 6522 registers are as given in the table of figure 6.3.

Address	Register Desig.	Description	
		Write	Read
O9xO	ORB/IRB	Output Register "B"	Input Register "B"
O9x1	ORA/IRA	Output Register "A"	Input Register "A"
O9x2	DDRB	Data Direction Register "B"	
O9x3	DDRA	Data Direction Register "A"	
O9x4	T1C-L	T1 Low-Order Latches	T1 Low-Order Counter
O9x5	T1C-H	T1 High-Order Counter	
O9x6	T1L-L	T1 Low-Order Latches	
O9x7	T1L-H	T1 High-Order Latches	
O9x8	T2C-L	T2 Low-Order Latches	T2 Low-Order Counter
O9x9	T2C-H	T2 High-Order Counter	
O9xA	SR	Shift Register	
O9xB	ACR	Auxiliary Control Register	
O9xC	PCR	Peripheral Control Register	
O9xD	IFR	Interrupt Flag Register	
O9xE	IER	Interrupt Enable Register	
O9xF	ORA/IRA	Same as O9xO Except no "Handshake"	

Figure 6.3

Note: The chip select connections mean that these register locations are duplicated on page 0B. The fact that the register select lines are activated by address lines A_0-A_3, regardless of the state of address lines A_4-A_7, means that the hexadecimal code used for X, in figure 6.3, is unimportant.

$\overline{IRQ}$ (Interrupt Request)

The Interrupt Request output goes low whenever an internal interrupt flag is set and the corresponding interrupt enable bit is a logic 1. This output is "open-drain" to allow the interrupt request signal to be "wire-or'ed" with other equivalent signals in the system.

PA0-PA7 (Peripheral A Port)

The Peripheral A port consists of 8 lines which can be individually programmed to act as inputs or outputs under control of a Data Direction Register. The polarity of output pins is controlled by an Output Register and input data may be latched into an internal register under control of the CA1 line. All of these modes of operation are controlled by the system processor through the internal control registers. These lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode. Figure 6.4 illustrates the output circuit.

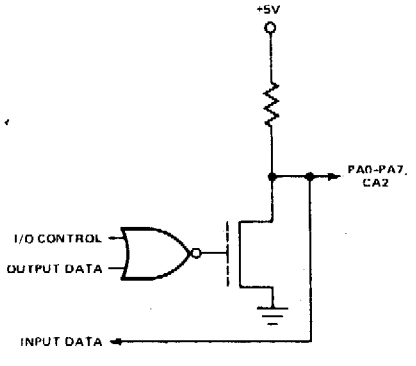


Figure 6.4

PB0-PB7 (Peripheral B Port)

The Peripheral B port consists of eight bi-directional lines which are controlled by an output register and a data direction register in much the same manner as the PA port. In addition, the polarity of the PB7 output signal can be controlled by one of the interval timers while the second timer can be programmed to count pulses on the PB6 pin. Peripheral B lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode. In addition, they are capable of sourcing 1.0mA at 1.5VDC in the output mode to allow the outputs to directly drive Darlington transistor circuits. Figure 6.5 is the circuit schematic.

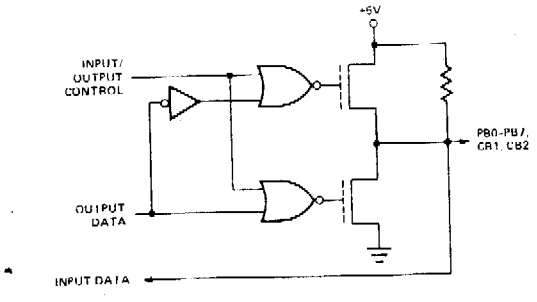


Figure 6.5

CA1, CA2 (Peripheral A Control Lines)

The two Peripheral A control lines act as interrupt inputs or as handshake outputs. Each line controls an internal interrupt flag with a corresponding interrupt enable bit. In addition, CA1 controls the latching of data on Peripheral A port input lines. CA1 is a high impedance input only while CA2 represents one standard TTL load in the input mode. CA2 will drive one standard TTL load in the output mode.

CB1, CB2 (Peripheral B Control Lines)

The Peripheral B control lines act as interrupt inputs or as handshake outputs. As with CA1 and CA2, each line controls an interrupt flag with a corresponding interrupt enable bit. In addition, these lines act as a serial port under control of the Shift Register. These lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode. Unlike PB0-PB7, CB1 and CB2 cannot drive Darlington transistor circuits.

CHAPTER 7

8154, RAM INPUT/OUTPUT

The 8154 provides 128 bytes of RAM and two 8-bit programmable I/O ports. In the 'Emma' systems the I/O ports are used for the keypad/display unit and the cassette interface.

The pin configuration diagram is shown in figure 7.1:-

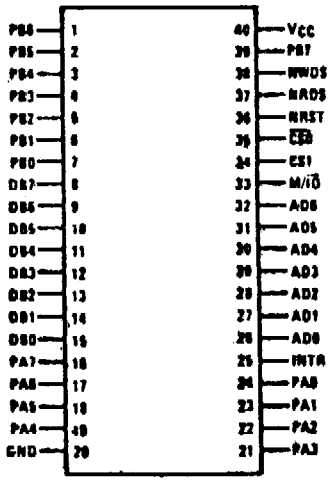


Figure 7.1

Pin functions:-

DB0 - DB7, Data Bus:- The eight bi-directional data bus lines are used to transfer data between the 8154 and the system processor. The 8154 data bus buffers are tri-state, giving a high impedance loading to the data bus unless a chip transfer operation is selected.

$\overline{CS0}$, CS1 Chip Select Inputs:- The microprocessor can only communicate with the 8154 when $\overline{CS0}$ is low and CS1 is high. For the other possible logic combinations for $\overline{CS0}$ and CS1, the tri-state data bus baffers will afford high impedance loading to the data bus.

On the 'Emma' board, the address decoding provides $\overline{CS0}$ low for memory pages 0C - 0F inclusive. CS1 is connected to address bus line A_q, thus the chip is selected when page 0E or 0F is accessed.

M/$\overline{IO}$, Memory I/O Select:- This select signal determines whether communication will be to the 8154 RAM or to the 8154 I/O ports. With M/$\overline{IO}$ high, the microprocessor can transfer to and from the RAM, M/$\overline{IO}$ low, communication will be with the I/O port registers.

The 'Emma' has the M/$\overline{IO}$ line connected to address line A_7, resulting in the 8154 registers and memory being available at the following locations:

0E0X - Clear Bit, Port A,
0E0Y - Clear Bit, Port B,
0E1X - Set Bit, Port A,
0E1Y - Set Bit, Port B,

Where X = 0 - 7 selects bit of port A
Y = 8 - F selects bit of port B

0E20 - Data Register, Port A.
0E21 - Data Register, Port B.
0E22 - Data Direction Register A ('0' = i/p, '1' = o/p)
0E23 - Data Direction Register B ('0' = i/p, '1' = o/p)
0E24 - Mode Definition Register, this is a control register which determines the handshaking modes of I/O transfer.
0E80 - 0EFF - RAM.

NRDS, Not Read Data Strobe:- A low level on this pin enables data to be read from the RAM I/O. On the 'Emma' board, this signal is formed by gating of the $\emptyset_2$ clock and the microprocessor R/$\overline{W}$ signal, to give;

$$NRDS = \overline{\emptyset_2 . \; R/\overline{W}}$$

NWDS, Not Write Data Strobe:- A low level on this pin enables data to be written to the RAM I/O. This signal is formed from the $\emptyset_2$ clock and R/$\overline{W}$, to obey the logic;

$$NWDS = \overline{\emptyset_2 . \; \overline{R/W}}$$

AD0 - AD6, Address Inputs:- Determine the memory location (M/$\overline{IO}$ high) or the IO register (M/$\overline{IO}$ low) accessed. These pins are connected to address bus lines A_0 - A_6.

PA0 - PA7, Port A:- Are input or output pins, as defined by the data held in port A data direction register.

On the 'Emma' board, port A is used by the monitor program for:-

PA_0 - PA_2,	binary encoded digit drives for display (outputs)
PA_3 - PA_5,	keypad column input (inputs)
PA_6	cassette interface output (output)
PA_7	cassette interface input (input)

PB0 - PB7, Port B:- Are input or output pins, as defined by the data held in port B data direction register.

On the 'Emma' board the monitor program defines port B as all outputs. Port B is then used to hold the segment data for each display character in turn, as PA_0 - PA_2 is repeatedly incremented to strobe the display.

INTR, Interrupt Request:- This is an active high signal used to interrupt the microprocessor when a strobed mode data transaction has occurred. Since this interrupt is not directly compatible with the active low $\overline{IRQ}$ of the 6502, the INTR pin is disabled (held low) on the 'Emma' board.

NRST, Master Reset:- NRST is the master reset input for the RAM I/O chip. A low on this pin clears all registers in the I/O portion of the chip and places the data bus in the high impedance state independent of any other control strobes. After a master reset the I/O ports are both defined as inputs. The master reset does not change any data previously stored in the RAM and does not allow data to be written into or read from RAM whilst NRST is low.

On the 'Emma' board, NRST is connected to the system reset line.

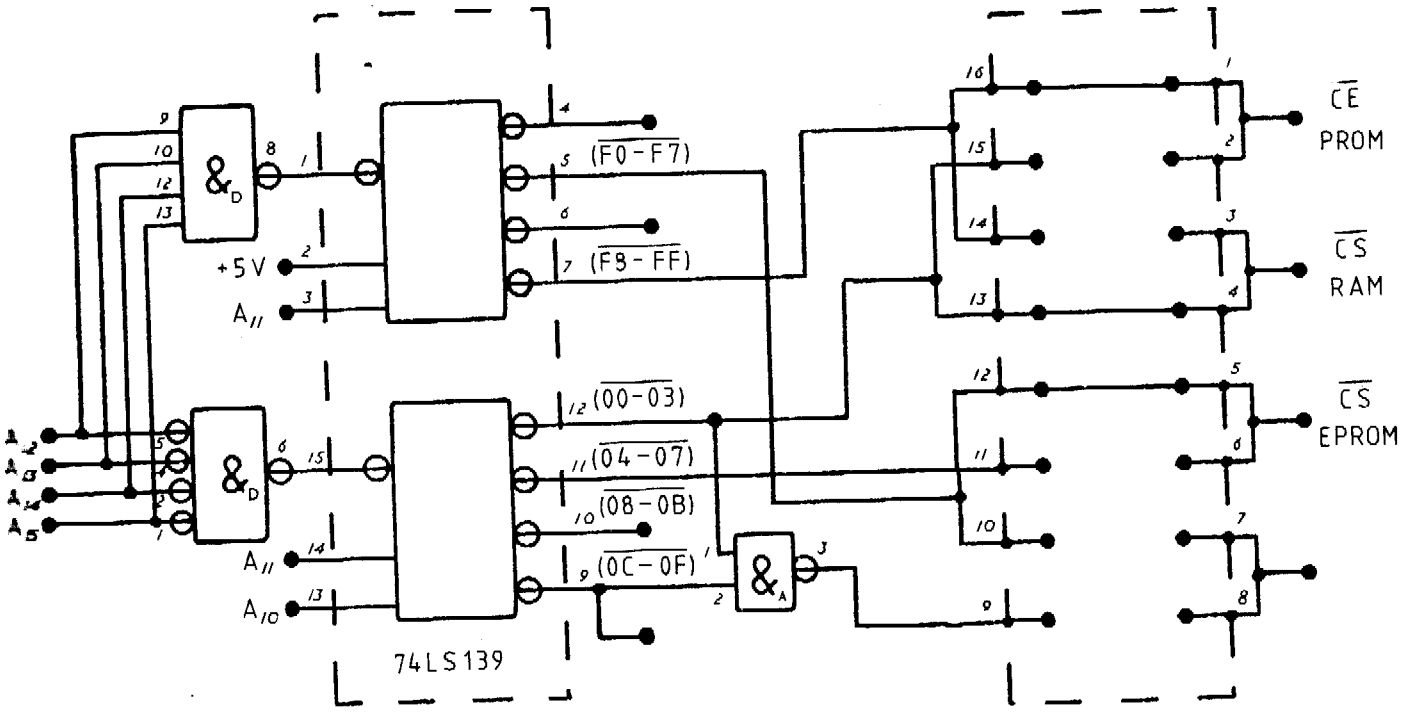
Since, on the 'Emma' board, the 8154 performs the function of display/keypad interface, and is not likely to perform any other task for most users, functional detail and characteristics are not included in this chapter. The complete manufacturer's data sheets are reproduced as appendix B to this manual.

CHAPTER 8

SYSTEM CONTROL SIGNALS

Address Decoding:-

In the 'Emma' system, address lines A_{10} - A_{15} are partially decoded to give the chip select signals required for the memory and I/O circuits. As shown in the circuit diagram of figure 8.1, lines A_{12} to A_{15} are used as inputs to a NAND gate, thus generating a logic low whenever lines A_{12} to A_{15} are high ('0' for pages F0 to FF).



PIN 10 TO $\overline{CS2}$, 6522
PIN 9 TO $\overline{CS0}$, 8154

Figure 8.1

Similarly, A_{12} to A_{15} are inverted, then NANDed, to give a '0' for pages 00 to 0F. The outputs from the two NAND gates are used as enable signals for the 74LS139 i.c., which is a dual 2-bit code into 4 line decoder. One decoder is enabled for pages F0 to FF and has inputs of '1' and A_{11}, thus generating enable low signals for the two 2K memory blocks pages F0 to F7 and F8 to FF. These enable signals are left as 2K blocks so that a 2716 EPROM may be selected by either signal. The second decoder is enabled for pages 00 to 0F and has as inputs, A_{10} and A_{11}. The four outputs from this decoder give enable low signals for the 1K blocks, pages 00 to 03, and 04 to 07, 08 to 0B, 0C to 0F. Enable low for pages 08 to 0B is wired to $\overline{CS2}$ of the 6522, whilst low for 0C - 0F is wired to $\overline{CS0}$ of the 8154. A wire link header is provided to enable the 'Emma' user to select the address locations for the RAM, PROM and EPROM. The 'Emma' will be shipped with header pin 1 shorted to pin 16 (PROM on pages F8 to FF), pin 4 to pin 13 (RAM on pages 00 to 03), pin 5 to pin 12 (EPROM on pages F0 to F7). An additional 2-input NAND gate has the low signals for pages 00 to 03 and 0C to 0F as inputs. This gate output will give a logic '1' only when pages 00 to 03 or pages 0C to 0F are selected. The 1K block, pages 04 to 07, is not used on the 'Emma' board. It is available from pin 11 of the wire link header for any user expansion.

Control Signal Shaping:-

The ϕ_2 clock is shaped and buffered by two inverters, as shown in the circuit diagram of figure 8.2.

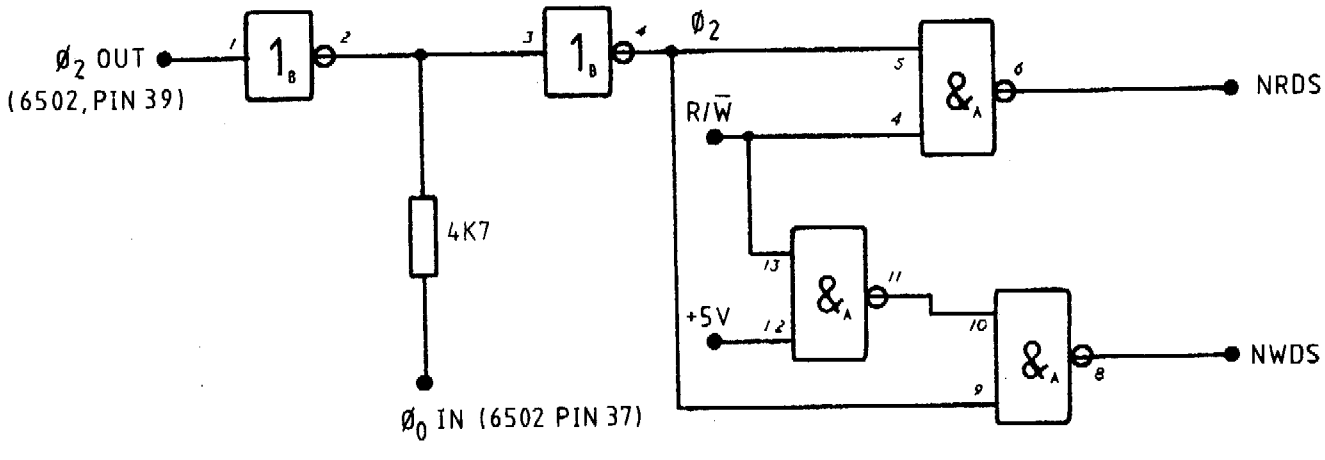


Figure 8.2

This buffered clock signal is then gated with the 6502 R/$\overline{W}$ signal to provide the two data strobes required for the 8154 i.c. The not write data strobe (NWDS) is also used as the $\overline{WE}$ signal for the 2114 RAM circuits.

Single Step :-

Whenever single step operation is selected, a non-maskable interrupt is generated for each instruction fetched, when pages F7 to FF are not accessed. Since the monitor resides on pages F7 to FF, it can run uninterrupted any other programs will break to the $\overline{NMI}$ vectors on completing each instruction. The circuit diagram for the single step interrupt signal is shown in figure 8.3

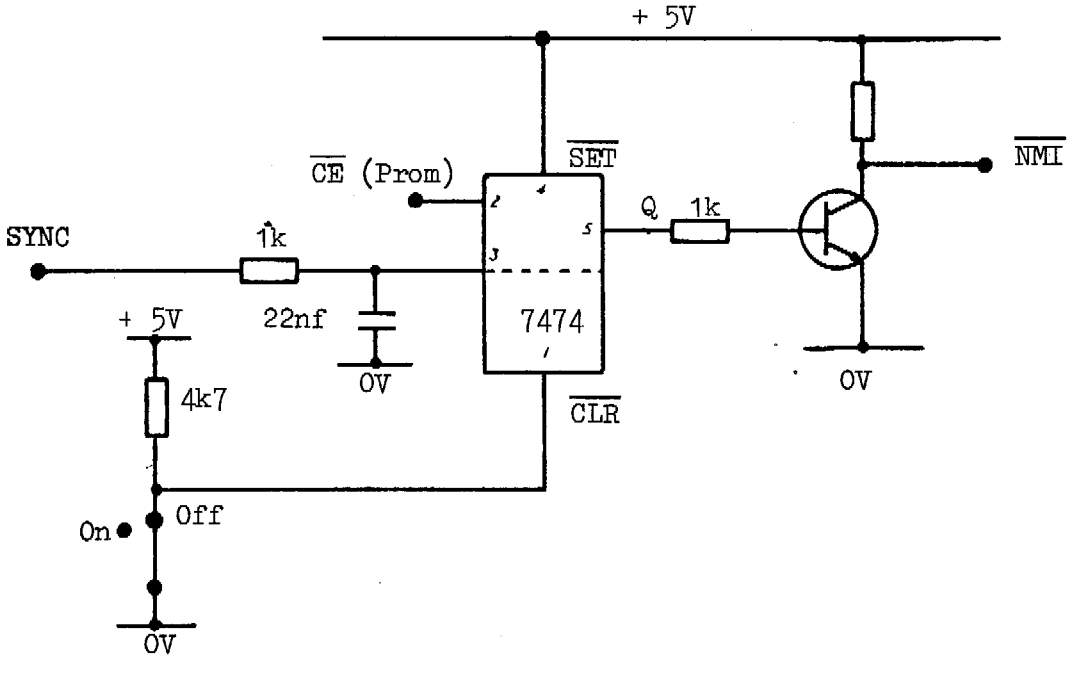


Fig 8.3

Note that the 6502 sync signal is used to generate the single step bistable clock pulse. To avoid a timing hazard with the bistable D input (gated PROM $\overline{CE}$ signal) the sync pulse is stretched with a CR network. When this sync pulse is examined on an oscilloscope it will appear distorted by the deliberate CR delay.

CHAPTER 9

CASSETTE INTERFACE

The EMMA uses a computer users tape standard (CUTS) interface for cassette tape recording of programs.

A complete circuit diagram of the cassette interface is shown in figure 9.1. Details of the 4024, 7-stage ripple counter/divider, and the 4013, dual D-type bistable are given in figures 9.2 and 9.3 respectively. The principle of operation of the interface is as follows:-

4024_1 counts $\emptyset_2$ clock pulses. A reset to this counter is generated by the logic gates connected to output pins 5,6 and 11 when the 4024 has counted 26 clock pulses. Thus a short duration pulse is generated every 26 microseconds.

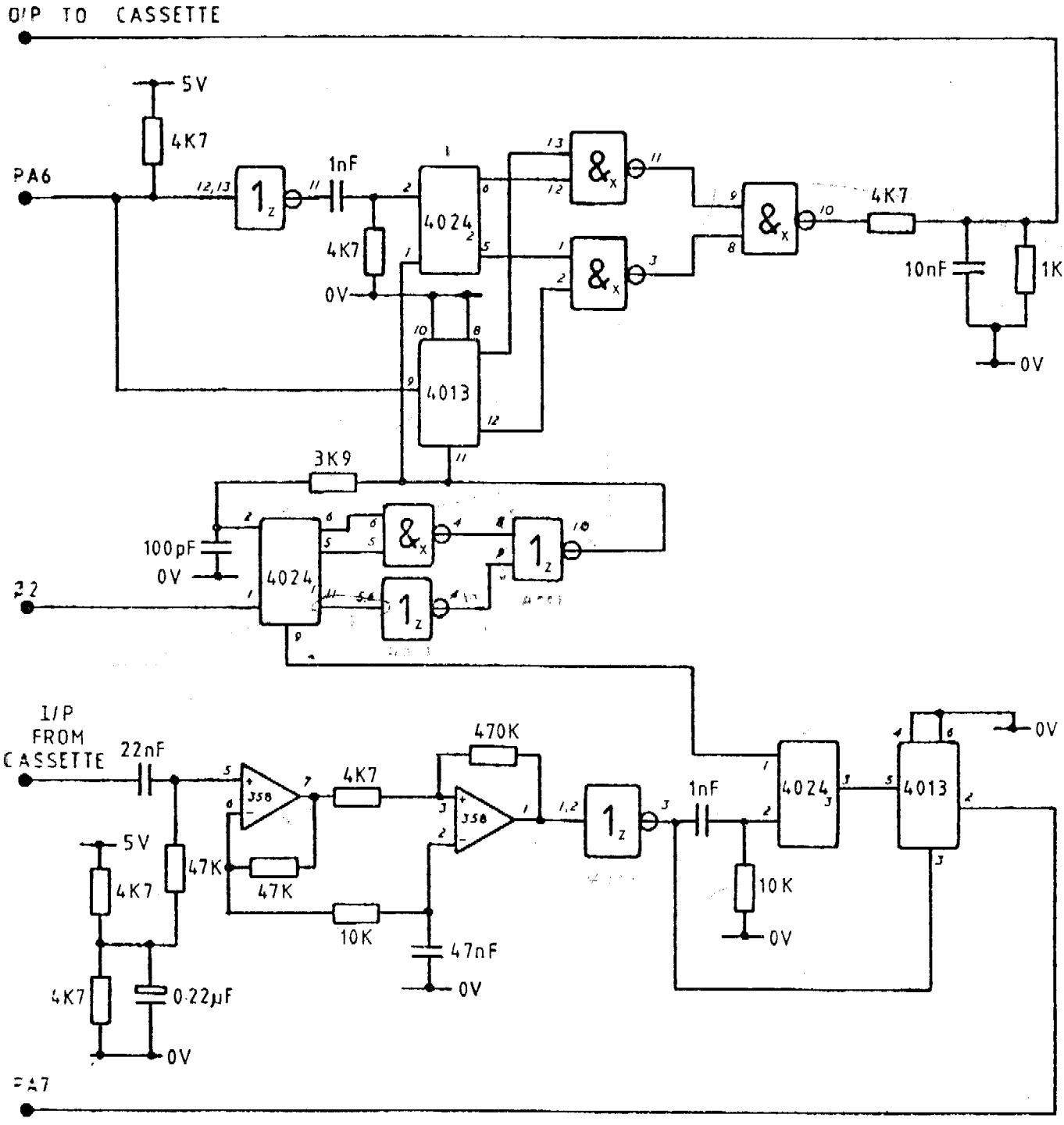
4024_2 counts the reset pulses; pin 6 of 4024_2 will go high after 8 pulses and then low after a further 8, producing a square wave on pin 6, with a periodic time of 16 x 26 microseconds (416μsec) giving a frequency of 2.4KHz. Similarly, a square wave with a frequency of 1.2KHz will be produced on pin 5 of 4024_2.

The two frequencies generated, 2.4KHz and 1.2KHz are applied to selection logic where the frequency gated out to the cassette is dependant upon the logic level on PA_6 of the 8154.

The input from the cassette is firstly amplified by the 358, dual operational amplifier. The potential divider to pin 5 of the 358 ensures that both inputs and the output to the first stage will be d.c. biased at the mid-point of the supply voltage (2.5V., with 5V. supply).

4024_3 counts the pulses generated from pin 9 of 4024_1.

The reset signals will occur at 4024_3 pin 2 at either 1.2KHz or 2.4KHz, this frequency will determine whether 4024_3 pin is '1' of '0' at reset time. This '1' or '0' is loaded into the 4013 and passed to PA_7 of the 8154.



'EMMA' - Cassette interface.

Fig 9.1(b)

CHAPTER 10

KEYBOARD/DISPLAY

The 'Emma' keyboard/display comprises 8 seven-segment displays and 24 key switches, mounted on a 6" x 6" printed circuit board which connects to the microcomputer board via a 16-way ribbon connector and d.i.l. header.

Circuit diagrams for the keyboard and display are given in figures 10.1 and 10.2, respectively. Please note that whilst a 7445 binary decoder is shown in both figures 10.1 and 10.2, only one 7445 is used, its decoded output being used for key column and display scanning simultaneously.

Keyboard:-

The 24 key switches are electrically organised into a 8 x 3 matrix. Two columns of eight keys are devoted to the haxadecimal keys, the third column providing the eight control key functions.

The eight rows are scanned by the monitor program sending a repeating binary count of 000 to 111 to output pins PA_0, PA_1, PA_2, of the 8154. At each step of the count one of the eight rows will be at logic '0'. To sense if a key switch has been depressed, the monitor reads 8154 input pins, PA_3, PA_4, PA_5. With no key depressed, these three inputs will all be at '1', a '0' will identify a column in which a key is depressed. By considering the code on PA_0, PA_1, PA_2, as well as knowing where the '0' occurs on PA_3, PA_4, or PA_5, the monitor program is able to deduce which key has been pressed. The monitor will not read a hex key until a control key has been pressed to select a mode of operation.

Display:-

Eight FND 560, 0.5" seven-segment l.e.d. characters form the 'Emma'

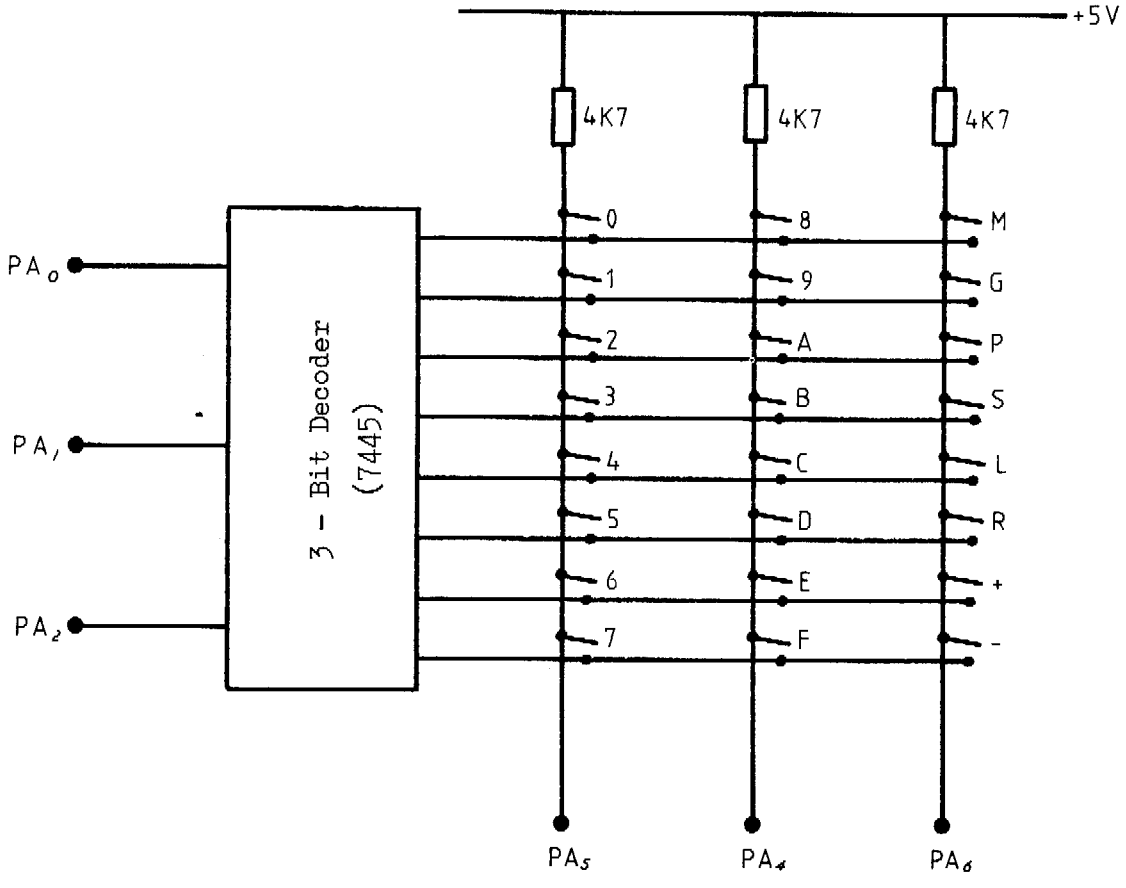
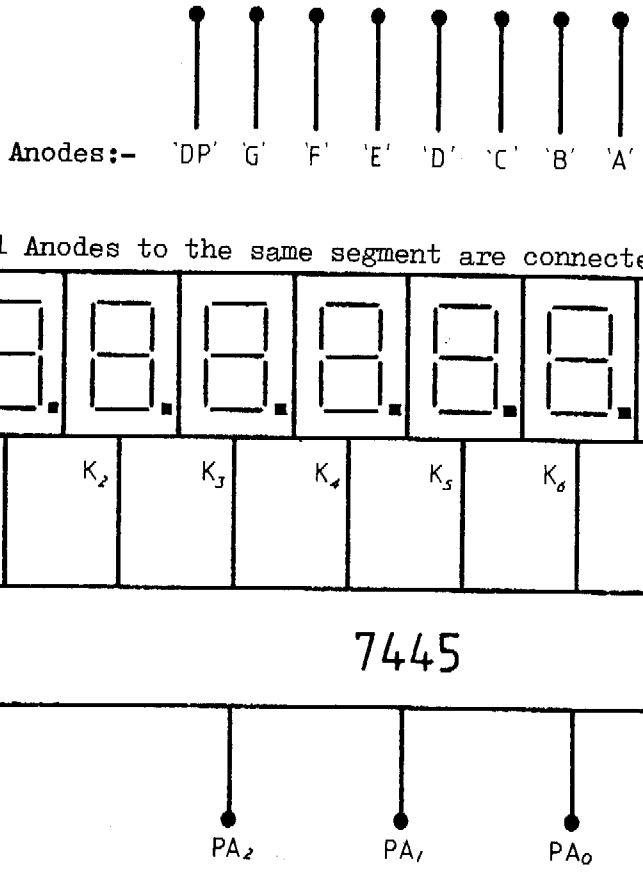
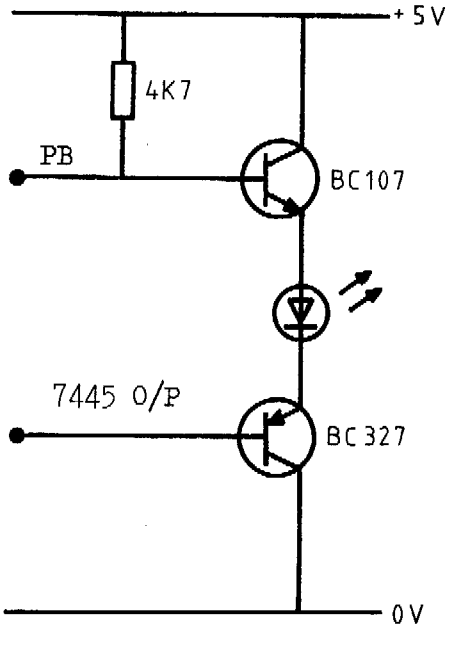

+5V
4K7
4K7
4K7
PA0
PA1
PA2
3 - Bit Decoder
(7445)
0
1
2
3
4
5
6
7
8
9
A
B
C
D
E
F
M
G
P
S
L
R
+
-
PA5
PA4
PA6

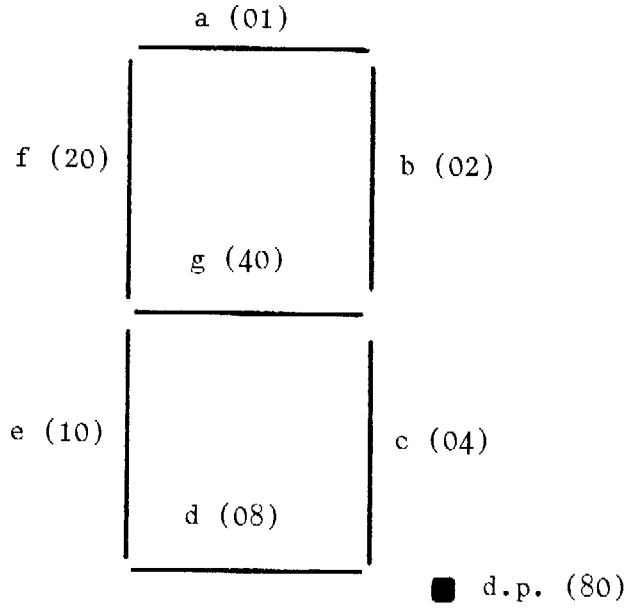
Fig 10.1



Display Organisation



Segment Drive Circuit



Input coding for segment selection

Fig 10.2

display. The display is strobed continuously by the monitor. As the binary codes on PA_0, PA_1, PA_2, pulls one of eight common cathodes low, the code on port PB_0 to PB_7 (8154) determines the segments illuminated on the selected character. Code 000 on PA_0, PA_1, PA_2, selects the left most character, 111 selects the right most character. The user, in producing a program which makes use of the display, should ensure that the display is scanned. A single continuous character will be slightly over-driven beyond the maximum average current rating of the FND 560 display. This situation is unavoidable, since an acceptable level of display brightness has to be achieved when a character is produced for only $\frac{1}{8}$ of the time.

CHAPTER 11

'EMMA' INTERCONNECTION DETAILS

The'Emma' microcomputer is based on a 12" x 9" printed circuit board. This circuit board has been designed to facilitate teaching, by:-

(a) organising the lay-out in such a way that the various elements of the computer are identified within separate blocks on the board,

(b) making all control bus, data bus and address bus lines accessible (and identified) on 0.1" spacing connector pins,

(c) giving easy access to the user I/O ports via standard 4mm. Sockets, and 0.1" spacing connector pins.

The complete circuit diagram for the 'Emma' is given in figure 11.1. This diagram does not include the cassette interface and keyboard/display details, which is given in chapters 9 and 10, respectively.

Integrated circuit details, relating to figure 11.1 are:-

IC1, 6502 microprocessor.
IC2, 6522 VIA.
IC3, IC4, 2114 RAM.
IC5, IC6, 74S571 (or equivalent) PROM.
IC7, 2716 EPROM.
IC8, 8154 RAM I/O.
IC9, 7474 Dual D-type Bistable.
IC10, 74LS00 and Quad 2-input NAND ($\&_A$)
IC11, 74LS139 Dual 2 line to 4 line decoder.
IC12, Decode select linking
IC13, 74LS20 Dual 4-input NAND. ($\&_D$)
IC14, 74LS04 Hex inverter. (1_B)

Pin details for the expansion connector are given in figure 11.2

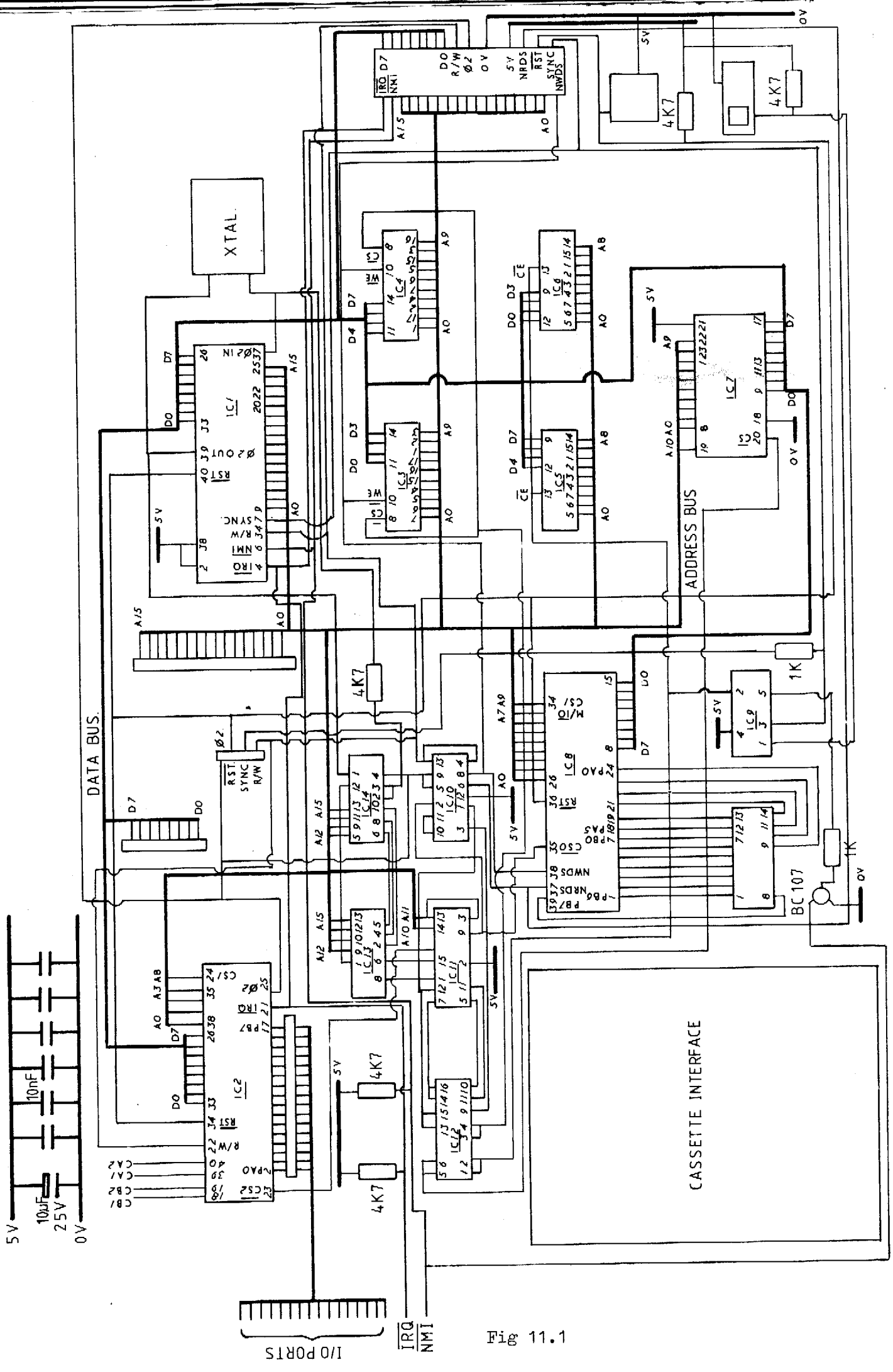


Fig 11.1

'HYMA' - Complete circuit diagram.