

GENERAL DESCRIPTION

The B.E.M-SBC4A/4B, series of high performance Single Board Computers are particularly suitable to be used in more complex applications. Special care has been given to allow access to all local devices (memory as well as VIA and USART) through DMA control. Except for the clock signals (E and Q), the whole bus structure is bi-directional. In spite of this powerful feature, the B.E.M-SBC4A/4B will also successfully be applied in more demanding stand alone applications.

Both cards are provided with the powerful 6809 microprocessor (4 MHz version is standard), a 6522 VIA for parallel I/O and timer applications, a 2651 USART for serial I/O communication and six 28-pin sockets for memory devices. The B.E.M-SBC4A and 4B differ only in the RAM/EPROM(ROM) allocation of the sockets. In the 4A version only 2 sockets are allocated to RAM devices (2 kbyte or 8 kbyte types) and 4 sockets are available for EPROM's (TEXAS INSTR. family or equivalent can be used). Jumpers will allow the selection of 4 kbyte, 8 kbyte and even 16 kbyte types (2532, 2564 and 2528). In the 4B version on the other hand, only one socket is allocated to EPROM(ROM) (the same restrictions as with the 4A version) and 5 sockets are available for RAM (2 kbyte or 8 kbyte types). The 4A version will be ideal in applications requiring a lot of resident software, while the 4B will be ideal in disk based systems or other applications requiring a lot of RAM and relatively few resident software. NOTE: in the 4A version the total on-board memory capacity can not exceed the processor addressing capacity (65 k max.).

Both cards are provided with a flexible PROM decoder circuit, enabling the application of custom designed memory map configurations. However, some standard memory map configurations are available (see page 7 for details). With each standard PROM, 2 different memory maps can be selected with a jumper.

The processor and the USART are provided with separate crystal based clocks.

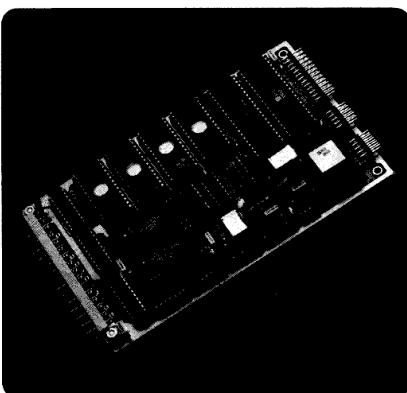
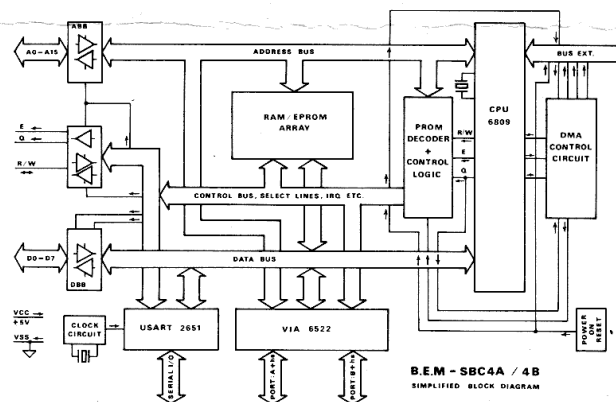
An important part of the local control logic on the B.E.M-SBC4A/4B cards is dedicated to the DMA control function. Bi-directional bus buffers are used for address bus, data bus and R/W.

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FOR MICROPROCESSOR APPLICATIONS

FEATURES

- ★ HIGH PERFORMANCE, 6809 BASED, SINGLE BOARD COMPUTERS
- ★ B.E.M-SBC4A WITH 2 → 16 KBYTE RAM AND 4 → 64 KBYTE ROM/ EPROM
B.E.M-SBC 4B WITH 2 → 40 KBYTE RAM AND 4 → 16 KBYTE ROM/ EPROM
- ★ FULLY BUFFERED AND DECODED (PROM). BI-DIRECTIONAL BUS STRUCTURE AND DMA CONTROL SECTION WILL ALLOW ACCESS TO ALL ON-BOARD DEVICES (MEMORY, VIA, USART) BY DMA
- ★ SINGLE POWER SUPPLY (+5V) REQUIRED
- ★ 1 VIA (6522) FOR PARALLEL I/O AND TIMER APPLICATIONS PROVIDING 16 PARALLEL I/O LINES + 4 HANDSHAKE LINES, TWO 16-BIT INTERVAL TIMERS/COUNTERS AND ONE 8-BIT SHIFTREGISTER
- ★ 1 USART (2651) FOR SYNCHRONOUS AND ASYNCHRONOUS SERIAL COMMUNICATION
- ★ SEPARATE CRYSTAL BASED CLOCKS FOR CPU AND USART
- ★ ALSO SUITABLE FOR STAND-ALONE APPLICATIONS
- ★ ON BOARD POWER-ON-RESET CIRCUIT
- ★ FLAT CABLE COMPATIBLE HEADERS FOR ALL I/O CONNECTIONS
- ★ ALL IC's MOUNTED IN HIGH QUALITY MACHINE TOOLED SOCKETS
- ★ GENEROUS OEM DISCOUNTS AVAILABLE



(MAIN) BUS CONNECTIONS

Pin	Function
1	N.C.
2	VSS (GND.)
3	D 7
4	D 6
5	D 5
6	D 4
7	D 3
8	D 2
9	D 1
10	D 0

Pin	Function
11	Q*
12	R/W
13	E
14	A 15
15	A 14
16	A 13
17	A 12
18	A 11
19	A 10
20	A 9

Pin	Function
21	A 8
22	A 7
23	A 6
24	A 5
25	A 4
26	A 3
27	A 2
28	A 1
29	A 0
30	VCC (+ 5V)
31	N.C.

* Via jumper J1.

Continued from page 1

Some properties of the on-board (local) I/O devices are summarized below:

1) One 6522 VIA (Versatile Interface Adapter) is standard (high speed version 6522A is optional). The VIA provides two 8-bit bi-directional ports, each with two programmable control lines for handshake purposes. Each I/O line can individually be programmed to be used either as input or as output. Moreover, two 16-bit programmable interval timers/counters and one 8-bit shiftregister are available to the user. The VIA can be used in many different modes, full details can be found in the original datasheet (Mos, Commodore, Rockwell or Synertek). Connections are made through a 26-pin flat cable compatible header with a pin lay-out equal to other BEM application cards and parallel I/O adapters.

2) One 2651 USART (Universal Synchronous Asynchronous Receiver Transmitter) is also standard. The 2651 is a highly sophisticated communication device, of which all parameters can be programmed (baudrate, parity, etc.). Applications range from single terminal control to complex synchronous multi-user networks. Connections are made through a 10-pin flat cable compatible

header with a pin lay-out equal to the B.E.M-AD3 (RS-232-C/ 20 mA current loop) adapter. All details on the 2651 USART can be found in the original datasheet (Signetics, National Semiconductor or Western Digital).

Both cards are provided with a POWER-ON-RESET circuit. Besides to the processor, VIA and USART, the output of this circuit (open collector) is connected also to pin 1 of the BUS EXTENSION header. A remote controlled reset switch (normally open) can be connected to the card (user supplied). If used, the on-board circuit will eliminate contact bounce.

Both cards require a single 5V power supply voltage to operate. Power supply connections as well as all address, data, clock and R/W signals are available through the, 31-pin B.E.M-BUS compatible connector (DIN 41617).

The B.E.M-SBC4A/4B are provided with high quality machine tooled sockets. Low Power Schottky IC's are used where possible. All jumpers are provided with jumper plugs for quick and simple modifications.

BUS EXTENSION FLAT CABLE HEADER CONNECTIONS

Pin	Function
1	RESET
2	FIRQ*
3	NMI
4	IRQ*
5	BA

Pin	Function
6	BS
7	DMAC
8	DMAR
9	HALT
▶ 10	MRDY*

* NOTES: FIRQ and IRQ are interchangeable or can be disconnected via jumpers (J11 → J14). MRDY pin is also jumper selectable to be connected to ground, the MRDY input of the CPU or disconnected (J10).

1) **RESET** A low level on the system RESET line will initiate the RESET procedure. The RESET line is connected to the P.O.R. (POWER ON RESET) circuit. After a return from a POWER-DOWN condition or a release of the RESET switch (if connected externally), this line will be low active for at least 50 msec. System cards provided with individual P.O.R. circuitry (e.g. B.E.M-PSIO-1 or B.E.M-VIA-1), interconnected to this line will generally cause no problems (open collector output). A pull-up resistor of 3k3 is provided on the card.

2) **FIRQ*** A low level on the FIRQ line will initiate a FAST INTERRUPT REQUEST sequence, provided its mask bit (6) in the Condition Code Register has been cleared (0) before. The FIRQ sequence has priority over the normal INTERRUPT REQUEST (IRQ, see 4), and is fast in the sense that it stacks the contents of the CC Register and the program counter only. The FIRQ line is generally connected to the FIRQ input of the processor (Jumper J11 installed). A pull-up resistor of 3k3 is provided on the card.

3) **NMI** A high to low transition on the NMI line will initiate the NON MASKABLE INTERRUPT procedure. A Non Maskable Interrupt can not be inhibited and also has higher priority than IRQ, FIRQ or software interrupts. The NMI line is connected directly to the NMI input of the CPU. A pull-up resistor of 3k3 is provided on the card.

4) **IRQ*** A low level on the IRQ line will initiate a normal INTERRUPT REQUEST sequence, provided its mask bit (4) in the Condition Code Register has been cleared (0) before. IRQ has lower priority than FIRQ and takes more time to finish because the entire machine state will be stacked. The IRQ line will generally be connected to the IRQ input of the CPU (Jumper J14 installed). A pull-up resistor of 3k3 is provided on the card.

5) **BA** and **BS** The BA (BUS AVAILABLE) and BS (BUS STATUS) lines indicate the CPU state as represented in the table below. Both lines are buffered.

State		Description
BA	BS	
0	0	Normal (Running)
0	1	Interrupt Acknowledge
1	0	SYNC Acknowledge
1	1	HALT or Bus Grant

7) **DMAC** A low level on this output line indicates that the bus is free (direction is inverted). The DMAC (DMA ACKNOWLEDGE) line will periodically become low after a DMA REQUEST (DMAR, see 8) or permanently low if and as long as the processor is halted (HALT, see 9). The input is provided with a 3k3 pull-up resistor on the card. More details on DMA can be found on page 5.

8) **DMAR** A low level applied to the DMAR (DMA REQUEST) input line will start the DMA procedure (CYCLE STEAL DMA). The user must understand DMA implications thoroughly, because of the 6809 auto-refresh procedure during DMA operations. The DMAC (pin 7) must be monitored permanently by the DMA CONTROLLER. During high cycles the DMA controller must be off the bus to allow auto refreshing of the processor.

9) **HALT** A low level applied to this input will halt the processor as soon as the current instruction is fully completed (up to 20 clock cycles). The HALT input can be used to perform HALT MODE DMA. The bus will be available for DMA, as soon as the DMAC line is low. During the HALT mode, the processor is stopped and does not require auto refresh.

10) **MRDY*** The function of pin 10 is jumper selectable (J10) and can be connected to ground, disconnected or connected to the MRDY (MEMORY READY) input of the processor. The MRDY line will generally be used for interfacing with slow memory and peripheral devices requiring longer READ and WRITE cycles. The READ and WRITE cycles can be stretched with a maximum of 10 clock cycles.

NOTE: Some older types of B.E.M application and I/O cards, able to generate an Interrupt Request, have the IRQ line connected to pin 2 of the BUS EXTENSION HEADER (650X and 6800 compatible). For this purpose, the B.E.M-SBC4A/4B cards are provided with jumpers (J11 → J14) enabling the user to interchange the functions of pin 2 and 4 (FIRQ ↔ IRQ).

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias	0°C to + 70°C
Storage Temperature	-55°C to +120°C
Voltage on any Pin with respect to Ground	-0.3 V to +7 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the B.E.M-SBC4A/4B cards. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

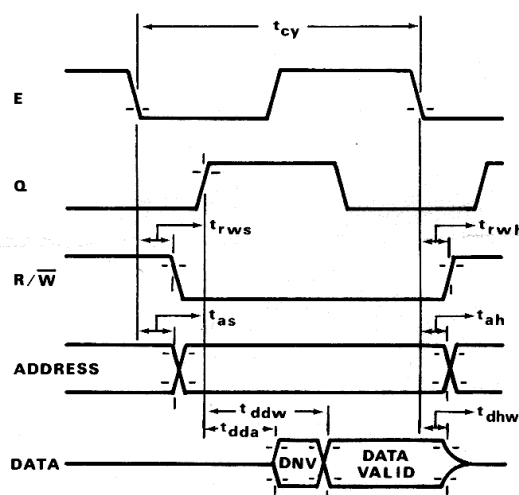
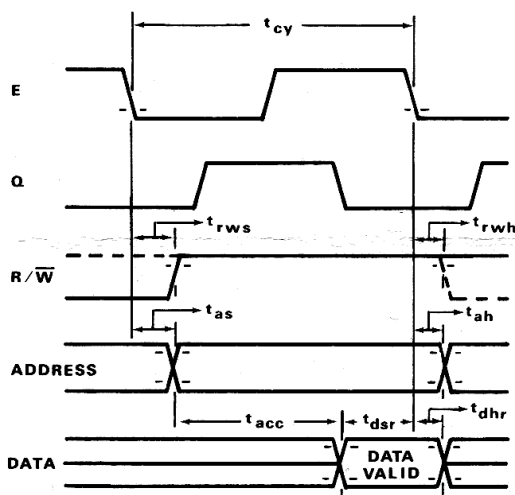
DC CHARACTERISTICS

TA = 0°C to +70°C, VCC = +5 V ± 5% (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
MAIN BUS	I _{LIH}			20 100	μA μA	V _{IN} = 2.7V V _{IN} = 7.0V
	I _{LIL}			-400	μA	V _{IN} = 0.4V
	I _{LD}			20 -200	μA μA	V _{IN} = 2.7V V _{IN} = 0.4V
	I _{CC}		600	800	mA	VCC = 5.25V TA = 0°C (worst case conditions)
	V _{IL}	-0.5		0.8	V	
	V _{IH}	2		VCC	V	
	V _{OL}			0.5	V	I _{OL} = 24 mA
BUS EXT.	V _{OH}	2			V	I _{OH} = -15 mA
	V _{IHT}	2			V	RESET, NMI, IRQ, FIRQ and MRDY
	V _{IHTR}	4			V	RESET only
	V _{ILT}	-0.3		0.8	V	RESET, NMI, IRQ, FIRQ and MRDY
	V _{OL1}			0.5	V	I _{OL1} = 8 mA
	V _{OL2}			0.4	V	I _{OL2} = 4 mA
	V _{OH2}	2.4			V	I _{OH2} = -0.4 mA
VIA	V _{IL1}	0.5		0.8	V	DMAR and HALT inputs provided with pull-up resistors (3k3)
	V _{IH1}	2		VCC	V	
	V _{IHV}	2.4		VCC	V	
	V _{ILV}	-0.3		0.4	V	
	I _{INV}			±2.5	μA	V _{IN} = 0 to 5V
	I _{IHV}	-100			μA	V _{IN} = 2.4V
	I _{ILV}			-1.6	mA	V _{IN} = 0.4V
USART	V _{OHV}	2.4			V	I _L = -100 μA
	V _{OLV}			0.4	V	I _L = 1.6 mA
	I _{OHV}	-100 -1.0			μA mA	V _{OH} = 2.4V V _{OH} = 1.5V (PB0 → PB7)
	I _{OLV}	1.6			mA	V _{OL} = 0.4V
	I _{OFF}			10	μA	
	C _{IN}			7	pF	1 MHz
	C _{OUT}			10	pF	1 MHz
USART	V _{ILU}	-0.3		0.8	V	
	V _{IHU}	2.0			V	
	V _{OLU}			0.4	V	I _{OL} = 1.6 mA
	V _{OHU}	2.4			V	I _{OH} = -100 μA
	I _{ILU}			10	μA	V _{IN} = 0 to 5.5V

AC CHARACTERISTICS (BUS READ/WRITE CYCLE TIMING)

Symbol	Parameter	Limits		Unit	Test Conditions
		Min.	Max.		
t_{cy}	Total Clock Cycle Time (E, Q)	1000		nsec	Input pulse levels 0.8V to 2.4V. Input rise and fall times: 10 nsec. VCC = 5.0V TA = 0 to +70 °C Timing figures and diagrams are for bus signals only.
t_{as}	Address Set-Up Time		200	nsec	
t_{ah}	Address Hold Time	30		nsec	
t_{dhw}	Data Hold Time (Write Mode)	30		nsec	
t_{dsr}	Data Set-Up Time (Read Mode)	130		nsec	
t_{dhr}	Data Hold Time (Read Mode)	0		nsec	
t_{rws}	R/W Set-Up Time		200	nsec	
t_{rwh}	R/W Hold Time	30		nsec	
t_{dda}	Delay Time Q High to Data Bus Active		35	nsec	
t_{ddw}	Delay Time Q High to Data Out Valid		225	nsec	
t_{acc}	Memory Read Access Time		655	nsec	



VIA FLAT CABLE HEADER CONNECTIONS

Pin	Function (port: A)
1	VCC (+5V)
2	CA1
3	CA2
4	N.C.
5	PA0
6	PA1
7	PA2
8	PA3
9	PA4
10	PA5
11	PA6
12	PA7
13	VSS (0V)

Pin	Function (port: B)
14	VSS (0V)
15	PB0
16	PB1
17	PB2
18	PB3
19	PB4
20	PB5
21	PB6
22	PB7
23	IRQ*
24	CB1
25	CB2
▶26	VCC (+5V)

* To local IRQ via jumper J16.

USART FLAT CABLE HEADER CONNECTIONS

Pin	Function
1	VSS
2	DCD
3	CTS
4	TxD
5	VCC/DSR*
6	RTS
7	DTR
8	RxC
9	TxC
▶10	RxD

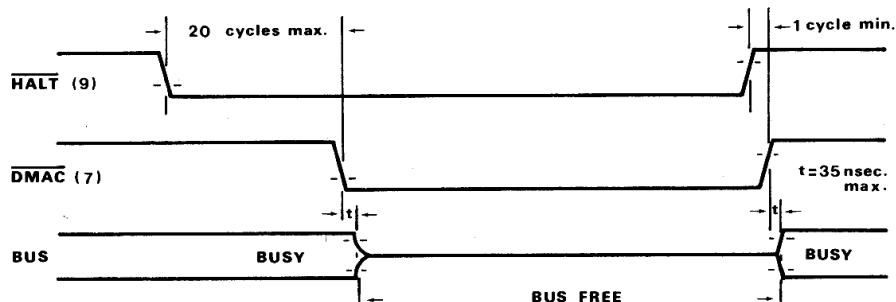
* Selectable via jumper J9.

DMA CONTROL NOTES

Two different DMA control modes can be used with the B.E.M-SBC4A/4B cards. Which mode will be used depends on the application.

- 1) **HALT MODE DMA** During the HALT mode, the processor is stopped and the bus direction is inverted to allow access to the bus and the local memory, VIA and USART available on the B.E.M-SBC4A/4B. The

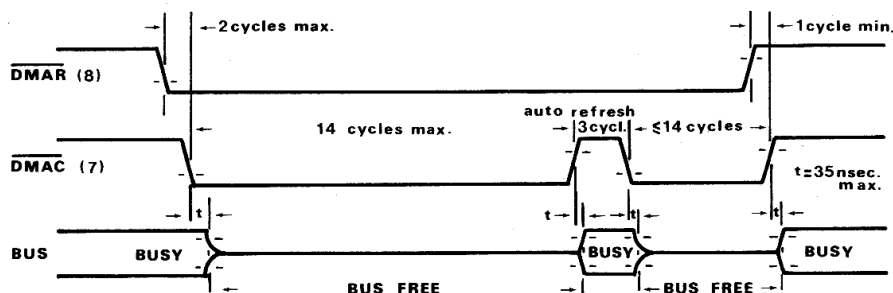
HALT mode is initiated by making the HALT input (pin 9 of BUS EXTENSION header) low. As the timing diagram represented below shows, the bus will be free some time after HALT line is turned low (up to 20 clock cycles). The processor has to finish its current instruction completely. The bus will be available for DMA operations as soon and as long as the DMAC signal (pin 7 of BUS EXTENSION header) is low. Once halted, there are no timing limits in respect to the length of the DMA operation.



HALT MODE DMA TIMING

- 2) **CYCLE STEAL DMA** In the CYCLE STEAL DMA mode, the DMAR (DMA REQUEST) line (pin 8 of BUS EXTENSION header) is used for DMA control. Provided that the processor is not in the HALT mode as described in the previous section, the CYCLE STEAL DMA procedure will be initiated by making the DMAR input low. Within 2 clock cycles after DMAR is switched to a low level, the DMAC output line will be switched to a low level also, acknowledging that

the bus is free. In general there are no problems if the DMA cycle is equal or shorter than 14 CPU clock cycles. However, if the DMA procedure takes more time, the CPU will periodically require access to the bus (1 clock cycle, surrounded by dead cycles) for auto-refresh purposes. This implies the DMA controller must allow interruption of the DMA operation during long DMA cycles. The drawing represented below, shows the timing requirements in the CYCLE STEAL DMA mode.



CYCLE STEAL DMA TIMING (> 14 cycles)

PIN LAY-OUT CPU, VIA & USART

VSS	1	40	HALT
NMI	2	39	XTAL
IRQ	3	38	EXTAL
FIRQ	4	37	RESET
BS	5	36	MRDY
BA	6	35	Q
VCC	7	34	E
A0	8	33	DMA/BREQ
A1	9	32	R/W
A2	10	31	D0
A3	11	30	D1
A4	12	29	D2
A5	13	28	D3
A6	14	27	D4
A7	15	26	D5
A8	16	25	D6
A9	17	24	D7
A10	18	23	A15
A11	19	22	A14
A12	20	21	A13

VSS	1	40	CA1
PA0	2	39	CA2
PA1	3	38	RS0
PA2	4	37	RS1
PA3	5	36	RS2
PA4	6	35	RS3
PA5	7	34	RES
PA6	8	33	D0
PA7	9	32	D1
PB0	10	31	D2
PB1	11	30	D3
PB2	12	29	D4
PB3	13	28	D5
PB4	14	27	D6
PB5	15	26	D7
PB6	16	25	E2
PB7	17	24	CS1
CB1	18	23	CS2
CB2	19	22	R/W
VCC	20	21	IRQ

D2	1	28	D1
D3	2	27	D0
RxD	3	26	VCC
VSS	4	25	RxC
D4	5	24	DTR
D5	6	23	RTS
D6	7	22	DSR
D7	8	21	RESET
TxC	9	20	BRCLK
A1	10	19	TxD
CE	11	18	TEMT/*
A0	12	17	CTS
R/W	13	16	DCD
RxDV	14	15	TxDV
			DSCWG

WARNING!!!

Bus lines may not be short circuited for extended periods. According to Bus Buffer specifications only one output per device may be shorted at a time for continuous periods lasting no longer than one second.



MEMORY MAP AND REGISTER ADDRESSES

The drawings represented below show the memory map configurations available for the B.E.M-SBC4A/4B single board computers together with the memory details of the circuit diagram. The numbers within a circle refer to the socket numbers on the cards. If not specified, the cards will be delivered with the standard PROM decoder (4A1 respectively 4B1). With the standard PROM, the card can be used only with 2 kbyte RAM's such as the TMM 2016 (Toshiba), the HM 6116 (Hitachi) or equivalent types. Two different memory map configurations can be selected, respectively to be used with 4 kbyte (2532) and 8 kbyte (2564) EPROM types (TEXAS INSTR. family or equivalent).

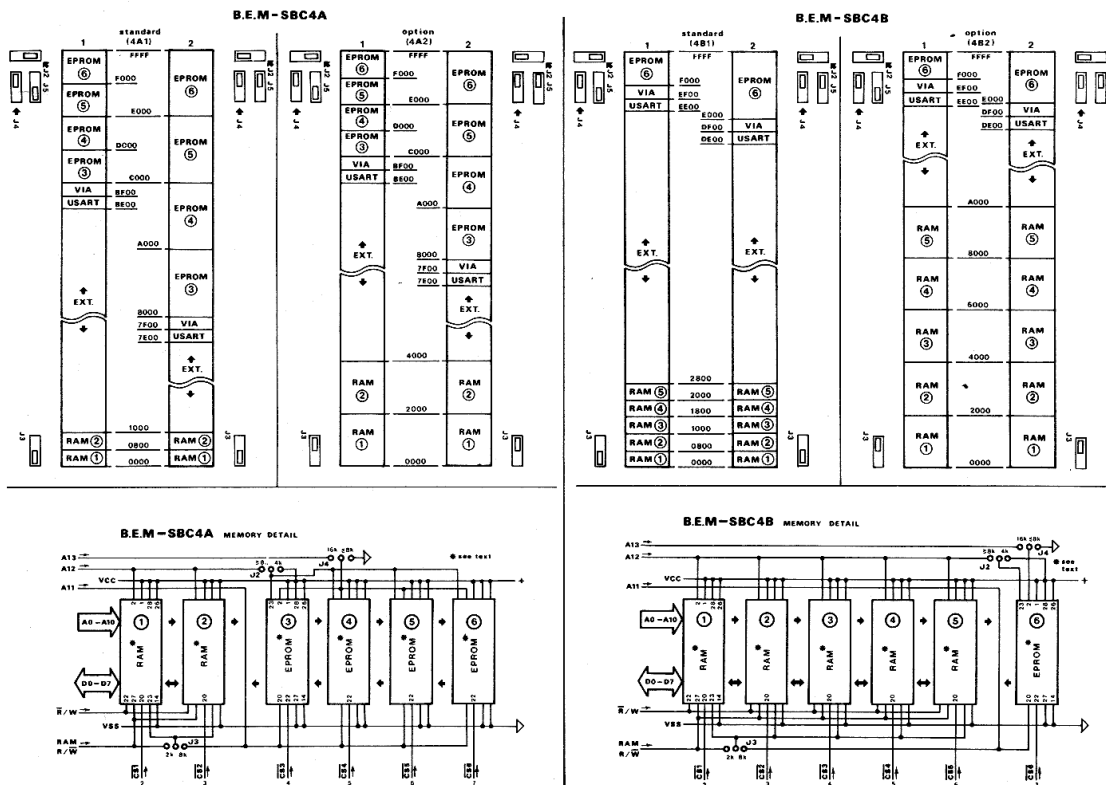
However, an optional PROM decoder can be delivered on request without additional cost. When ordering, the customer must specify 4A2 or 4B2. These PROM's are useful only with 8 kbyte RAM's such as the TC 5564 (Toshiba), the HM 6264 (Hitachi) or equivalent types. Also two different memory map configurations can be selected in this case, respectively to be used with 4 kbyte and 8 kbyte EPROM types (same restrictions as above).

On request any memory map configuration can be delivered to custom specifications at additional cost. The memory field of any device available on the cards can be split into sections of one page (256 address locations) minimum which can be located anywhere in the map in steps of one page. Also 16 kbyte EPROM devices (2528) can be used in custom map configurations. Please contact factory or nearest distributor for details and cost.

The areas, denoted with EXT. are free for external expansion. As all maps show, one page is reserved for the VIA as well as for the USART. The VIA only requires 16 successive address locations as represented in the table to the right. Starting with the

Device	Relative address	Function / Register		
		Name	Write	Read
6522 VIA	0	ORB/IRB	Output Register Port "B"	Input Register Port "B"
	1	ORA/IRA	Output Register Port "A"	Input Register Port "A"
	2	DDRB	Data Direction Register "B"	
	3	DDRA	Data Direction Register "A"	
	4	T1L/C-L	T1 Low-Order Latch	T1 Low-Order Counter
	5	T1C-H	T1 High-Order Counter	
	6	T1L-L	T1 Low-Order Latch	
	7	T1L-H	T1 High-Order Latch	
	8	T2L/C-L	T2 Low-Order Latch	T2 Low-Order Counter
	9	T2C-H	T2 High-Order Counter	
	A	SR	Shift Register	
	B	ACR	Auxiliary Control Register	
	C	PCR	Peripheral Control Register	
	D	IFR	Interrupt Flag Register	
	E	IER	Interrupt Enable Register	
	F	ORA/IRA	Same as Address 1 Except No "Handshake"	
2651 USART	0 4 8 C	THR/RHR	Transmit Holding Register	Receive Holding Register
	1 5 9 D	SSDR/SR	SYN 1 / SYN 2 / DLE Register	Status Register
	2 6 A E	MR	Mode Register 1/2	
	3 7 B F	CR	Command Register	

start address in the map (relative address 0 in the table above) all 16 registers can repeatedly be accessed every 16 locations throughout the reserved page. The same is valid for the USART, with this difference that the USART only requires 4 successive address locations.





GENERAL DESCRIPTION

The B.E.M-SBC4C and B.E.M-SBC5C Single Board Computers are modified versions of the A and B models and are intended to replace them in time. The C versions accept 24-pin and 28-pin "BYTE WIDE" EPROM's and RAM's with JEDEC JC-42 pinning, which have become the industrial standard for these devices. The A and B versions only accept EPROM's with the so-called TEXAS pinning. This update must be considered as a supplement to the 4A/4B and 5A/5B data sheets. Only the memory section shows minor differences, all other features and circuit details have been remained unchanged.

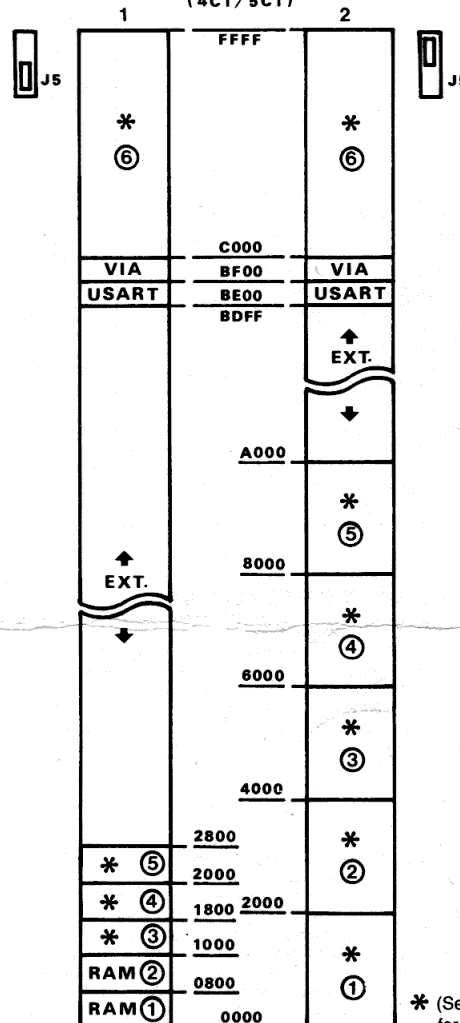
The six 28-pin sockets available for memory devices can be allocated to RAM or EPROM devices. The memory map configuration is determined by a PROM decoder circuit. Some standard map's are available (see drawing to the right). Custom map's can be delivered at additional cost with the same limitations as the A and B versions.

Many different memory types can be applied in the sockets 1 to 6. The configuration depends not only on the correct PROM decoder, but also on the correct setting of jumper plugs and some straps (the modification of straps is only required for some special memory configurations). The sockets 1 and 2 will accept 2 kbyte or 8 kbyte RAM's, dependent on the setting of jumper plug J3. With J3 in the position for 8 kbyte RAM's also 4 kbyte and 8 kbyte EPROM's can be used in these sockets (2732/2764 or equivalents). The sockets 3, 4 and 5 will also accept 2 kbyte or 8 kbyte RAM's dependent on the setting of jumper plug J2. With J2 in the position for 8 kbyte RAM's also 4 kbyte and 8 kbyte EPROM's can be used in these sockets. A strap "A" underneath each socket (3, 4 and 5), when removed and rewired to address line A13 will also allow the application of 16 kbyte EPROM's (27128 or equivalent) in these sockets. The straps can be removed with a sharp knife or equivalent tool.

With jumper J2 removed completely and the straps B, C and D underneath socket 6 rewired correctly, the sockets 3, 4, 5 and 6 will also accept low cost 2 kbyte EPROM's (2516/2716). In the latter case the sockets 3, 4 and 5 can only be modified as a group. If done, no other devices can be used in these sockets. Dependent on jumper plug J4, socket 6 will accept either 16 kbyte EPROM's or EPROM's ≤ 8 kbyte (2732/2764) in standard version. In the latter position also 8 kbyte RAM's can be applied. Moreover, dependent on additional modifications of the straps B, C and D, also 2 kbyte EPROM's (2716/2516) and 2 kbyte RAM's can be applied in this socket.

STANDARD MAP CONFIGURATION

(4C1/5C1)

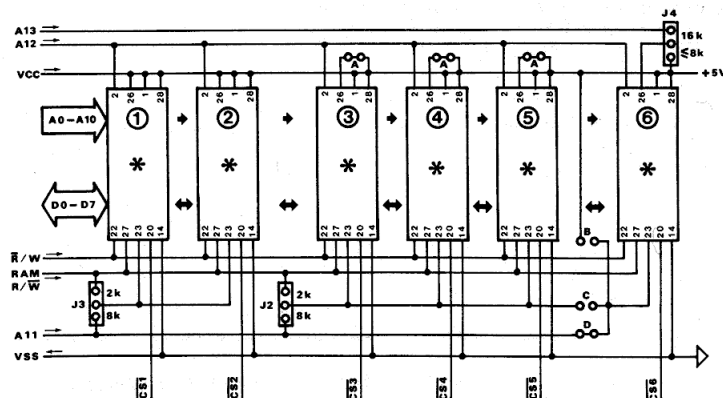


* (See page 2 for details)

B.E.M-SBC4C/SBC5C(M)

MEMORY DETAIL

* RAM or EPROM
(see text for details)



MEMORY IC SOCKET ALLOCATION TABLE

The table represented below shows all possible combinations together with the correct jumper settings and strap conditions. Note: except for the standard memory map configurations, each

custom configuration generally requires a special PROM decoder also. Please contact factory or nearest representative for details and cost.

SOCKET	RAM		EPROM				standard straps
	2 kbyte	8 kbyte	2 kbyte	4 kbyte	8 kbyte	16 kbyte	
1 & 2							
3, 4 & 5							
6							

Notes: If not specified, the standard strap configuration is assumed. Jumpers are drawn as seen at the component side of the printed circuit board, with the bus connector facing to the left. The table is represented for the B.E.M-SBC5C. The B.E.M-SBC4C shows minor differences. However, the same table can still be used. Standard straps A and D are located at the solder side of the print.

- ① Sockets 3, 4 and 5 only suitable for 2 kbyte EPROM's and only in combination with 2 kbyte EPROM in socket 6.
 ② Not very practical, but can only be used with the sockets 3, 4 and 5 also prepared for 2 kbyte RAM devices.

- ③ Strap A must be removed and the floating part (the solder spot not connected to VCC) must be rewired to address line A13 for each socket (3, 4 or 5) to accept 16 kbyte EPROM's.

MEMORY MAP CONFIGURATIONS

If not specified, the B.E.M-SBC4C and B.E.M-SBC5C will be delivered with the standard memory map configuration represented on page 1. The cards are provided with respectively a 4C1 and a 5C1 PROM decoder. However, the A and B memory map configurations as printed in the original B.E.M-SBC4A/B and B.E.M-SBC5A/B data sheets are also optionally available without additional cost. Just specify the required PROM decoder (4A1, 4B1, 5A1 or 5B1) with the order (e.g B.E.M-SBC5C + 5B1 PROM). NOTE: the Jumper settings (J2 → J4) for the C versions are not the same as for the A and B versions. Just follow the directions in the jumper table on this page.

With the standard PROM decoder, two different memory map's can be selected with J5. In case of map:1, the sockets 1 and 2 can only be used with 2 kbyte RAM devices. The other sockets will accept RAM or EPROM devices, dependent on jumper and/or strap settings as described before. Although, socket 6 is prepared to accept 16 kbyte EPROM devices, also 8 kbyte and 4 kbyte EPROM's can be used in this socket (depends on J4). However, if lower capacity EPROM's are applied, the EPROM field will appear not only at the top of the memory map, but also at several other echo locations within the decoded 16 kbyte field. Also in the case of map:2, if for instance a 4 kbyte EPROM is applied in socket 3. The EPROM field will appear at two locations within the decoded 8 kbyte field (the lower and upper 4 kbyte sections will be equal). Custom map configurations, within the technical limits of the cards (the same as the A and B versions) can be delivered at additional cost. Please contact factory or nearest representative for details.

MEMORY DEVICES

The following EPROM and RAM types can be applied with the B.E.M-SBC4C and B.E.M-SBC5C cards. This list is far from complete and must be considered as a guide only.

SUITABLE MEMORY TYPES		
RAM	2 kbyte	HM6116, HM6117, TMM2016, TC5516, TC5517, MB8416, NMC6116, μ PD446, MSM5128, HM6516
	8 kbyte	TC5564, TC5565, HM6264
EPROM	2 kbyte	TMS2516, TMM323, HN462716, 2716, μ PD2716
	4 kbyte	TMS2732, 2732, 2732A, TMM2732, HN462732, μ PD2732
	8kbyte	TMS2764, 2764, TMM2764, HN482764, μ PD2764
	16 kbyte	27128

NOTE: or equivalent types.

representatives:

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ALL CARDS ARE FULLY TESTED AND BURNED-IN BEFORE SHIPMENT