

GENERAL DESCRIPTION

The B.E.M-VIDEO-1, low cost VIDEO DISPLAY CONTROLLER CARD, is specially designed for character or block graphics based raster scan video display purposes. The CRT controller is used in the transparent addressing mode with screen updates during the horizontal and vertical blanking (retrace) times, enabling updating without visible screen perturbations.

The card is fully decoded and relocatable in steps of only 4 address locations throughout the entire 65 k address space. Because of the minor memory space required by this card, it will fit into the map of almost any system. Also applications with many B.E.M-VIDEO-1 cards combined into one system are possible.

Relocation control is achieved with one 2 st. and three 4 st. DIL switches (binary encoded), enabling the user to select any field of 4 address locations starting at \$XXXY (X = any HEX value 0 → F and Y = 0, 4, 8 or C).

The B.E.M-VIDEO-1 is specially designed with the SY-6545-1 CRT controller chip, manufactured by Synertek, because of its transparent addressing mode. The CRT controller also features fully programmable display parameters (rows, columns, blanking, etc.), fully programmable cursor, external light pen capability and external frame synchronization with other video systems or the mains frequency. Detailed description of the SY-6545-1 CRT controller chip is beyond the purpose of this datasheet. For more details, the original data sheet and application notes (AN3 and AN4) of the manufacturer (Synertek) are recommended.

In standard version, the card will be delivered with 2 kbyte RAM, sufficient to hold 2048 characters of text (e.g. 1 page of 25 lines with 80 characters per line, or 2 pages of 26 lines with 40 characters per line). However, the on-board RAM capacity can be doubled to 4 kbyte if necessary, simply by plugging another RAM device (e.g. TMM 2016) into the free socket available for this purpose.

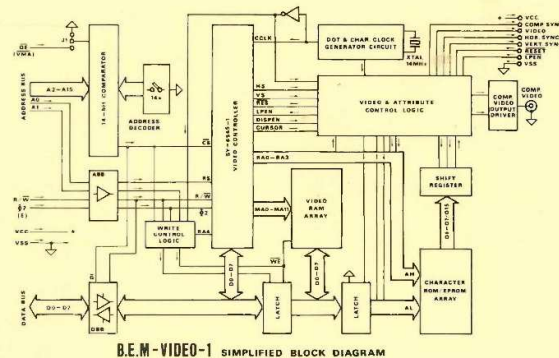
The B.E.M-VIDEO-1 can be applied with many different character formats, practically ranging from 5×7 to 16×16 dot matrix formats. To achieve this flexibility, the card is provided with two 24-pin

Continued on page 2.

FOR MICROPROCESSOR APPLICATIONS

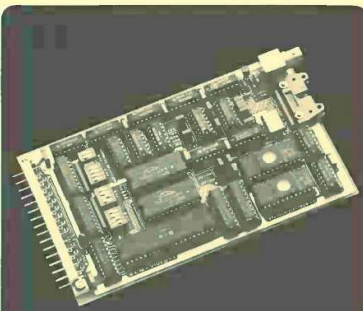
FEATURES

- GENERAL PURPOSE VIDEO CONTROLLER CARD FOR CHARACTER AND BLOCK GRAPHICS RASTER SCAN DISPLAY PURPOSES
- 1 MHz CRT CONTROLLER (SY-6545-1) IS STANDARD. 2 MHz VERSION IS OPTIONAL (SY-6545A-1)
- USES TRANSPARENT ADDRESSING MODE WITH BLANKING UPDATES
- FULLY DECODED AND RELOCATABLE IN STEPS OF ONLY 4 ADDRESS LOCATIONS THROUGHOUT THE ENTIRE 65K ADDRESS SPACE
- SINGLE (+5V) POWER SUPPLY REQUIRED
- UP TO 4K BYTE ON BOARD RAM (2K BYTE STANDARD)
- UP TO 4K WORDS (16-BIT) ON BOARD CHARACTER ROM/EPROM CAPACITY. 2K BYTE ROM WITH STANDARD CHARACTER SET (8×8 DOT MATRIX) IS STANDARD
- CUSTOM DESIGNED CHARACTER SETS ARE POSSIBLE
- MANY DIFFERENT CHARACTER FORMATS UP TO 16 × 16 DOT MATRIX CAN BE SELECTED (WITH APPROPRIATE CHARACTER ROM/EPROM)
- NUMBER OF CHARACTERS PER LINE AND NUMBER OF LINES PER PAGE CAN BE PROGRAMMED
- MANY JUMPERS (21) ARE AVAILABLE TO ADAPT THE CARD TO ALMOST ANY USER APPLICATION
- COMPOSITE VIDEO OUTPUT VIA RIGHT ANGLE BNC CONNECTOR
- 10-PIN FLAT CABLE HEADER FOR LIGHT PEN, RESET, VIDEO, HOR SYNC, VERT SYNC, COMP SYNC AND VCC/VSS POWER SUPPLY CONNECTIONS
- SUITABLE FOR 650X, 6800 AND 6809 BASED SYSTEMS
- ALL IC'S MOUNTED IN HIGH QUALITY MACHINE TOOLED SOCKETS
- GENEROUS OEM DISCOUNTS AVAILABLE



(MAIN) BUS CONNECTIONS

Pin	Function	Pin	Function	Pin	Function
1	N.C.	11	OE (VMA)*	21	A 8
2	VSS (GND.)	12	R/W	22	A 7
3	D 7	13	Φ 2 (E)	23	A 6
4	D 6	14	A 15	24	A 5
5	D 5	15	A 14	25	A 4
6	D 4	16	A 13	26	A 3
7	D 3	17	A 12	27	A 2
8	D 2	18	A 11	28	A 1
9	D 1	19	A 10	29	A 0
10	D 0	20	A 9	30	VCC (+ 5V)
				31	N.C.



Continued from page 1

sockets for character ROM purposes. Special attention has been given to allow the application of custom character sets programmed in EPROM (450 nsec access time minimum). Widely used 2 kbyte and 4 kbyte ROM's and EPROM's (2516/2716, 2532 or 2732) can be used. Only one ROM is necessary for character formats up to 8 dots wide. The second ROM is necessary only with character formats wider than 8 dots. In addition to the second ROM, also a second shift register will be necessary (a socket is available for this purpose). In standard version the B.E.M-VIDEO-1 will be delivered with a 2 kbyte character ROM containing 256 different characters and graphic symbols in an 8x8 dot matrix format (see page: 7 for details).

With reduced character set (128), the most significant data bit (D7) can be used for controlling attributes like blink and reverse video on character base. Jumpers are available to select the blink and or the reverse video mode on or off. In addition, reverse video can be selected for the whole screen. A separate jumper is available to select a blink frequency of approximately 1Hz or 0.5Hz synchronous to the frame frequency (irregular blink behaviour will be avoided). Which blink frequency will be selected is up to the user personal preference.

Two different dot frequencies can be selected with a jumper in standard version (14 MHz or 7 MHz). In combination with the standard character ROM this feature will allow the user to select 80 or 40 characters on a line. With other dot frequencies (dependent on basic crystal frequency) almost any format can be handled if required. The CRT controller is flexible enough but applicable dot frequencies, or more accurate, frame frequencies are limited by video monitor requirements (generally equal or close to the mains frequency).

The character width can theoretically be selected from 1 to 16 dots but in general character widths smaller than 6 dots will not be practical. Four jumpers are available to select any character width from 1 to 16 dots (the jumpers are binary encoded, see jumper tables on page: 9 for details). In addition one more jumper is necessary to select between character widths ≤ 8 dots or > 8 dots. Of course the character width selection can only be used in combination with an appropriate character ROM or EPROM.

The character height is also programmable. Theoretically also from 1 to 16 dots but in practice the minimum height will be limited to 7 dots. In combination with 4K character ROM's or EPROM's the full character set capability (256) can be combined with any character format within the limits of the B.E.M-VIDEO-1 card. However, with 2K character ROM's or EPROM's there are some limitations. The character set will be limited to 128 different symbols for character heights > 8 dots. However, with character heights ≤ 8 dots, it will be possible to select the full character set capability but without attributes (reverse video and blink features) or to select two different character sets (jumper selectable) of 128 symbols each, in combination with the use of the attributes (see jumper tables on page: 9 for details).

The composite video output signal is available via a right angle BNC connector (75 Ohm). The signal is conform the RS - 170 recommendations. Details can be found on page: 3. A 10-pin flat cable header located to the right of the BNC connector is used for all useful video control signals, including some lines for power supply connections (e.g. for a light pen circuit). All signal lines are terminated with a 1 K pull-up resistor. The output signals (horizontal sync., vertical sync., composite sync. and video) are available via TTL open-collector drivers. There are two input lines. One is used for the light pen and the other for reset purposes. The RESET line will mainly be used to synchronize the frame frequency of the B.E.M-VIDEO-1 to an external source.

Except for one jumper (J1) all jumpers are provided with jumper plugs for quick and simple modifications without soldering. All IC's are mounted in high quality machine tooled sockets. Low Power Schottky IC's are used where possible (in some critical sections Advanced Low Power Schottky devices are applied).

Custom designed character sets and non standard dot frequencies are possible. Please contact factory or nearest distributor for details.

Each B.E.M-VIDEO-1 card will be delivered with software examples written in 6502 and 6809 assembler language to simplify the user system integration.

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias	0°C to + 70°C
Storage Temperature	-55°C to + 120°C
Voltage on any Pin with respect to Ground	-0.3V to + 7V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the B.E.M-VIDEO-1 card. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

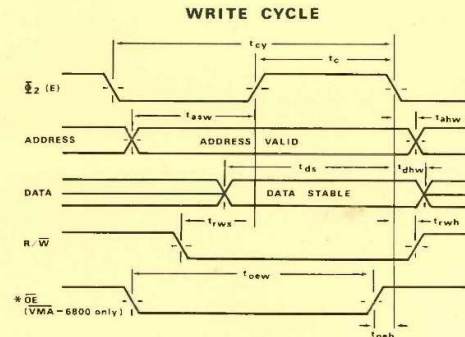
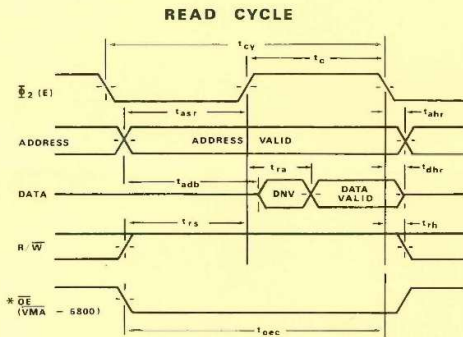
TA = 0°C to +70°C, VCC = +5V $\pm$ 5% (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
I _{LIH}	Input Load Current on any Bus Input Pin "High level"			20 100	μ A μ A	V _{IN} = 2.7 V V _{IN} = 7.0 V
I _{LIL}	Input Load Current on any Bus Input Pin "Low Level"			-400	μ A	V _{IN} = 0.4 V
I _{LD}	Leakage Current Data Bus Pins "Off State"			20 -200	μ A μ A	V _{IN} = 2.7 V V _{IN} = 0.4 V
I _{CC}	VCC Power Supply Current in Standard Version with 2 kbyte RAM and standard Character ROM (2 kbyte)		750	950	mA	VCC = 5.25 V TA = 0°C (worst case conditions)
V _{IL}	Input "Low" Voltage (any Bus Input Pin)	-0.5		0.8	V	
V _{IH}	Input "High" Voltage (any Bus Input Pin)	2		VCC	V	
V _{OL}	Output "Low" Voltage (Data Bus only)			0.5	V	I _{OL} = 24 mA
V _{OH}	Output "High" Voltage (Data Bus only)	2			V	I _{OH} = -15 mA
V _{VOL}	Video Control Output "Low" Voltage (V, HS, VS, CS)			0.4	V	I _{VCL} = 12 mA
V _{VOH}	Video Control Output "High" Voltage (V, HS, VS, CS)	2			V	I _{VCL} = 3 mA (1K Pull-up Resistor)
V _{VIL}	Video Control Input "Low" Voltage (RES, LPEN)	-0.5		0.8	V	(1K Pull-up Resistor)
V _{VIH}	Video Control Input "High" Voltage (RES, LPEN)	2		VCC	V	(1K Pull-up Resistor)

AC CHARACTERISTICS (Bus Timing only)

		SY-6545-1*		SY-6545A-1*					
Symbol		Parameter		Limits		Limits		Test Conditions	
				Min.	Max.	Unit	Min.		
READ CYCLE	t _{cy}	Total Clock Cycle Time Φ2 (E)		1000		nsec	500		Input pulse levels 0.8V to 2.4V. Input rise and fall times: 10 nsec. VCC = +5.0V TA = 0+ 70°C
	t _c	Φ2 (E) Clock Cycle High		440		nsec	200		
	t _{asr}	Address Set-Up Time		220		nsec	130		
	t _{ahr}	Address Hold Time		0		nsec	0		
	t _{ra}	Read Access Time			350	nsec		160	
	t _{rdh}	Read Data Hold Time		40		nsec	40		
	t _{adb}	Address to Data Bus Delay			70	nsec		70	
	t _{rs}	Read Set-Up Time		180		nsec	90		
	t _{rh}	Read Hold Time		0		nsec	0		
t _{oc}	OE (VMA) Low Time in respect to Φ2 (E) ↓		660		nsec	330		6800 mode only	
WRITE CYCLE	t _{cy}	Total Clock Cycle Time Φ2 (E)		1000		nsec	500		6800 mode only
	t _c	Φ2 (E) Clock Cycle High		440		nsec	200		
	t _{asw}	Address Set-Up Time		220		nsec	130		
	t _{ahw}	Address Hold Time		0		nsec	0		
	t _{rws}	Write Set-Up Time		180		nsec	90		
	t _{rwh}	Write Hold Time		0		nsec	0		
	t _{ds}	Data Set-Up Time		275		nsec	110		
	t _{dhw}	Data Hold Time		0		nsec	0		
	t _{sew}	OE (VMA) Set-Up Time in respect to Φ2 (E) ↓		660		nsec	330		
	t _{oeh}	OE (VMA) Rising Time before Φ2 (E) ↓			15	nsec		15	

* SY-6545-1 used in standard version (1 MHz), SY-6545A-1 is optional (2 MHz).



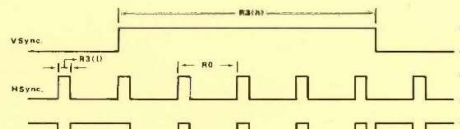
VIDEO CONTROL SIGNALS

The B.E.M-VIDEO-1 card is provided with a 10-pin flat cable header used in some unusual applications. All connections are summarized in the table to the right. In addition to the separated Sync. signals (Hor. Sync. and Vert. Sync.), required with some video monitor systems, also the composite sync. signal and the normal video signals will be available to the user. The timing and signal levels of Hor. Sync., Vert. Sync. and Comp. Sync. are represented in the drawing to the right. In respect to the video output signal, the black level is low and the white level is high.

The RES input is used to synchronize the B.E.M-VIDEO-1 card to an external source (frame only). For this application it will be necessary to program the CRT controller so, the frame frequency is somewhat lower than the external source. The LPEN input is used to connect a light pen. The input signal has been inverted (low is active). Detailed description on light pen requirements can be found in the original CRT controller data sheet. Finally, the +5V power supply connections (VCC and VSS) are also available through this connector, for instance to feed the light pen circuit or

VIDEO CONTROL HEADER CONNECTIONS

Pin	Symbol	Function
1	LPEN	Light Pen
2	RES	Reset Frame Sync.
3	VSS	Power Supply 0V
4	VS	Vertical Sync.
5	VSS	Power Supply 0V
6	HS	Horizontal Sync.
7	VSS	Power supply 0V
8	V	Video
9	VCC	Power Supply +5V
10	CS	Composite Sync.



RELOCATION CONTROL AND REGISTER ADDRESSES

The B.E.M-VIDEO-1 card occupies only four successive address locations and is also relocatable in steps of four locations throughout the entire 65K address space. Therefore, any card start address \$XXXY can be selected (X = 0 to F, all HEX values and Y = 0, 4, 8 or C).

Each X value can individually be selected with a 4 st. DIL switch (binary encoded, 1=1, 2=2, 3=4 and 4=8, ON=0 and OFF=1). A 2 st. DIL switch is used for the Y value (1=4 and 2=8, ON=0 and OFF=1). The table represented below, shows the relative card address functions.

Relative card address	Function	
	Read	Write
0	CRTC status register	CRTC address register
1	CRTC data register	CRTC data register
2	not used	CRTC address register + character latch
3	not used	CRTC data register + character latch

At the address locations 2 and 3, the same CRTC registers are accessed as at respectively 0 and 1, but with the additional function, that also the character latch can be written. Location 2 will normally not be used, but location 3 is required for correct transparent addressing operations (see "OPERATING THE B.E.M-VIDEO-1" on page: 5 for details).

Only the three most significant bits of the status register are used to monitor the status of the CRTC. The bits 0 to 4 are not used. The table below shows the functions of the most significant bits.

Bit	Function
5	0 = Scan not in vertical blanking portion of its timing 1 = Scan is in vertical blanking portion of its timing
6	Switches to 0 whenever R16 or R17 is read Switches to 1 if LPEN strobe occurs
7	Switches to 0 when R31 is read or written (NOT READY) Switches to 1 if update strobe (RA4) occurs (READY) See also "OPERATING THE B.E.M-VIDEO-1" on page: 5

Data written into the data register at location 1 is stored in the internal CRTC register selected by the CRTC address register. An internal CRTC register can only be accessed in two passes. First the CRTC address register at location 0 has to be loaded, followed by a write or read operation of the selected register at location 1.

The CRT Controller is provided with the following internal registers:

Reg. Addr.	Reg. No.	Register name	Type of info	Read/Write	Valid bits							
					7	6	5	4	3	2	1	0
0	R0	Horiz. total - 1	# characters	W	✓	✓	✓	✓	✓	✓	✓	✓
1	R1	Horiz. displayed	# characters	W	✓	✓	✓	✓	✓	✓	✓	✓
2	R2	Horiz. sync. pos	# characters	W	✓	✓	✓	✓	✓	✓	✓	✓
3	R3	Sync. width ①	#char/#lines	W	✓	✓	✓	✓	✓	✓	✓	✓
4	R4	Vert. total -1	# char. rows	W	x	✓	✓	✓	✓	✓	✓	
5	R5	Vert. adjust	# scan lines	W	x	x	x	✓	✓	✓	✓	✓
6	R6	Vert. displayed	# char. rows	W	x	✓	✓	✓	✓	✓	✓	✓
7	R7	Vert. sync. pos.	# char. rows	W	x	✓	✓	✓	✓	✓	✓	✓
8	R8	Mode control ②		W	✓	✓	✓	✓	✓	✓	✓	✓
9	R9	Scan lines - 1	# scan lines	W	x	x	x	✓	✓	✓	✓	✓
A	R10	Cursor start ③	Scan line no.	W	x	✓	✓	✓	✓	✓	✓	✓
B	R11	Cursor end ③	Scan line no.	W	x	x	x	✓	✓	✓	✓	✓
C	R12	Display start (H)		W	x	x	x	x	✓	✓	✓	✓
D	R13	Display start (L)		W	✓	✓	✓	✓	✓	✓	✓	✓
E	R14	Cursor pos. (H)		R+W	x	x	x	x	✓	✓	✓	✓
F	R15	Cursor pos. (L)		R+W	✓	✓	✓	✓	✓	✓	✓	✓
10	R16	Light pen reg (H)		R	x	x	x	x	✓	✓	✓	✓
11	R17	Light pen reg (L)		R	✓	✓	✓	✓	✓	✓	✓	✓
12	R18	Update addr. (H)		W	x	x	x	x	✓	✓	✓	✓
13	R19	Update addr. (L)		W	✓	✓	✓	✓	✓	✓	✓	✓
14 to 1E	R20 to R30	Not Used										
1F	R31	Dummy register ④		W	x	x	x	x	x	x	x	x

= number of, x = not used or don't care, ✓ = valid info.

NOTE: ① The least significant 4 bits contain the width of HSYNC in number of character clock (CCLK) cycles and the higher 4 bits contain the width of VSYNC in number of scan lines.

NOTE: ② The mode control register selects the operating mode of the CRT Controller. The function of the bits are as follows:

Bit	Function
0	Always 0
1	Scan mode, 0 = non-interface, 1 = interface
2	Video RAM addressing, 0 = straight binary 1 = row/column
3	Video RAM access, always 1 for this card
4	Display enable skew, always 1 for this card
5	Cursor skew, always 1 for this card
6	Update strobe, always 1 for this card
7	Update mode, always 0 for this card

Row/column addressing requires more RAM than is really necessary to store the required data (always 256 bytes for each line of characters on screen). Because only 4 Kbyte (2 Kbyte is standard) RAM is available in maximum configuration, the Row/column mode can only be used in combination with small screen formats (16 lines

of characters maximum). To profit the on board RAM capacity optimally, it is advised to use the straight binary addressing mode. In this mode, each byte of RAM can contain a character. However, the software will appear to be more complex than in the row/column mode.

NOTE: ③ The least significant 5 bits contain the scan line number where the cursor block starts. The shape of the cursor is determined by these bits in combination with the least significant 5 bits of R11. See also the notes on these registers in the section "CALCULATING THE CRTC REGISTER VALUES" on page: 6. Bit 5 and 6 are used to select the cursor mode in the following way:

Bit		Cursor mode
6	5	
0	0	Steady cursor
0	1	No cursor
1	0	Blinking at 1/16 field rate
1	1	Blinking at 1/32 field rate

NOTE: ④ The dummy register stores no data, but is required to detect when the transparent addressing update occurs. Normally this register will be selected via address location 3. See also "OPERATING THE B.E.M-VIDEO-1" for details.

COMPOSITE VIDEO OUTPUT SIGNAL

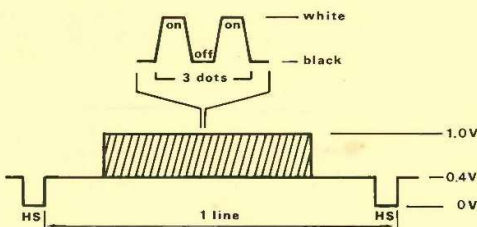
The composite video output signal as represented in the drawing to the right, is measured with a 75 Ohm load resistor. Only a single line is represented to show some important parameters.

Negative synchronisation is used with the lowest level at 0V (ground level). The black and white levels are respectively +0.4V and +1V (approximately).

The Horizontal and Vertical Sync. timing and blanking periods are fully programmable as been explained in the operational section of this data sheet and the original CRTC data sheet. So, the B.E.M-VIDEO-1 card can be adapted to almost any video monitor requirements.

The Dot period depends on the basic clock frequency and the

position of jumper J2. In the standard version (14MHz basic clock) the Dot period can be selected to be 70 nsec (at fo) or 140 nsec (at fo/2). Rise and fall time of the Dot signal are 20 nsec or shorter.



OPERATING THE B.E.M-VIDEO-1

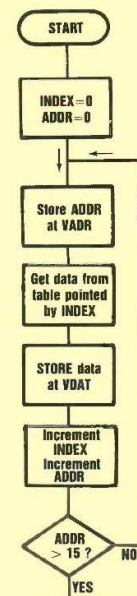
INITIATING THE SY-6545-1 CRT CONTROLLER

After POWER-ON/RESET, the internal registers of the CRTC must be set to their correct operating values. The contents of the registers R0 to R7 and R9 depend on the used frequencies (horizontal and vertical), the desired screen format and the used character size. The section "CALCULATING THE CRTC REGISTER VALUES" explains how to obtain the correct values for these registers. Register R8 must be set to \$78 for straight binary RAM addressing and, to \$7C for the row/column mode. Other values are not allowed for the B.E.M-VIDEO-1 card. Normally the registers R10 to R15 will be set to default values at INITIATE time. See the original SY-6545-1 data sheet for more details on these registers.

The following example shows the flow diagram of a general program, to load all internal registers (R0 - R15) of the CRTC. The data table must contain the values of the registers R0 to R15. VADR is the relative card address 0 and VDAT is the relative card address 1.

CALCULATING THE CRTC REGISTER VALUES

In the original SY-6545-1 datasheet the functions of the internal registers are explained. Here, two examples will demonstrate how to obtain the correct values. One example is for a screen format of 24 lines of 80 character and the second example is for a screen format of 24 lines of 40 characters. In both examples the standard EUROPEAN scan frequencies are assumed (64 µsec line time and 20 msec frame time) and the character format is 8 × 8 dots (standard character ROM). Also the calculations are for the 14 MHz standard crystal. J2 must be in the correct position (fo for the 24 × 80 mode and fo/2 for the 24 × 40 mode, see also jumper section on page: 9 for details).



Reg. No.	Parameter	Example 1	Example 2
R0	Dot time CCLK Hor.total	1 : fo = 71.4 nsec 8 x dot time = 571.2 nsec 64 : 5712 = 112 char. R0 = Hor.tot - 1 = 111 char.	1 : fo/2 = 142.9 nsec 8 x dot time = 1.143 μ sec 64 : 1.143 = 56 char. R0 = Hor.tot - 1 = 55 char.
R1	Hor. disp.	R1 = 80 char./ line	R1 = 40 char./ line
R2	Hor. Sync. position	R2 = 95 char.	R2 = 50 char.
		R2 depends on monitor and hor. position on screen ①	
R3	Sync. width	R3 = \$43	R3 = \$43
		R3 depends on monitor ②	
R4	Char.col.time Vert.total	8 x line time = 512 μ sec 20 000 : 512 = 39 char. R4 = Vert.tot - 1 = 38 char.	8 x line time = 512 μ sec also 39 char. R4 = Vert.tot - 1 = 38 char.
R5	Vertical adjust	R5 = 0 No adjust	R5 = 0 No adjust
		The exact frame time is 39 x 512 = 19 968 μ sec.	
R6	Vert. disp.	R6 = 24 char.	R6 = 24 char.
R7	Vert.Sync. position	R7 = 30 char.	R7 = 30 char.
		R7 depends on monitor and vertical position on screen ①	
R8	Mode contr.	R8 = \$78 Binary addr. mode	R8 = \$78 also binary addr.
R9	Char.height	R9 = 7 Char. = 8 dots high	R9 = 7 Char. = 8 dots high
R10	Cursor ①	R10 = 0 Cursor is steady	R10 = \$40 Blinking cursor
R11	Cursor ①	R11 = 7 Cursor 8 lines high	R11 = 6 Cursor 7 lines high

NOTE: ① The value in R2 determines the start of the horizontal sync. pulse, expressed in characters measured in respect to the first character on the line. The difference between R2 and R1 determines the blank period (expressed in characters) at the right side of the screen and the difference between R0 and R2 the blank period at the left side of the screen. The vertical sync. position (R7) is calculated in a similar way. The blank period at the top of the screen (expressed in number of vertical characters) is determined by the difference of R4 and R7 and the blank period at the bottom of the screen by the difference of R7 and R6.

NOTE: ② In the examples above, the value \$43 has been selected for R3. This is not an arbitrary value. The high Nibble (4) will take care, the vertical sync. width is 4 times the line time ($4 \times 64 \mu\text{sec} = 256 \mu\text{sec}$). The low Nibble (3) will guarantee that the horizontal sync. width will be 3 times the character clock time (1.71 μsec in example: 1 and 3.43 μsec in example: 2). Some video monitors require different values. However, R3 = \$43 will generally be suitable.

NOTE: ③ With R10 and R11, any cursor height can be programmed. The cursor can never be higher than the character height. The cursor can be shaped as a solid block within the limited space of a standard character. The width is equal to the character width. The height can range from a single line (1 dot high) to the maximum height of the character. Also the position of the cursor can start on any line within the limited space of the character.

R12 and R13 contain the display start address in RAM. The start address is the address of the first character on the first line (in the left high corner) of the screen. With these registers, scrolling on character base through the complete memory will be possible. R12 contains the higher part and R13 the lower part of the address.

R14 and R15 contain the cursor display address in RAM. This is the address, the cursor will appear on the screen, if that part of memory is displayed on the screen (the total memory capacity of the B.E.M-VIDEO-1 may exceed the display capability, so it is possible that the cursor address is pointing to an off-screen section). R14 contains the higher part and R15 the lower part of the address.

In a different approach it will also be possible to calculate a crystal frequency, starting with screen format, character size and scan frequencies. It is advised to take the number of displayed characters on a line not more than 80% of the horizontal total (R0).

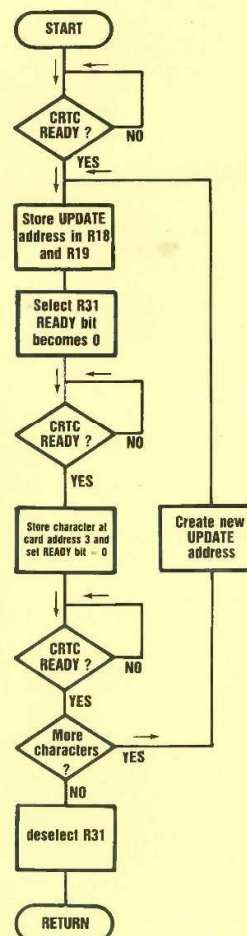
ERASING THE SCREEN

The screen will be erased by storing the blank character code (\$20 for the standard character ROM) in all Ram locations (or a part of it if more pages are available). The routine explained in "WRITING A CHARACTER TO RAM (SCREEN)" can be used for this purpose, calling this routine for all Ram locations to be cleared will do the job.

WRITING A CHARACTER TO RAM (SCREEN)

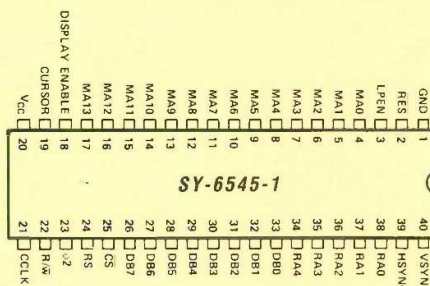
A character written in RAM does not always appear on the screen. It depends on the amount of RAM, the selected format and the contents of the registers R12 and R13 if the written location is on the screen.

The B.E.M-VIDEO-1 is designed for transparent addressing with updates during horizontal and vertical blank (retrace) periods. So, the UPDATE address registers (R18 and R19), the dummy register (R31) and the READY bit (bit 7) in the status register must be used to store one or more characters in RAM. The following procedure performs such a task:

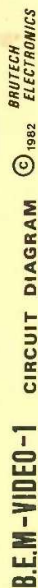


The drawing represented below, shows the standard character set delivered with each B.E.M-VIDEO-1. Bit 7 is assumed not to be used for attribute control. However, if bit 7 is used for attribute control the graphic symbol section can not be used in that case.

BRUTECH ELECTRONICS can deliver any character set (in EPROM) for the B.E.M.-VIDEO-1 to custom specifications within the limits of the B.E.M.-VIDEO-1 design (16x16 dot matrix maximum). Special design sheets are available for this purpose. Please contact factory for information on conditions and cost.

[illegible]

SY-6545-1 PIN LAY-OUT



JUMPERS

The B.E.M-VIDEO-1 card is provided with many jumpers (21), enabling the user to adapt this card to individual requirements. Except for J1, all jumpers are provided with jumper plugs for quick and simple modifications without the need to solder. A short list describing the jumper functions is represented below.

Jumper J1 is used to adapt the card to 6502, 6809 or 6800 based systems. In standard version J1 is strapped to ground for applications with 6502 and 6809 based systems. If applied with 6800 based systems, the strap has to be removed with a sharp knife or equivalent tool and rewired in the other position. J1 can be found just below the address switch for A15. The strap is located at the solder side of the printed circuit board.

All other jumpers are represented in the tables 1 to 5 arranged in logical groups. The position of the jumpers in the tables correspond to the positions at the component side of the printed circuit board.

The jumpers J2 and J3 are represented in table: 1. J2 is used to select the Dot frequency equal to f_0 (14 MHz) or $f_0/2$ (7 MHz). In the standard version f_0 is used for instance in applications with 80 characters on a line and $f_0/2$ for 40 characters on a line (this is only an example, the exact number of characters on a line can be programmed, see also the operational section of this data sheet and the original CRTIC data sheet for details). Jumper J3 is used to select the character Blink frequency (can be used only in combination with Blink attribute mode). The Blink frequency is synchronous with the frame frequency to guarantee regular blinking. Which Blink frequency will be selected is up to the user personal preference. NOTE: The Blink mode mentioned here is independent of the blinking of the cursor (the latter is programmable).

The jumpers J4 to J8 are used to select the character width in dots. The jumpers are represented in table: 2. Application

is useful only in combination with an appropriate character set. One character ROM (EPROM) is necessary for character widths up to 8 dots wide. Two ROM's (EPROM's) are necessary for character widths > 8 dots. In standard version the B.E.M-VIDEO-1 card will be delivered with a character ROM containing a character set (256 symbols) in 8×8 dot matrix. The standard character set is represented on page: 7. Custom designed character sets are possible up to 16×16 dot matrix formats. Special design sheets are available for this purpose. Please contact factory or nearest distributor for details. BRUTECH ELECTRONICS can deliver the B.E.M-VIDEO-1 with any character set (within the limits of the B.E.M-VIDEO-1 design) at additional cost (dependent on complexity and quantity).

The jumpers J9 to J13 as represented in table:3 are used for attribute selection (only hardware selectable attributes). Data bit 7 is used for attribute control. Only Blink or Reverse video or Blink + Reverse video can be selected on a character by character base. Except for the RAL mode (whole screen in reverse video) data bit 7 is used to control the attribute (1=ON, 0=OFF). So, the attributes can only be used with reduced character set (128).

The jumpers J14 to J17 as represented in table:4 are used to prepare the character ROM sockets for the proper EPROM type (or pin and function compatible ROM type). As the table shows, the most widely used 2K and 4K EPROM types can be applied. Special attention has been given to enable the application of EPROM's (450 nsec access time minimum) for character ROM purposes. This feature will allow the application of custom designed character sets, even in small quantities.

Finally the jumpers J18 to J21 as represented in table:5 are used to select the proper character ROM (EPROM) parameters in relation to the character height, character set and the application of attributes.

JUMPER TABLES

table:1

Miscellaneous functions	
J3 	Blink Frequency 1Hz
J3 	Blink Frequency 0.5 Hz
 J2	Dot Frequency f_0
 J2	Dot Frequency $f_0/2$ ($f_0 = 14\text{MHz}$, standard version)

table:2

	A	B	C	D	Character Width (Dots)	Char. ROM's
					1	1
					2	
					3	
					4	
					5	
					6	
					7	
					8	
					9	2
					10	
					11	
					12	
					13	
					14	
					15	
					16	

table:3

J9	J10	J11	J12	J13	Attribute selection	Data Bit:7	Char.set limits
					No Attributes	0/1	256
					Blink Mode	1= ON	128
					Reverse Video	1= ON	128
					Blink + Reverse Video	1= ON	128
					All Screen Reverse Video	0/1	256
					All Scr. Rev. Video + Blink	1= ON	128

Table: 4

J14	J15	J16	J17	Character EPROM Type ²	Pin Lay-Out ¹
				2716 / 2516 (2K)	Intel + T.I.
				2732 (4K)	Intel
				2532 (4K)	T.I.

¹ Intel and Texas Instr. are used for reference only.

² Or pin and functional compatible ROM's.

Table:5

J18	J19	J20	J21	Character Set Selection	ROM CAP.	ATTR.
				128 Char. Set > 8 Dots High	2K	YES
				128 Char. Set:1 ≤ 8 Dots High	2K ¹	YES
				128 Char. Set:2 ≤ 8 Dots High		
				128 Char. Set:1 > 8 Dots High	4K ¹	YES
				128 Char. Set:2 > 8 Dots High		
				256 Char. Set ≤ 8 Dots High	2K	NO ²
				256 Char. Set > 8 Dots High	4K	NO ²

¹ Two different character sets in one ROM/EPROM

GENERAL NOTES

1) In the circuit diagram on page 8, the numbers within a circle refer to the position of the IC's in the mechanical lay-out represented below.

2) For detailed description of the SY-6545-1 CRT controller, the original data sheet and application notes (AN3, AN4) of the manufacturer (Synertek) are recommended.

MECHANICAL SPECIFICATIONS

1) PRINTED CIRCUIT: 1.6 mm epoxy glass fiber reinforced in EURO CARD format (100 × 160 mm). Double sided metallized with plated through holes finally covered with an epoxy mask on both sides.

2) BUS CONNECTOR: 31-pin gold plated indirect connector (DIN 41617)

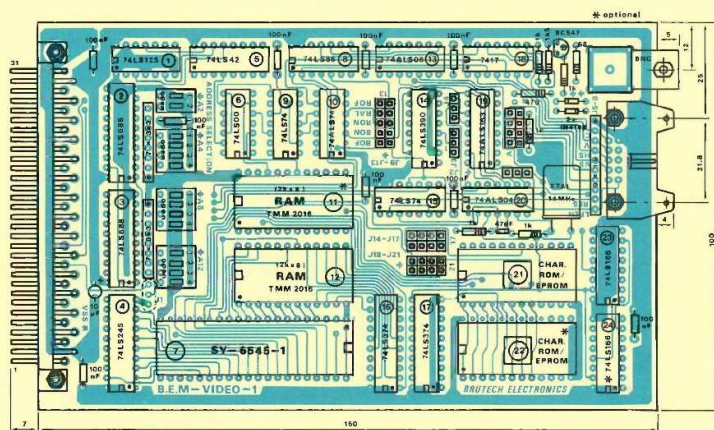
3) VIDEO CONTROL HEADER: 10-pin flat cable header accepting standard female socket connectors designed for flat cable with 0.05" (1.27 mm) conductor spacing.

4) BNC CONNECTOR: 75 Ohm right angle standard BNC connector

5) STANDARD version with high quality machine tooled sockets

6) MAXIMUM THICKNESS
All versions: 18.8 mm
Solder side: - 2.0 mm
Component side: +15.0 mm

MECHANICAL LAY-OUT (dimensions in mm)



representatives:

**BRUTECH
ELECTRONICS**
P.O. Box 58
3645 ZK Vinkeveen
Telex: 18576 BEMIN
The Netherlands



```

0010 0200      ;
0020 0200      ;
0021 0200      ;*****
0022 0200      ;*
0030 0200      ;* Program example for the B.E.M-VIDEO-1 WRITTEN *
0031 0200      ;* IN 6502 ASSEMBLER LANGUAGE.
0032 0200      ;* CARD START ADDRESS $C500
0033 0200      ;*
0034 0200      ;*****
0040 0200      ;
0050 0200      ;
0060 0200      ; EQUATES
0070 0200      ;
0080 0200      VADR  = $C500 ;ADDRESS/STATUS REGISTER CRTC
0090 0200      VDAT  = VADR+1 ;DATA REGISTER OF CRTC
0100 0200      VLAT  = VADR+3 ;DATA REGISTER + CHAR. LATCH
0110 0200      ;
0120 0200      ;VARIABLE STORAGE
0130 0200      ;
0140 0200      ;      *=0
0150 0000      COL   *=*+1      ;COLUMN NUMBER
0160 0001      ROW   *=*+1      ;ROW NUMBER
0170 0002      VACT  *=*+2      ;ACTUAL RAM ADDRESS
0180 0004      TEMP  *=*+2      ;TEMP. STORAGE
0190 0006      CODE  *=*+1      ;TEMP. STORAGE
0200 0007      .OPT GEN

```

```

0220 0007      ;PROGRAM START
0230 0007      ;
0240 0007      ;      *=$200
0250 0200 D8      START  CLD
0260 0201 20 76 02 JSR INIVID      ;INITIATE B.E.M-VIDEO-1
0270 0204 20 99 02 JSR CLRRAM      ;CLEAR RAM (SCREEN)
0280 0207      ;
0290 0207      ;
0300 0207      ; WRITE COMPLETE CHARACTER SET
0310 0207      ;
0320 0207      ;
0330 0207 A9 00      LDA #0
0340 0209 85 06      STA CODE      ;START CODE
0350 020B A9 04      LDA #4
0360 020D 85 01      STA ROW      ;START ROW
0370 020F A9 0C      NEXT1 LDA #12 ;USE 32 FOR 80 CHAR
0380 0211 85 00      STA COL      ;START COLUMN OF EACH ROW
0390 0213 A2 10      LDX #16      ;16 CHARACTERS / ROW
0400 0215 20 DE 02   NEXT2 JSR CALCVA ;CALCULATE VACT
0410 0218 A5 06      LDA CODE      ;GET CODE
0420 021A 20 B0 02   JSR WRITE      ;WRITE CHARACTER TO RAM
0430 021D E6 06      INC CODE      ;NEXT CODE
0440 021F F0 0A      BEQ READY      ;ALL DONE
0450 0221 E6 00      INC COL      ;NEXT COLUMN IN ROW

```

```

0460 0223 CA          DEX          ;16 DONE?
0470 0224 D0 EF      BNE NEXT2     ;NO
0480 0226 E6 01      INC ROW       ;NEXT ROW
0490 0228 4C 0F 02   JMP NEXT1     ;LOOP FOR NEXT ROW
0500 022B           ;
0510 022B           ; READY      ;256 CHARACTERS WRITTEN
0520 022B           ;
0530 022B           ;
0540 022B A9 0A      LDA #10       ;CURSOR START/MODE
0550 022D 8D 00 C5   STA VADR      ;SELECT R10
0560 0230 AD 01 C5   LDA VDAT      ;GET DATA
0570 0233 09 60      ORA #$60      ;SET BLINK MODE
0580 0235 8D 01 C5   STA VDAT      ;CURSOR IN BLINK MODE
0590 0238           ;CURSOR STILL AT ADDRESS 0
0600 0238           ;
0610 0238           ;
0620 0238           ; WRITE MESSAGE AT SECOND ROW
0630 0238           ;
0640 0238           ;
0650 0238 A9 01      LDA #1
0660 023A 85 00      STA COL        ;SECOND COLUMN
0670 023C 85 01      STA ROW        ;SECOND ROW
0680 023E 20 DE 02   JSR CALCVA     ;CALCULATE VACT
0690 0241 20 15 03   JSR SETCUR     ;MOVE CURSOR TO THIS POSITION
0700 0244 A0 00      LDY #0
0710 0246 B9 52 02   MES1 LDA MESTAB,Y ;GET CHARACTER
0720 0249 F0 06      BEQ MESRDY     ;END OF MESSAGE
0730 024B 20 2A 03   JSR WRTINC     ;WRITE CHAR. + UPDATE CURSOR
0740 024E C8        INY
0750 024F D0 F5      BNE MES1       ;NEXT CHARACTER
0760 0251           MESRDY         ;DONE
0770 0251           ;
0780 0251 00        BRK
0790 0252           ;
0800 0252           ;
0810 0252 42 2E 45   MESTAB .BYTE 'B.E.M-VIDEO-1 Example 24 x 40 lines',0
0810 0255 2E 4D 2D
0810 0258 56 49 44
0810 025B 45 4F 2D
0810 025E 31 20 45
0810 0261 78 61 6D
0810 0264 70 6C 65
0810 0267 20 32 34
0810 026A 20 78 20
0810 026D 34 30 20
0810 0270 6C 69 6E
0810 0273 65 73 00
0820 0276           ;
0830 0276           ; FOR 24 X 80 FORMAT, CHANGE 40 TO 80

0850 0276           ; INITIATE B.E.M-VIDEO-1 FOR 24 X 40
0860 0276           ; CURSOR OFF AT ADDRESS 0

```

```

0870 0276          ; DISPLAY START AT ADDRESS 0
0880 0276          ;
0890 0276 A0 10     INIVID LDY #16          ;16 REGISTERS TO BE WRITTEN
0900 0278 A2 00     LDX #0                ;START AT REGISTER 0
0910 027A 8A        INIVI1 TXA            ;REGISTER NUMBER
0920 027B 8D 00 C5   STA VADR             ;SELECT IT
0930 027E BD 89 02   LDA INITAB,X         ;GET REGISTER CONTENTS
0940 0281 8D 01 C5   STA VDAT            ;STORE IT IN CRTC
0950 0284 E8        INX                  ;NEXT REGISTER NUMBER
0960 0285 88        DEY                  ;READY?
0970 0286 D0 F2     BNE INIVI1           ;NO
0980 0288 60        RTS
0990 0289          ;
1000 0289          ;
1010 0289          ; TABLE WITH REGISTER VALUES FOR 24 X 40
1020 0289          ;
1030 0289 37 28 30   INITAB .BYTE 55,40,48,$43,38,0,24,30,$78,7,$20,7
1030 028C 43 26 00
1030 028F 18 1E 78
1030 0292 07 20 07
1040 0295 00 00 00   .BYTE 0,0,0,0
040 0298 00
1050 0299          ;
1060 0299          ; FOR THE 24 X 80 FORMAT CHANGE THE FIRST 3 VALUES
1070 0299          ; TO RESPECTIVELY 111, 80 AND 95.
1080 0299          ; ALL OTHER VALUES REMAIN UNCHANGED
1090 0299          ;

```

```

1110 0299          ; CLEAR RAM
1120 0299          ; THIS ROUTINE CLEARS 8 PAGES (2 K RAM)
1130 0299          ; CODE $20 (BLANK) WILL BE WRITTEN TO ALL LOCATIONS
1140 0299          ;
1150 0299 A9 00     CLRRAM LDA #0
1160 029B 85 02     STA VACT
1170 029D 85 03     STA VACT+1
1180 029F A0 08     LDY #8                ;8 PAGES
1190 02A1 A9 20     CLRRA1 LDA #$20       ;BLANK CODE
1200 02A3 20 B0 02   JSR WRITE           ;WRITE TO RAM
1210 02A6 E6 02     INC VACT             ;NEXT LOCATION
1220 02A8 D0 F7     BNE CLRRA1
1230 02AA E6 03     INC VACT+1           ;HIGH BYTE
1240 02AC 88        DEY                  ;READY?
1250 02AD D0 F2     BNE CLRRA1           ;NO
1260 02AF 60        RTS

```

```

1280 02B0          ; WRITE CONTENT OF ACCUMULATOR TO RAM
1290 02B0          ; VACT CONTAINS ADDRESS IN RAM
1300 02B0          ;

```

```

1310 02B0 48          WRITE PHA          ;SAVE CODE
1320 02B1 A9 12          LDA #18
1330 02B3 8D 00 C5      STA VADR          ;SELECT UPDATE ADDRESS H
1340 02B6 A5 03          LDA VACT+1      ;GET HIGH PART OF ADDRESS
1350 02B8 8D 01 C5      STA VDAT          ;STORE IT
1360 02BB A9 13          LDA #19
1370 02BD 8D 00 C5      STA VADR          ;SELECT UPDATE ADDRESS L
1380 02C0 A5 02          LDA VACT          ;GET LOW PART OF ADDRESS
1390 02C2 8D 01 C5      STA VDAT          ;STORE IT
1400 02C5 A9 1F          LDA #31
1410 02C7 8D 00 C5      STA VADR          ;SELECT R31
1420 02CA AD 00 C5      WRITE1 LDA VADR    ;STATUS
1430 02CD 10 FB          BPL WRITE1      ;NOT READY
1440 02CF 68            PLA              ;GET CODE
1450 02D0 8D 03 C5      STA VLAT          ;WRITE LATCH
1460 02D3 AD 00 C5      WRITE2 LDA VADR    ;STATUS
1470 02D6 10 FB          BPL WRITE2      ;NOT DONE
1480 02D8 A9 12          LDA #18
1490 02DA 8D 00 C5      STA VADR          ;DESELECT R31
1500 02DD 60            RTS

```

```

1520 02DE          ; CALCULATE VACT
1530 02DE          ; VACT = ROW * 40 + COL
1540 02DE          ;
1550 02DE A9 00      CALCVA LDA #0
1560 02E0 85 03      STA VACT+1          ;INI HIGH PART OF ADDRESS
1570 02E2 98          TYA
1580 02E3 48          PHA
1590 02E4 A0 03      LDY #3              ; ROW * 8
1600 02E6 A5 01      LDA ROW
1610 02E8 0A          CALC1 ASL A
1620 02E9 26 03      ROL VACT+1
1630 02EB 88          DEY
1640 02EC D0 FA      BNE CALC1
1650 02EE 85 04      STA TEMP          ;SAVE RESULT (8 * ROW)
1660 02F0 A5 03      LDA VACT+1
1670 02F2 85 05      STA TEMP+1
1680 02F4 A5 04      LDA TEMP
1690 02F6 0A          ASL A
1700 02F7 26 03      ROL VACT+1          ;* 16
1710 02F9 0A          ASL A
1720 02FA 26 03      ROL VACT+1          ;* 32
1730 02FC 65 04      ADC TEMP
1740 02FE 85 02      STA VACT
1750 0300 A5 03      LDA VACT+1
1760 0302 65 05      ADC TEMP+1
1770 0304 85 03      STA VACT+1          ;ROW * 40
1780 0306          ;
1790 0306          ; ONLY FOR 80 CHAR/LINE THE NEXT 2 INSTRUCTIONS
1800 0306          ; ASL VACT
1810 0306          ; ROL VACT+1
1820 0306 A5 02      LDA VACT

```

```

1830 0308 65 00      ADC COL
1840 030A 85 02      STA VACT
1850 030C A5 03      LDA VACT+1
1860 030E 69 00      ADC #0
1870 0310 85 03      STA VACT+1      ;ROW * 40 + COL
1880 0312 68         PLA
1890 0313 A8         TAY
1900 0314 60         RTS

```

```

1920 0315           ; SET CURSOR TO VACT
1930 0315           ;
1940 0315 A9 0E     SETCUR LDA #14
1950 0317 8D 00 C5  STA VADR      ;CURSOR ADDRESS H
1960 031A A5 03     LDA VACT+1    ;RAM ADDRESS HIGH PART
1970 031C 8D 01 C5  STA VDAT
1980 031F A9 0F     LDA #15
1990 0321 8D 00 C5  STA VADR      ;CURSOR ADDRESS L
2000 0324 A5 02     LDA VACT      ;RAM ADDRESS LOW PART
2010 0326 8D 01 C5  STA VDAT     ;CURSOR SET NOW
2020 0329 60         RTS

```

```

2040 032A           ; WRITE ACCUMULATOR TO RAM
2050 032A           ; VACT POINTS TO ADDRESS IN RAM
2060 032A           ; INCREMENT COL NUMBER, IF RESULT >=40
2070 032A           ; THEN COL=0 AND ROW=ROW+1
2080 032A           ; CALCULATE NEW VACT AND SET CURSOR TO IT
2090 032A           ;
2100 032A 20 B0 02  WRTINC JSR WRITE
2110 032D E6 00     INC COL
2120 032F A5 00     LDA COL      ;GET NEW COLUMN POSITION
2130 0331 C9 28     CMP #40     ;USE 80 FOR 80 CHAR.
2140 0333 90 10     BCC WRTIN1   ;NO LINE OVERFLOW
2150 0335 A9 00     LDA #0
2160 0337 85 00     STA COL
2170 0339 E6 01     INC ROW
2180 033B A5 01     LDA ROW      ;GET NEW ROW POSITION
2190 033D C9 18     CMP #24
2200 033F 90 04     BCC WRTIN1   ;NO SCREEN OVERFLOW
2210 0341 A9 00     LDA #0
2220 0343 85 01     STA ROW
2230 0345 20 DE 02  WRTIN1 JSR CALCVA ;CALCULATE VACT
2240 0348 4C 15 03  JMP SETCUR   ;SET CURSOR
2250 034B           .END
END OF ASSEMBLY
TOTAL ERRORS = 0000 <0000>

```

CALC1	02E8	CALCVA	02DE	CLRRA1	02A1	CLRRAM	0299
CODE	0006	COL	0000	INITAB	0289	INIVI1	027A
INIVID	0276	MES1	0246	MESRDY	0251	MESTAB	0252
NEXT1	020F	NEXT2	0215	READY	022B	ROW	0001
SETCUR	0315	START	0200	TEMP	0004	VACT	0002
VADR	C500	VDAT	C501	VLAT	C503	WRITE	02B0
WRITE1	02CA	WRITE2	02D3	WRTIN1	0345	WRTINC	032A