



**BRUTECH
ELECTRONICS**

P.O. Box: 58 Vinkeveen
The Netherlands

B.E.M.-MON-1

LOW COST MONITOR COMBI CARD

(HARDWARE DESCRIPTION)

GENERAL DESCRIPTION

The BEM-MON-1 MONITOR COMBI CARD is specially designed to be used in combination with the BEM-CPU-1 CENTRAL PROCESSOR CARD. This combination can be used either in stand-alone applications (minimum system configuration) or as a base configuration in highly sophisticated systems. Special attention has been given to allow maximum flexibility in user applications.

The MON-1 circuitry can be divided into 5 major sections. Referring to the block diagram these sections are respectively from left to the right:

1) The Bus Buffer Section:

All bus lines are buffered. The data bus is provided with bi-directional buffers. Control logic on card will avoid writing to ROM and EPROM fields.

2) The RAM Array:

The MON-1 is provided with a 2K byte RAM Array divided into 2 blocks of 1K byte each. In standard version the MON-1 will be delivered with 1K byte of RAM located from \$0000 - \$03FF (including the essential pages 0 and 1). Sockets for one more 1K byte of RAM located from \$0400 - \$07FF will make on board expansion very simple. On request the MON-1 can be delivered with 2K byte of RAM fully tested and burned-in.

3) The EPROM Array:

The MON-1 is provided with sockets for two EPROM's of the 2708 type or pin compatible PROM's/ROM's. Decoding is fixed. EPROM "1" is located from \$0800 - \$0BFF, EPROM "2" from \$0C00 - \$0FFF.

4) The 6530-004 Multi function Chip with Decoder and Control Logic:

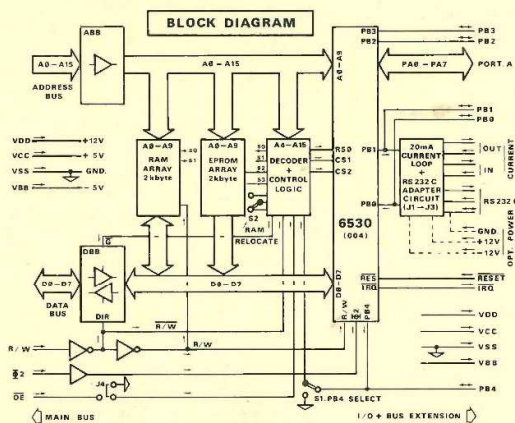
The 6530-004 IC is combining 4 devices in one Chip. Decoder and Control Logic take care all devices are decoded unique enabling the user to expand the system till the last byte.

"Continued on page 2"

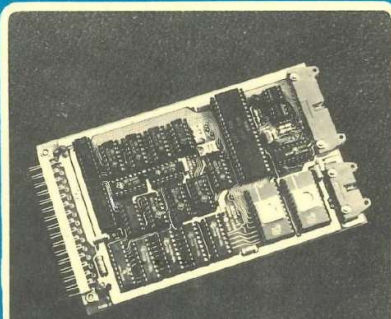
FOR MICROPROCESSOR APPLICATIONS

FEATURES

- * LOW COST MONITOR COMBI CARD
- * STANDARD VERSION WITH 1K BYTE RAM
- * SOCKETS FOR 1K BYTE RAM EXPANSION
- * SOCKETS FOR 2K BYTE EPROM (2 X 2708) EXPANSION
- * 1K BYTE DEBUG MONITOR (TIM) IN ROM
- * 64 BYTES RELOCATABLE RAM
- * PROGRAMMABLE TIMER
- * 13 PROGRAMMABLE I/O LINES IN TOTAL
- * RS 232 C INTERFACE WITH OPTO COUPLERS
- * 20 mA CURRENT LOOP INTERFACE WITH OPTO COUPLERS
- * 8 BIT HIGH SPEED PARALLEL INPUT PORT WITH HANDSHAKE
- * FULLY BUFFERED BUS STRUCTURE
- * FULLY DECODED SYSTEM FOR MAXIMUM EXPANSION CAPABILITIES
- * ALL IC's (LOW POWER SCHOTTKY) MOUNTED IN SOCKETS
- * GENEROUS OEM DISCOUNTS AVAILABLE



BEM - BUS - COMPATIBLE



(MAIN) BUS CONNECTIONS

Pin	Function	Pin	Function	Pin	Function
1	VBB -5V	11	OE *	21	A 8
2	VSS GND	12	R/W	22	A 7
3	D 7	13	Φ 2	23	A 6
4	D 6	14	A 15	24	A 5
5	D 5	15	A 14	25	A 4
6	D 4	16	A 13	26	A 3
7	D 3	17	A 12	27	A 2
8	D 2	18	A 11	28	A 1
9	D 1	19	A 10	29	A 0
10	D 0	20	A 9	30	VCC + 5V

GENERAL DESCRIPTION (continued)

The discrete functions of the 6530 (004) device are respectively:

4-1) A 1K byte ROM containing the small but powerful TIM* PROGRAM (TIM = Terminal Interface Monitor). The ROM is normally located from \$7000 - \$73FF. However, during start-up procedure only, the ROM field is copied to the top of the Memory Map enabling the processor to fetch the Monitor program start address (RESET Vector). Copy mode is controlled by I/O line PB4 and can be switched off with control switch S1 (PB4 select switch).

In the "Off" position the user has to supply its own Vectors, for instance burned into the PROM on the CPU-1 Central Processor Card (see datasheet for more details). This important feature will enable the user to start-up the system pointing directly to the user program (TURN KEY SYSTEM).

4-2) A 64 byte relocatable RAM field. Using control switch S2 (RAM Relocate Switch) the RAM field can be positioned at two different locations. In the low position (●) the RAM field is located from \$6FC0 - \$6FFF (direct under Monitor ROM field). In the high position (●●) the RAM field is located from \$FFC0 - \$FFFF (Top of Map).

If the system is used under Monitor control (S1 = ON) the RAM field has to be located high. During the initialize procedure the top 8 locations of the Monitor ROM field containing the TIM Vectors will be copied to RAM (the top 8 locations of the Memory Map). Because all Vectors are in RAM now they can be modified under Monitor control.

Especially the IRQ, NMI and User IRQ Vectors can be modified to point to user routines (more details will be found in software description of TIM).

If the system is initialized under User Program Control (e.g. user supplied Vectors in PROM) the 64 byte RAM field will normally be located in the low position.

4-3) A PIA (Peripheral Interface Adapter). In general the 6530 Multi function chip is supplied with 16 Programmable I/O pins divided into 2 - 8 bit PORTS, PA0 - PA7 and PB0 - PB7. However, due to Mask options (6530-004) PB5 and PB6 are not accessible to the user. These pins are used for decoding purposes (CS1, CS2).

PB7 is connected to the IRQ line of the BUS EXTENSION HEADER. Normally PB7 will be used to generate Timer controlled interrupts (SEE: 4-4 for more details).

If used for interrupt purposes PB7 has to be defined as an input. However, if the interrupt feature is not used the user can profit PB7 for I/O purposes.

The strap on the MON-1 Card between 2 holes near pin 2 of the BUS EXTENSION HEADER has to be removed for instance with a sharp knife. The connection can be restored later with a jumper if necessary. Under Monitor control all other I/O lines are dedicated to the Monitor.

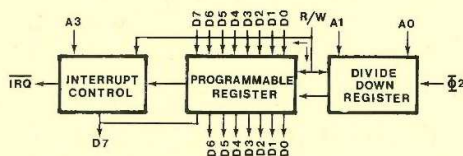
All lines of PORT A for instance are used as 8 bit parallel input port for the high speed paper tape reader option together with PB2 and PB3 as handshake signals.

As mentioned before PB4 is used to control ROM copy mode. PB1 and PB0 are used as output and input for the terminal interface circuit. Under user program control most I/O lines can be redefined.

Each PORT is controlled by two internal registers, the Data Direction Register and the Peripheral I/O Register. To define inputs and outputs the DDR has to be written first (1 = output, 0 = input). After I/O definition the user is able to write and read data to and from the data pins. This can only be done at the address of the Peripheral Register. Data is only written to those lines defined as outputs.

During a read operation the microprocessor is not reading the I/O Registers but in fact is reading the Peripheral Data pins. For those Peripheral Data pins which are programmed as outputs the microprocessor will read the corresponding data bits of the I/O Register.

4-4) A Programmable Interval Timer. The Timer section of the 6530 as illustrated below contains three basic parts: preliminary divide down register, programmable 8-bit register and interrupt logic.



The interval timer can be programmed to count up to 256 time intervals. Each time interval can be either 1T, 8T, 64T or 1024T increments, where T is the system clock period. When a full count is reached, an interrupt flag is set to a logic "1". After the interrupt flag is set the internal clock begins counting down to a maximum of -255T. Thus, after the interrupt flag is set, a Read of the timer will tell how long since the flag was set up to a maximum of 255T.

The 8 bit system Data Bus is used to transfer data to and from the Interval Timer. If a count of 52 time intervals were to be counted, the pattern 0 0 1 1 0 1 0 0 would be put on the Data Bus and written into the Interval Time register.

At the same time data is being written to the Interval Timer, the counting intervals of 1, 8, 64, 1024T are decoded from address lines A0 and A1. During a Read or Write operation address line A3 controls the interrupt capability of PB7, i.e., A3 = 1 enables IRQ on PB7, A3 = 0 disables IRQ on PB7. When PB7 is to be used as an interrupt flag with the Interval Timer it should be programmed as an input. If PB7 is enabled by A3 and an interrupt occurs PB7 will go low. When the timer is read prior to the interrupt flag being set, the number of time intervals remaining will be read, i.e., 51, 50, 49, etc.

When the timer has counted down to 0 0 0 0 0 0 0 0 on the next count time an interrupt will occur and the counter will read 1 1 1 1 1 1 1 1. After interrupt, the timer register decrements at a divide by "1" rate of the system clock. If after interrupt, the timer is read and a value of 1 1 1 0 0 1 0 0 is read, the time since interrupt is 28T. The value read is in two's complement.

Value read = 1 1 1 0 0 1 0 0

Complement = 0 0 0 1 1 0 1 1

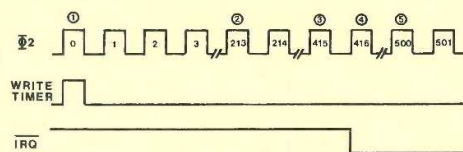
ADD 1 = 0 0 0 1 1 1 0 0 = 28.

Thus, to arrive at the total elapsed time, merely do a two's complement add to the original time written into the timer. Again, assume time written as 0 0 1 1 0 1 0 0 (=52). With a divide by 8, total time to interrupt is $(52 \times 8) + 1 = 417T$. Total elapsed time would be $416T + 28T = 444T$, assuming the value read after interrupt was 1 1 1 0 0 1 0 0.

After the interrupt, whenever the timer is written or read the interrupt is reset. However, the reading of the timer at the same time the interrupt occurs will not reset the interrupt flag. When the interrupt flag is read on DB7 all other DB outputs (DB0 thru DB6) go to "0".

When reading the timer after an interrupt, A3 should be low to disable the IRQ pin. This is done to avoid future interrupts until after an

The illustration below shows an example of interrupt.



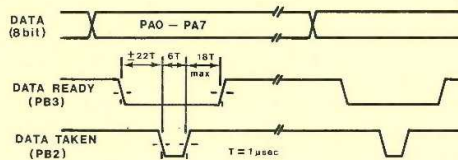
1. Data written into interval timer is $00110100 = 52_{10}$
2. Data in Interval timer is $00011001 = 25_{10}$
 $52 - \frac{213}{8} = 52.261 = 25$
3. Data in Interval timer is $00000000 = 0_{10}$
 $52 - \frac{415}{8} = 52.511 = 0$
4. Interrupt has occurred at $\frac{415}{8}$ pulse #416
Data in Interval timer = 11111111
5. Data in Interval timer is 11011100
two's complement is $01010100 = 84_{10}$
 $84 + (52 \times 8) = 500_{10}$

5) The I/O Interface Section:

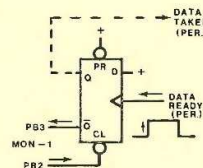
As mentioned before (SEE: 4-3) all PIA I/O lines are normally dedicated to the Monitor. In this section some interface details are discussed.

5-1) The high speed parallel input port can be used to connect for instance a high speed paper tape reader. See Monitor instruction summary for entering the high speed read mode. PORT A is used as input for the 8-bit word (PA0 = LSB, PA7 = MSB). PB3 and PB2 are used for handshake control. The peripheral has to generate a Data Ready Signal (low = ready). Within 22 μ sec data has been read by the system, acknowledged by generating a Data Taken pulse (about 6 μ sec long).

The Data Ready Signal must return to a high level within 18 μ sec after the Data Taken pulse, otherwise there is a chance the character will be read twice. The timing diagram shows the interface signals.



A suggested handshake control circuit profiting a "D" type flip flop (e.g. 74LS74) to avoid multiple character reading is represented to the right.



5-2) Interface logic on the MON-1 Card will enable the user to connect a TTY or CRT Terminal in full duplex mode. Opto-couplers are used for isolation. However, to profit the use of opto-couplers completely, the user has to connect an external power supply (+12V).

The jumpers J1, J2 and J3 will enable the user to select between an external supply and the internal system supply. In less critical applications the internal supply connection can be used. However, the application of opto-couplers in that case is dubious.

A 20 mA current loop as well as a RS 232 C interface circuit will enable the user to connect almost any terminal. TIM software will take care of Baud Rate. Any Baud Rate between 100 and 300 Baud will suit. After POWER-ON-RESET and initialize procedure the system will wait for the first character input from the terminal. The first character must be a return (CR). TIM will determine the Baud Rate from this character and will be locked to it till the RESET procedure is repeated. It is possible to connect two peripherals at the same time for instance a CRT connected to the RS 232 C interface and a printer to the current loop circuit (ofcourse the Baud Rate must be equal). It is not advised to connect two input devices at the same time. For more details we refer to the circuit diagram and the jumper section.

BUS EXTENSION HEADER

Pin	Function
1	RESET
2	IRQ
3	N.C.
4	N.C.
5	N.C.
6	N.C.
7	N.C.
8	N.C.
9	N.C.
10	N.C.

I/O HEADER

Pin	Function
1	VBB, System -5V
2	-12V EXT. Supply
3	20 mA Current Loop OUT
4	EXT. GND. / RS 232-C (Common)
5	RS 232-C INPUT
6	RS 232-C OUTPUT
7	20 mA Current Loop IN
8	+12V EXT. Supply
9	20 mA Current Loop IN (Return)
10	20 mA Current Loop OUT (Return)
11	VDD, System +12V
12	PB 0
13	PB 1

Pin	Function
14	PB 4
15	VCC, System +5V
16	PB 2 Data Taken
17	PB 3 Data Ready
18	PA 7
19	PA 6
20	PA 5
21	PA 4
22	PA 3
23	PA 2
24	PA 1
25	PA 0
26	VSS, System GND.

NOTES:

IRQ is controlled by interval timer (SEE: 4-4).

RESET. A low level on RESET (POWER-ON-RESET or manual RESET by CPU system) will RETURN all I/O lines of the 6530 device to the input mode and will

If a terminal with RS 232-C interface logic is used normally it requires "Ready" signals to enable receiving and transmitting data. The user has to connect these Ready lines to VCC, VDD or an external positive power supply line.

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias..... 0°C to 70°C
 Storage Temperature..... -55°C to +120°C
 Voltage on Any Pin except Pin 1 (VBB) and Pin 31 (VDD) with respect to Ground (VSS).... -0.3V to + 7V
 Voltage on Pin 1 (VBB) with respect to Ground (VSS)..... -7 V to +0.3V
 Voltage on Pin 31 (VDD) with respect to (VBB)..... -0.3V to +20V
 External Power Supply..... ±15V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the BEM-MON-1 Card. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(TA = 0°C to + 70°C | VDD = + 12V, VCC = + 5V | + 5% unless otherwise specified)
 VBB = - 5V, VSS = 0V

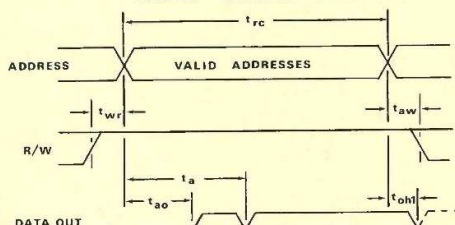
Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ. ¹	Max.		
GENERAL CARD DATA	I _{LIH} Input Load Current on any Bus Input Pin "High Level"			20 100	μ A μ A	V _{IN} = 2.7 V V _{IN} = 7 V
	I _{LIL} Input Load Current on any Bus Input Pin "Low Level"			-200	μ A	V _{IN} = 0.4 V
	I _{LD} Leakage Current Data Bus Pins "Off State"			20 -200	μ A μ A	V _{IN} = 2.7 V V _{IN} = 0.4 V
	I _{CC1} VCC Power Supply Current Standard Version with 1K byte RAM, without EPROM's		350	660	m A	V _{IN} = 2.7 V V _{IN} = 0.4 V VCC = 5.25V TA = 0°C (Data out not selected, worst case conditions)
	I _{CC2} VCC Power Supply Current With 2K byte RAM and 2 EPROM's*		460	880	m A	At TA = 0°C (worst case conditions)
	I _{DD} VDD Power Supply Current With 2 EPROM's*		100	130	m A	At TA = 0°C (worst case conditions)
	I _{BB} VBB Power Supply Current With 2 EPROM's*	- 60		- 90	m A	At TA = 0°C (worst case conditions)
	I _E External Power Supply Current		30 - 30	40 - 40	m A m A	V _{E+} = + 12V Terminal V _{E-} = - 12V Connected
	V _{IL} Input "Low" Voltage (Bus)	-0.5		0.8	V	
	V _{IH} Input "High" Voltage (Bus)	2		VCC	V	
	V _{OL} Output "Low" Voltage (Data Bus)			0.5	V	I _{OL} = 24 mA
	V _{OH} Output "High" Voltage (Data Bus)	2			V	I _{OH} = -15 mA

¹ Typical values are for TA = 25°C and nominal supply voltage.

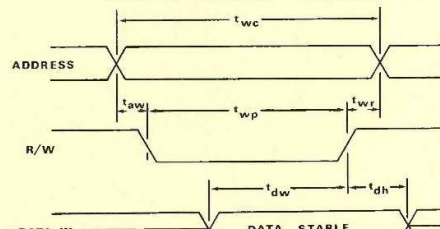
* Values are for TMS 2708 JL EPROM's Texas Instruments and INTEL 2708.

TYPICAL PIA DATA	V _{IHP} PIA Input Voltage "High Level"	2.4		VCC	V	PIA Data at TA = 25°C
	V _{ILP} PIA Input Voltage "Low" Level	-0.3		0.4	V	
	I _{IHP} PIA Input "High" Current Port A, Port B	-100	-300		μ A	V _{IN} = 2.4V
	I _{ILP} PIA Input "Low" Current Port A, Port B		-1.0	-1.6	m A	V _{IN} = 0.4V
	V _{OHP} PIA Output "High" Voltage	2.4			V	I _L = -100 μA
	V _{OLP} PIA Output "Low" Voltage			0.4	V	I _L = 1.6 mA
	I _{OHP} PIA Output "High" Current (Sourcing) Port A, Port B	-0.1 -3.0	-1.0 -5.0		m A m A	V _{OH} = 2.4V V _{OH} = 1.5V (PA0 - PB0)
	I _{OLP} PIA Output "Low" Current (Sinking) Port A, Port B	1.6			m A	V _{OL} = 0.4V

READ CYCLE TIMING



WRITE CYCLE TIMING



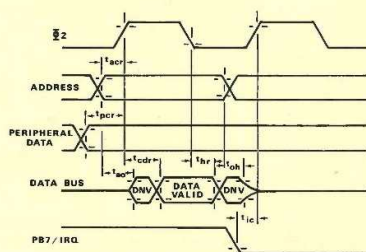
AC CHARACTERISTICS (RAM/EPROM)

AC CHARACTERISTICS (RAM/EPROM)			TMS 4045-45 (2114)			EPROM - 2708			
Symbol		Parameter	Limits			Unit	Limits		
			Min.	Typ.	Max.		Min.	Typ.	Max.
READ CYCLE	t_{rc}	Read Cycle	470			ns	470		
	t_a	Access Time			470	ns		470	
	t_{ao}	Valid Address to Output Time		90	135	ns		90	135
	t_{ohl}	Previous Read Data Valid with Respect to Address	30			ns	15		
WRITE CYCLE	t_{wc}	Write Cycle	470			ns	AC CONDITIONS OF TEST: Reference Levels: 0.8V and 2.0V. Output Load: 1 TTL Gate and $C_L=100$ pf. ($T_A=0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, $V_{DD}=+12\text{V} \pm 5\%$, $V_{CC}=+5\text{V} \pm 5\%$, $V_{BB}=-5\text{V} \pm 5\%$, $V_{SS}=0\text{V}$, unless otherwise specified.		
	t_{aw}	Address to Write Setup Time	0			ns			
	t_{wp}	Write Pulse Width	200			ns			
	t_{wr}	Write Recovery Time	20			ns			
	t_{dw}	Data Setup Time	180			ns			
	t_{dh}	Data Hold Time	20			ns			

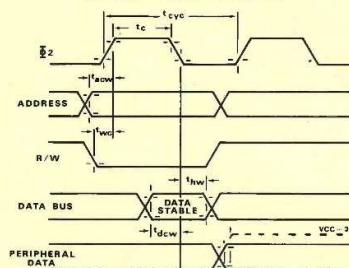
AC CHARACTERISTICS (6530)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
READ CYCLE	t_{acr} Address Valid before Positive transition of Clock	180			ns	PORT A and PORT B are loaded with 30 pf + 1 TTL Load Reference Levels in Timing Diagram are: $h = 2.0\text{ V}$ $l = 0.4\text{ V}$ Unless otherwise Specified
	t_{pcr} Peripheral Data Valid before positive transition of Clock	300			ns	
	t_{ao} Valid Address to Output Time		91	135	ns	
	t_{cdr} Data Bus Valid after Positive transition of Clock			430	ns	
	t_{hr} Data Bus Hold Time	10			ns	
	t_{oh} Data Bus Active after Address			135	ns	
	t_{ic} $\overline{\text{IRQ}}$ (Interval Timer Interrupt) Valid before Positive transition of Clock	180			ns	
WRITE CYCLE	t_{cyc} Clock Period	1		10	μs	
	t_c Clock Pulse Width	470			ns	
	t_{wc} R/W Valid before Positive transition of Clock	180			ns	
	t_{acw} Address Valid before Positive transition of Clock	180			ns	
	t_{dcw} Data Bus Valid before Negative transition of Clock	300			ns	
	t_{hw} Data Bus Hold Time	10			ns	
	t_{cpw} Peripheral Data Valid after Negative transition of Clock			1	μs	
	t_{cmos} Peripheral Data Valid after Negative transition of Clock driving CMOS (Level = $V_{CC} - 30\%$)			2	μs	

READ CYCLE TIMING



WRITE CYCLE TIMING





IMPORTANT MONITOR LOCATIONS AND MONITOR COMMAND SUMMARY

(See TIM manual for detailed description)

PROMPTING CHARACTER IS A PERIOD (.)

DISPLAY COMMANDS

.R Display Registers (PC,F,A,X,Y,SP)
.M ADDR Display Memory (8 bytes beginning at ADDR)

ALTER COMMAND (:)

.: DATA Alters Previously Displayed Item or Next Item

PAPER TAPE I/O COMMANDS

.LH Load HEX Tape
.WB ADDR1 ADDR2 Write BPNF Tape (From Low ADDR1 to High ADDR2)
.WH ADDR1 ADDR2 Write HEX Tape (From Low ADDR1 to High ADDR2)

CONTROL COMMANDS

.G Go, Continue Execution from current PC Address
.H Toggles High-Speed-Reader Option (If its On, Turns it Off; If Off, Turns it On)

BRK AND NMI ENTRY POINTS TO TIM

TIM is normally entered when a 'BRK' instruction is encountered during program execution. At that time CPU registers are output: * PC F A X Y SP and control is given to the Keyboard.

User may enter TIM by programmed BRK or induced NMI. NMI entries cause a '#' to precede the '*' in the CPU register printout format.

NON-BRK IRQ (EXTERNAL DEVICE) INTERRUPT HANDLING

A NON-BRK IRQ interrupt causes an indirect jump to the address located at 'UINT' (\$FFFF). This location can be SET using the ALTER CMD, or loaded automatically in Paper Tape Form with the LH CMD if the user assigns his IRQ interrupt vector to \$FFFF in the source assembly program.

If not RESET by the user, UINT is SET to cause external device interrupts to enter TIM as NMIs. I.e., if a NMI occurs without an induced NMI signal, it is an external device interrupt.

SETTING AND RESETTING PROGRAM BREAKPOINTS

Breakpoints are SET and RESET using the Memory Display and ALTER COMMANDS. BRK has a '00' operation code. To SET a breakpoint simply Display the Memory location (First instruction byte) at which the breakpoint is to be placed then alter the location to '00'. There is no limit to the number of breakpoints that can be active at one time.

To RESET a breakpoint, restore the altered Memory location to its original value.

When and if a breakpoint is encountered during execution, the breakpoint data preceded by an '*' is displayed. The program counter value displayed is the BRK instruction + 1.

MONITOR ROUTINES

JSR WRT Type a character, Source=Accumulator.
\$72C6 A, X cleared; Y preserved.
JSR RDT Read a character, Value in Accumulator.
\$72E9 X cleared; Y not preserved.
JSR CRLF Type CR - LF with delay.
\$728A A, X cleared; Y preserved.
JSR SPACE Type a Space character.
\$7377 A, X, Y preserved.
JSR WROA Type two bytes (address) in HEX.
\$729A (AH = \$00EE, AL = \$00ED).
X cleared; Y preserved.
JSR WROB Type a byte in HEX., Source=Accumulator. A, X cleared; Y preserved.
\$72B1
JSR RDHSR Read a character from parallel input port (high speed paper tape reader). Character is stored into X register. Accumulator contains character trimmed to 7 bits, Y preserved.
\$733D
JMP START Return to Monitor from user program
\$7086 and print prompting character.

SPECIAL LOCATIONS

START ADDRESS SET with HEX. tape on load
AH = \$00F7
AL = \$00F6
CR - LF DELAY SET on load or with user program
\$00E3 (in bit times, minimum of 1. Zero means 256 bits time delay).
UINT VECTOR User IRQ vector
\$FFFF
NMI VECTOR Hardware NMI vector
\$FFFA
RESET VECTOR Hardware RESET vector
\$FFFC
IRQ VECTOR Hardware IRQ vector
\$FFFE

TAPE FORMAT

TIM will generate and load paper tape in assembler output format. The format is as follows:
Zero or more leading characters except ";"
(usually blank leader). Any number of records of the form: ;ccaaaadddd...ddssss, where:
cc is the number of bytes in the record in HEX.
aaaa is the HEX. address to store the first byte of data, dddd...dd is the data (two HEX. digits per byte), ssss is the check-sum, which is the arithmetic sum, to 16 bits, of all count, address and data bytes represented by the record
A terminating record of zero length, either: ;00 or ; CR (Carriage-return).

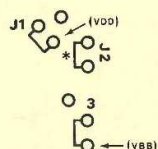
JUMPERS:

The power supply jumpers for the interface section are located just below the I/O HEADER near the 75188 interface IC. Drawings are for component side of print.

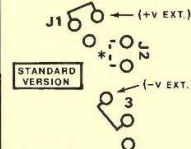
Jumper J4 is located near the bus connector somewhat right from the middle. The strap interconnecting PB7 to the IRQ pin is located just below the BUS

INTERFACE SECTION

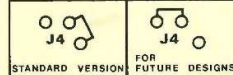
INT. POWER SUPPLY



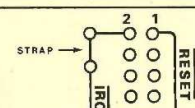
EXT. POWER SUPPLY



CARD SELECT (J4)

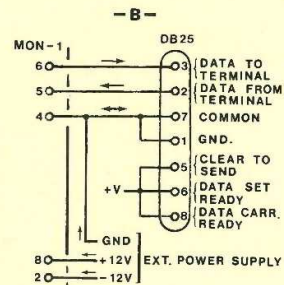
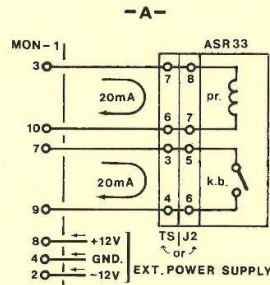


STRAP OPTION PB7/IRQ



TERMINAL CONNECTIONS

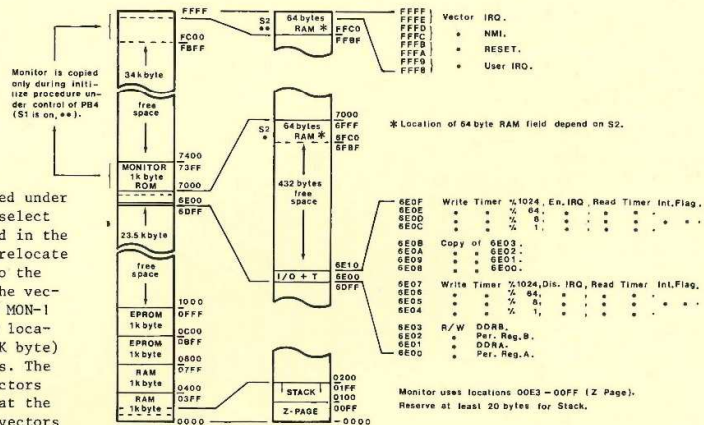
To connect a terminal properly two examples are represented to the right. In example "A" a Teletype of the ASR-33 type is connected (20 mA Current Loop). Example "B" represents the general connection to a terminal with RS 232-C interface (25-pin "D" connector). In our case the pins 5, 6 and 8 have to be connected to a positive level. External power supply connections are discussed before (SEE: page 3 section 5-2 and jumper section on page 7).



MEMORY MAP OF B.E.M-MON-1 MONITOR COMBI CARD

NOTES:

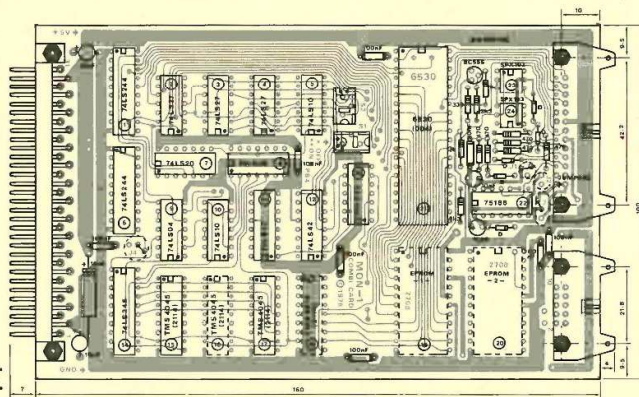
If the system is initialized under user program control the PB4 select switch (S1) has to be switched in the "Off" position (*). The RAM relocate switch (S2) can be switched to the "Low" position (*) because the vectors are not fetched from the MON-1 Card. In this case all memory locations from \$7400 - \$FFFF (35 K byte) are free for user applications. The user has to supply its own vectors at least reading some memory at the top of the map. For instance vectors can be burned into PROM device on BEM-CPU-1 Processor Card.



MECHANICAL SPECIFICATIONS

- 1) PRINTED CIRCUIT: 1.6 mm. epoxy glass fiber reinforced in EURO CARD format (100 X 160 mm.) Double sided metallized with plated through holes finally covered with an epoxy mask on both sides.
- 2) BUS-CONNECTOR: 31-pin (gold plated) indirect connector (DIN 41617)
- 3) HEADERS: 1 x 26-pin + 1 x 10-pin Flat Cable Headers accepting standard female socket connectors designed for Flat Cable with 0.050" (1.27 mm.) conductor spacing
- 4) STANDARD version with IC sockets
- 5) MAXIMUM THICKNESS all versions: 12.5 mm.
Solder side :- 2.0 mm.
Component side :- 8.8 mm.

MECHANICAL LAY-OUT (dimensions in mm.)



representatives:

BRUTECH ELECTRONICS
P.O.Box 58, Vinkeveen
Telex: 18576 BEMIN
The Netherlands

