



**BRUTECH
ELECTRONICS**

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B.E.M - CPU-1

LOW COST CENTRAL PROCESSOR CARD
(based on 6502 microprocessor)

GENERAL DESCRIPTION

The BEM-CPU-1 CENTRAL PROCESSOR CARD is a general purpose processor card based on the 6502 microprocessor. In standard version the BEM-CPU-1 will be delivered with a 1 MHz crystal based clock. A 2 MHz version supplied with the 6502A is optionally available.

The address bus, data bus and control lines R/W and $\Phi 2$ are fully buffered with 3-state buffers controlled either by the DMA control circuit available on the card, or by an external signal (TSC) depending on the position of the BUS CONTROL switch. Another switch ($\Phi 2$ MODE SELECT) enables the user to select the $\Phi 2$ output line to be either continuous active or under DMA control (TSC).

Except for a small PROM (32 X 8 bit) decoded on location \$FFE0 - \$FFF, (normally used for the user specific vectors) the BEM-CPU-1 is not supplied with memory or other addressable devices. Even the PROM can be switched off. (PROM SELECT switch) enabling the user to have full access to any memory location in the system under DMA control.

The lack of essential memory and I/O implies the CPU-1 has to be used always in combination with other cards to create a working system. At least some RAM will be necessary on page 0 and page 1 (stack). For detailed description of 6502 system implications the hardware and application manuals of MOS Technology, Rockwell or Synertek are recommended.

The CPU-1 is provided with three manually controlled switches located at the top left side of the card. From left to the right the functions are respectively:

1) RUN/HALT

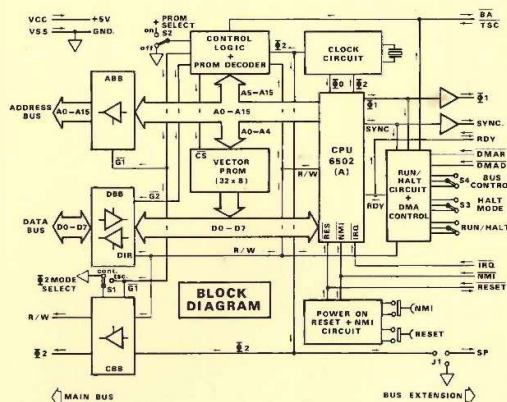
In the RUN position the CPU-1 works normal. However, if the switch is turned in the HALT position the processor will stop.

"Continued on page 2."

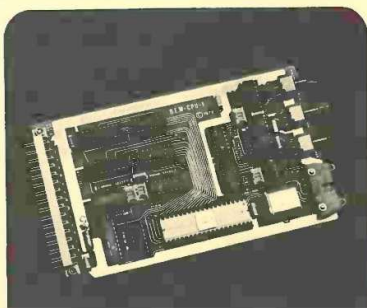
FOR MICROPROCESSOR APPLICATIONS

FEATURES

- * LOW COST 6502 BASED CPU CARD
- * 1 MHz CRISTAL BASED CLOCK STANDARD (2 MHz OPTIONAL)
- * SINGLE (+ 5V) POWER SUPPLY REQUIRED
- * FULLY BUFFERED BUS STRUCTURE (3-STATE BUFFERS)
- * DMA CONTROL CIRCUIT ON CARD
- * POWER-ON-RESET CIRCUIT ON CARD
- * VECTOR PROM (32 X 8) ON CARD (SELECTABLE)
- * SELECTABLE HALT MODE ($\Phi 1$ / SYNC.)
- * SELECTABLE $\Phi 2$ OUTPUT MODE (CONT. / 3-STATE)
- * SELECTABLE BUS CONTROL (INT. / EXT.)
- * CONTROL SWITCHES FOR: RUN/HAULT, RESET AND NMI
- * 31-PIN INDIRECT BUS CONNECTOR (DIN 41617)
- * 10-PIN FLAT CABLE HEADER (BUS EXTENSION)
- * ALL IC's (LOW POWER SCHOTTKY) MOUNTED IN SOCKETS
- * GENEROUS OEM DISCOUNTS AVAILABLE



BEM - BUS - COMPATIBLE



(MAIN) BUS CONNECTIONS

Pin	Function	Pin	Function	Pin	Function
1	N.C.	11	N.C.	21	A 8
2	VSS GND	12	R/W	22	A 7
3	D 7	13	$\Phi 2$	23	A 6
4	D 6	14	A 15	24	A 5
5	D 5	15	A 14	25	A 4
6	D 4	16	A 13	26	A 3
7	D 3	17	A 12	27	A 2
8	D 2	18	A 11	28	A 1
9	D 1	19	A 10	29	A 0
10	D 0	20	A 9	30	VCC + 5V

GENERAL DESCRIPTION (continued)

A small sliding switch (HALT MODE SELECT) on the card will enable the user to select one or two HALT modes.

- A) $\Phi 1$, the processor will stop at the first $\Phi 1$ clock pulse of a non-write cycle after the RUN/HALT switch has been switched to the HALT position.
- B) SYNC., the processor will stop at the first $\Phi 1$ clock pulse of a SYNC. cycle after switching to the HALT position.

In combination with the BUS CONTROL switch the user can select the bus to be active or in 3-state after the processor has entered the HALT mode. In DMA applications the bus must be in 3-state. An active bus (in the HALT mode) will be very useful in hardware debugging and analyzing applications. Simple external logic will enable the user to create "single cycle" and "single instruction" operation as well as "hardware breaks".

- 2) NMI The function of the NON MASKABLE INTERRUPT push button switch is to create a manual controlled NMI signal, normally used to interrupt a running program. The NMI switch is connected to a timing circuit to create a pulse without bounce. The output of this circuit is directly connected to the NMI input of the processor and the NMI line of the BUS EXTENSION header. This input can be used in

wire-or configuration. (The output circuit of the timer is of the open collector type provided with pull-up resistor).

- 3) RESET The function of the RESET push button is to create a manual controlled RESET signal. The RESET switch is connected to the POWER-ON-RESET circuit. This circuit will generate a RESET pulse after a return from a POWER-DOWN situation or each time the RESET switch is activated. The P.O.R. circuit in combination with the PROM (provided with the user specific system vectors) will enable the user to create its own TURN KEY SYSTEM. The output of the P.O.R. circuit (open collector type too.) is directly connected to the RESET input of the processor and the RESET input (output) line of the BUS EXTENSION header.

The BUS EXTENSION flat cable header is located at the top right side of the card. All other system cards using one or more BUS EXTENSION LINES are provided with a corresponding header at the same location. So they can be interconnected in a very simple way. The functions of the BUS EXTENSION LINES are described in detail below. The lines 1 to 3 are normalized throughout the BEM-BUS system. The other lines are dedicated to the processor card used in the system (BEM-CPU-1). Other CPU cards to be released in the near future may have other defined functions, but will never become in conflict with standard system cards.

BUS EXTENSION FLAT CABLE HEADER CONNECTIONS

Pin	Function	Pin	Function
1	RESET	6	RDY
2	IRQ	7	BA / TSC
3	NMI	8	DMAR
4	$\Phi 1$	9	DMAD
5	SYNC	10	SP

- 1) RESET A low level on the system RESET line will initialize the reset procedure. As discussed before the RESET line is connected to the P.O.R. circuit. After a return from a POWER-DOWN condition or a release of the RESET switch this line will be low active for at least 50 msec. System cards provided with individual P.O.R. circuitry (e.g. BEM-PIA-1A) interconnected to this RESET line will generally cause no problems (open collector output).

- 2) IRQ A low level on the IRQ line will initialize the Interrupt Request procedure only if the Interrupt Mask Flag in the processor status register has been enabled (bit 2, 0 = enabled, 1 = disabled). The IRQ line is connected to the IRQ input of the processor. A pull-up resistor of 3k3 is provided on the card.

- 3) NMI A high to low transition on the NMI line will initialize the NON MASKABLE INTERRUPT procedure. As described before the NMI line is connected to the NMI input of the processor and to the output of the NMI debounce circuit (NMI manual controlled switch). This output is of the open collector type provided with a 3k3 pull-up resistor.

- 4) $\Phi 1$ The phase 1 output of the processor

- 5) SYNC The SYNC. output of the processor is connected to this line via two cascaded inverters of the 74LS04 type too.

- 6) RDY This line is connected to the RDY input of the processor. The output of the DMA control circuit is connected to the RDY input too (open collector type with a pull-up resistor of 3k3). Using the RDY input together with some simple external logic the user can generate "single cycle" and "single instruction" modes as well as hardware breaks.

- 7) BA/TSC This line behaves like an open collector output circuit provided with a pull-up resistor of 2k2 and can be used either as an input or an output. Defined as an output (BA) this line will be used to acknowledge the Bus is available (BA, low = Bus Available) for DMA applications. Defined as an input (TSC) this line can be used to force the Bus in 3-state mode, e.g. to be used in high speed DMA during the $\Phi 1$ clock cycle.

- 8) DMAR A low level applied to this DMAR (DMA REQUEST) input line will stop the processor in a corresponding way as described under RUN/HALT control. The RUN/HALT control switch has to be considered as the manual control of the DMA mode.

- 9) DMAD A low level applied to this DMAD (DMA DISABLE) input line will be used to allow a DMA REQUEST on the DMAR input line to be ignored. The RUN/HALT switch will be inoperative too in that case. A low level applied to the DMAD line during a DMA operation (or HALT mode) will interrupt this mode and return the CPU-1 to the RUN mode. The DMA control circuit will take care the timing is correct.

- 10) SP In principle this spare line is free to be used for special purposes. However, on the CPU-1 the SP line can be inter-

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias..... 0°C to 70°C
Storage Temperature..... -55°C to +120°C
Voltage on Any Pin with respect
to Ground..... -0.3V to +7V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the BEM-CPU-1 card. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(TA= 0°C to + 70°C, VCC=+5V + 5% unless otherwise specified)

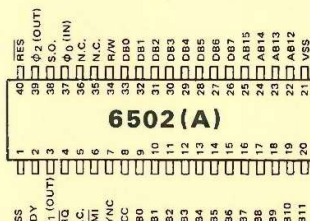
Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.*	Max.		
MAIN BUS	V _{OL} Output "Low" Voltage on any Bus Pin			0.5	V	Address } I _{OL} = 24 mA Data } I _{OL} = 8 mA R/W, Φ 2
	V _{OH} Output "High" Voltage on any Bus Pin	2			V	Address } I _{OH} = -3 mA R/W, Φ 2 } I _{OH} = -15 mA Data } I _{OH} = -15 mA
	I _L Leakage Current on any Bus Pin in "Off State"			20 -20 -200	μ A μ A μ A	All Pins V _{IN} = 2.7 V R/W, Φ 2 } V _{IN} = 0.4 V Data }
	V _{ILD} Input "Low" Voltage Data Bus	-0.5		0.8	V	
	V _{IHD} Input "High" Voltage Data Bus	2		VCC	V	
	I _{CC} VCC Power Supply Current (without PROM)		210	410	mA	Run Mode
	with PROM 74S288**		290	520	mA	Bus Loaded with 1 TTL Load

BUS EXTENSION	V _{IHT} Input High Threshold Voltage RESET, NMI, IRQ, RDY	2			V	RESET, NMI, IRQ and RDY lines are provided with pull-up resistors of 3k3 on card
	V _{ILT} Input Low Threshold Voltage RESET, NMI, IRQ, RDY			0.8	V	
	V _{OL1} Output Low Voltage RESET NMI, RDY, BA			0.5	V	I _{OL1} = 8 mA
	V _{OL2} Output Low Voltage Φ 1, SYNC			0.4	V	I _{OL2} = 4 mA
	V _{OH2} Output High Voltage Φ 1, SYNC	2.4			V	I _{OH2} = -0.4 mA
	V _{IL1} Input Low Voltage, DMAR, DMAD, TSC	-0.5		0.8	V	DMAR, DMAD and TSC inputs are provided with pull-up resistors on card (DMAR + DMAD with 3k3, TSC with 2k2)
	V _{IH1} Input High Voltage, DMAR DMAD, TSC	2		VCC	V	

* Typical values are for TA = 25°C.

** This is an example only, other suitable PROM's are: HA 7603, IM 5610, 6331-1 and 82S123.

CPU PIN CONFIGURATION



WARNING !

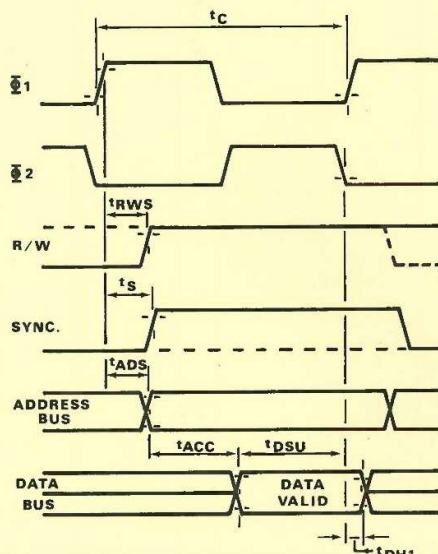
Bus lines may not be short circuited for extended periods. According to Bus Buffer specifications only one output per device may be shorted at a time for continuous periods lasting no longer than one second.

AC CHARACTERISTICS (READ/WRITE CYCLE TIMING)

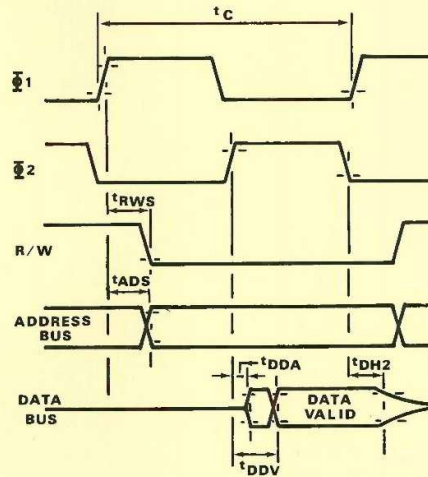
Symbol	Parameter	Limits (1 MHz)			Limits (2 MHz)			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t_C	Cycle Time	1000			500			ns
t_{RWS}	READ WRITE Set up Time		90	290		90	140	ns
t_{ADS}	Address Set up Time		90	290		90	140	ns
t_S	Sync. Set up Time			350			175	ns
t_{ACC}	Memory Read Access Time			535			260	ns
t_{DSU}	Data Stability Time Period	150			100			ns
t_{DH1}	Data Hold Time (Read Mode)	0			0			ns
t_{DH2}	Data Hold Time (Write Mode)		30	60		30	60	ns
t_{DDA}	Delay Time $\Phi 2$ High to Data Bus Active		25	35		25	35	ns
t_{DDV}	Delay Time $\Phi 2$ High to Data Out Valid		130	180		55	80	ns

Note: Timing figures and diagrams are for bus signals only.

READ CYCLE TIMING



WRITE CYCLE TIMING



Reference levels are:
high = 2.0 V

DMA CONTROL NOTES

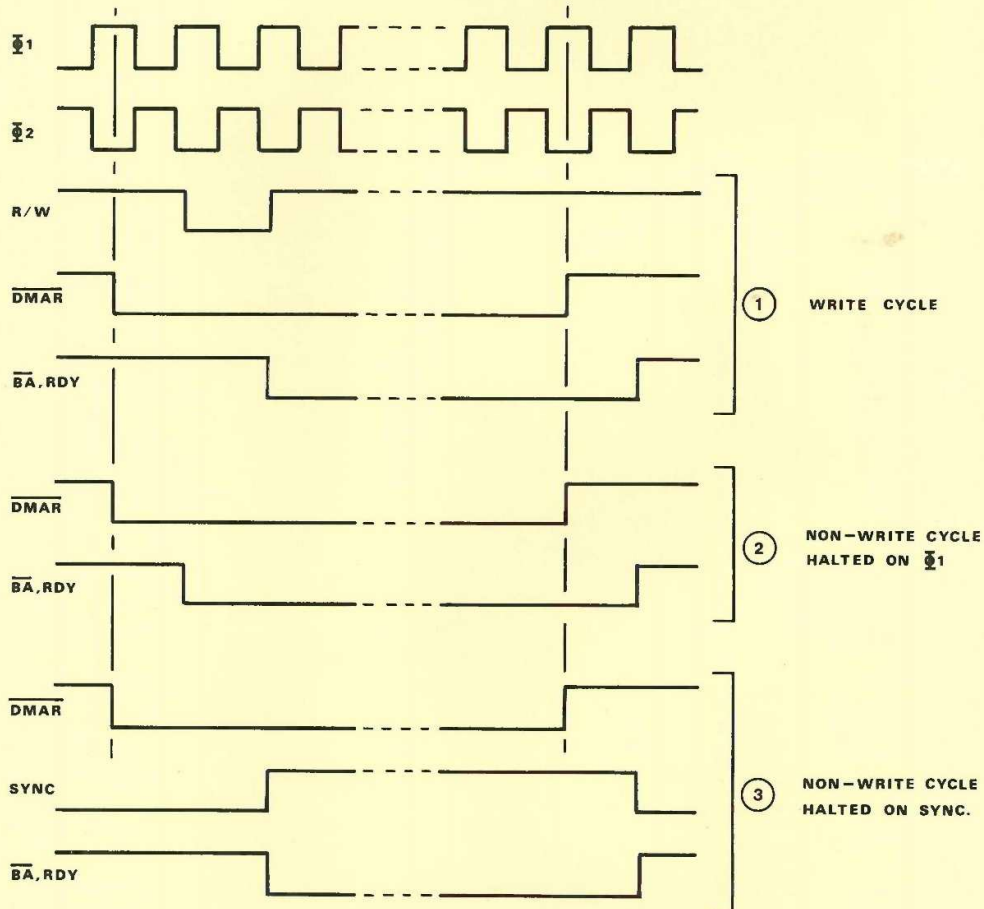
In the timing diagrams below some examples are shown representing the relation between DMA Request and Bus Available signals. The BA output will be active only if the BUS CONTROL switch is positioned in the internal mode. In case this switch is in the external mode position, for instance used in Bus Analyzing Applications, the user can profit the RDY line as a DMA Request Acknowledge output. (Note: in this particular case the DMAR input is used only to halt the processor. DMA is not possible because the address bus will be active in the HALT mode). In general the processor will stop at the next $\Phi 1$ clock cycle after the DMAR input goes low. However, there are some exceptions represented by the examples 1 and 3.

EXAMPLE 1: If the DMA Request occurs during or just before a WRITE operation, the WRITE operation will be finished first. BA will be active low at the first $\Phi 1$ clock cycle of the next READ operation.

EXAMPLE 2: This is the normal mode if the HALT MODE SELECT switch is switched to the $\Phi 1$ position.

EXAMPLE 3: In this example the HALT MODE SELECT switch is switched to the SYNC. position. The processor will stop now at the first $\Phi 1$ clock cycle of a SYNC. cycle (Op Code Fetch Instruction) after the DMAR input goes low.

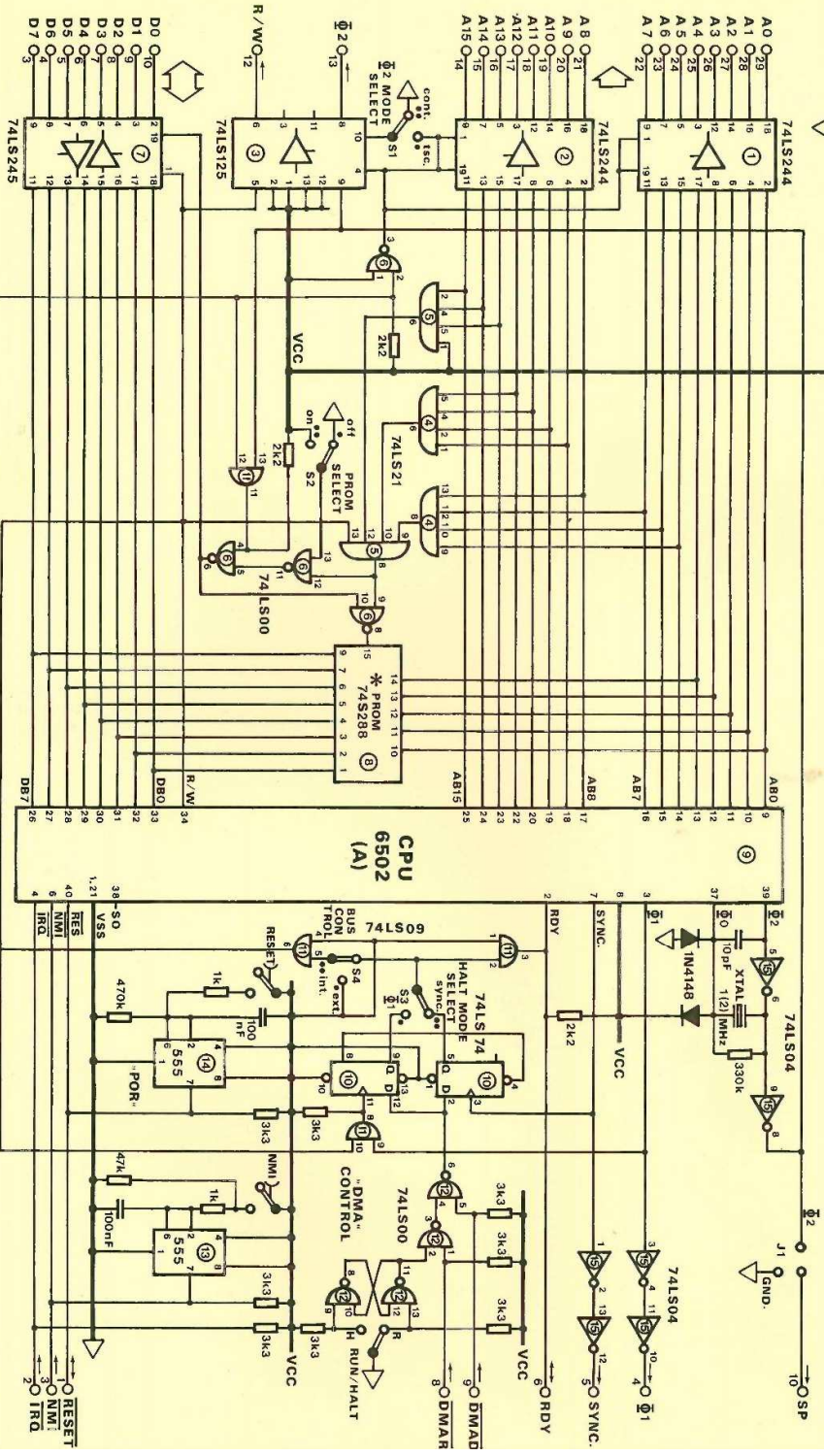
DMA TIMING



VCC 0V
10 100nF
VSS 2
+5V

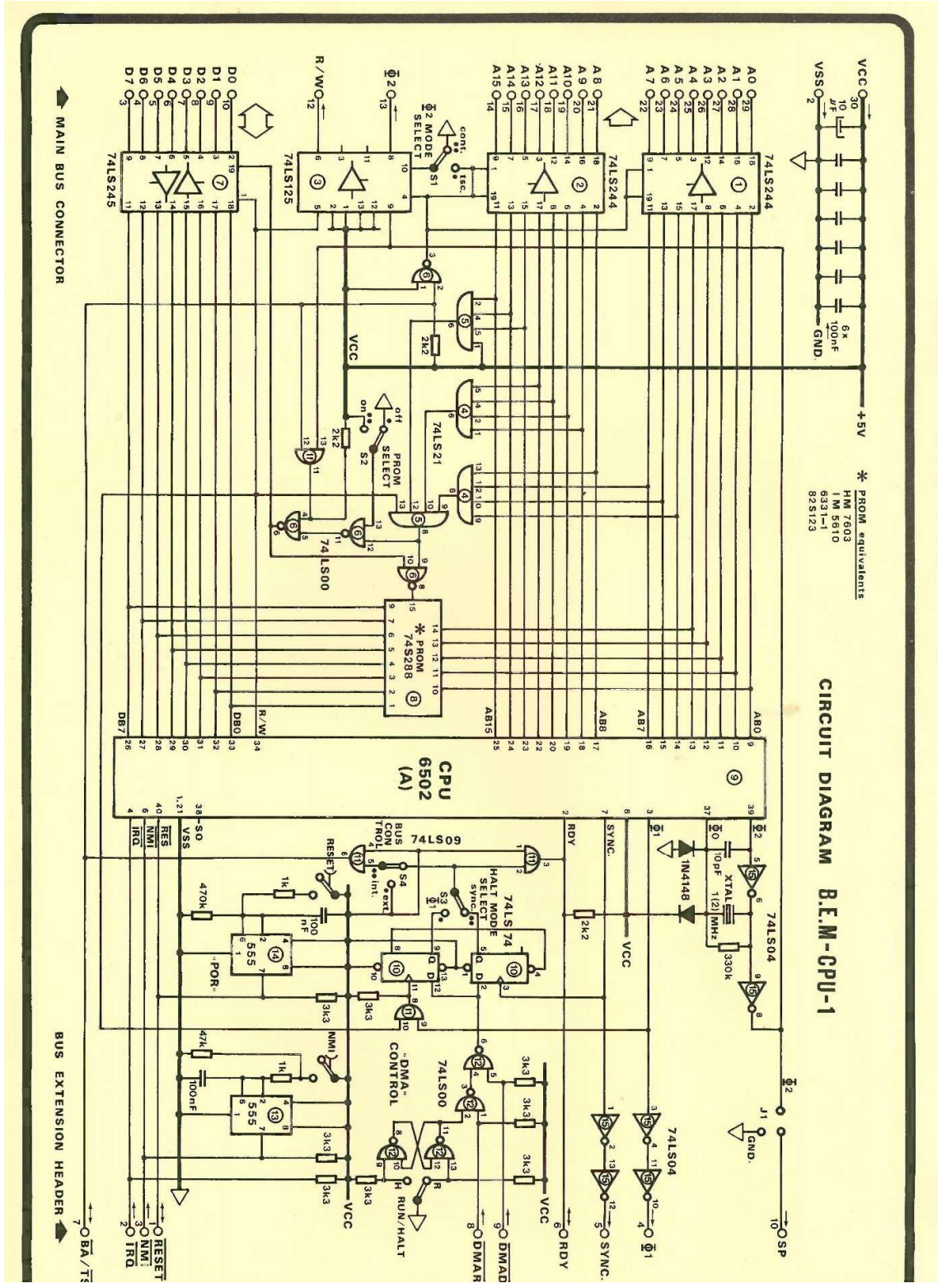
* PROM equivalents
HM 7603
1 M 5610
6331-1
825123

CIRCUIT DIAGRAM B.E.M-CPU-1



MAIN BUS CONNECTOR

BUS EXTENSION HEADER



SUMMARY OF 6502 ADDRESSING MODES AND INSTRUCTION SET

ACCUMULATOR ADDRESSING — This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

IMMEDIATE ADDRESSING — In immediate addressing, the operand is contained in the second byte of the instruction, with no further memory addressing required.

ABSOLUTE ADDRESSING — In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Thus, the absolute addressing mode allows access to the entire 65K bytes of addressable memory.

ZERO PAGE ADDRESSING — The zero page instructions allow for shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code efficiency.

INDEXED ZERO PAGE ADDRESSING — (X, Y indexing) — This form of addressing is used in conjunction with the index register and is referred to as "Zero Page, X" or "Zero Page, Y". The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally due to the "Zero Page" addressing nature of this mode, no carry is added to the high order 8 bits of memory and crossing of page boundaries does not occur.

INDEXED ABSOLUTE ADDRESSING — (X, Y indexing) — This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X", and "Absolute, Y". The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.

IMPLIED ADDRESSING — In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

RELATIVE ADDRESSING — Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is -128 to +127 bytes from the next instruction.

INDEXED INDIRECT ADDRESSING — In indexed indirect addressing (referred to as (Indirect, X)), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents is the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

INDIRECT INDEXED ADDRESSING — In indirect indexed addressing (referred to as (Indirect, Y)), the second byte of the instruction points to a memory location in page zero. The contents of this memory location is added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

ABSOLUTE INDIRECT — The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location is contained in the third byte of the instruction. The contents of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter.

INSTRUCTION SET in ALPHABETIC SEQUENCE

ADC Add Memory to Accumulator with Carry
AND "AND" Memory with Accumulator
ASL Shift Left One Bit (Memory or Accumulator)

BCC Branch on Carry Clear
BCS Branch on Carry Set
BEQ Branch on Result Zero
BIT Test Bits in Memory with Accumulator
BMI Branch on Result Minus
BNE Branch on Result not Zero
BPL Branch on Result Plus
BRK Force Break
BVC Branch on Overflow Clear
BVS Branch on Overflow Set

CLC Clear Carry Flag
CLD Clear Decimal Mode
CLI Clear Interrupt Disable Bit
CLV Clear Overflow Flag
CMP Compare Memory and Accumulator
CPX Compare Memory and Index X
CPY Compare Memory and Index Y

DEC Decrement Memory by One
DEX Decrement Index X by One
DEY Decrement Index Y by One

EOR "Exclusive-or" Memory with Accumulator

INC Increment Memory by One

JMP Jump to New Location
JSR Jump to New Location Saving Return Address

LDA Load Accumulator with Memory
LDX Load Index X with Memory
LDY Load Index Y with Memory
LSR Shift One Bit Right (Memory or Accumulator)
NOP No Operation

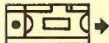
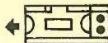
ORA "OR" Memory with Accumulator
PHA Push Accumulator on Stack
PHP Push Processor Status on Stack
PLA Pull Accumulator from Stack
PLP Pull Processor Status from Stack

ROL Rotate One Bit Left (Memory or Accumulator)
ROR Rotate One Bit Right (Memory or Accumulator)
RTI Return from Interrupt
RTS Return from Subroutine

SBC Subtract Memory from Accumulator with Borrow
SEC Set Carry Flag
SED Set Decimal Mode
SEI Set Interrupt Disable Status
STA Store Accumulator in Memory
STX Store Index X in Memory
STY Store Index Y in Memory

TAX Transfer Accumulator to Index X
TAY Transfer Accumulator to Index Y
TSX Transfer Stack Pointer to Index X
TXA Transfer Index X to Accumulator

TABLE OF CONTROL SWITCH FUNCTIONS

Control Switch	Name		
S1	Φ2 MODE SELECT	Φ2 Output under 3-state control together with other Bus lines	Φ2 Output is continuous available independent of 3-state mode of other Bus lines
S2	PROM SELECT	PROM not selected. Vectors have to be fetched externally	PROM selected*. The PROM field (\$FFE0 - \$FFFF) will be fetched from CPU-1
S3	HALT MODE SELECT	The processor stops on Φ1 clock pulse of any NON-WRITE cycle after a DMA Request or switching to the HALT MODE (RUN/HALT switch)	The processor stops on Φ1 clock pulse of SYNC. cycle after a DMA Request or switching to the HALT MODE (RUN/HALT switch)
S4	BUS CONTROL	3-state control of Bus lines is under control of TSC input only. (Low = 3-state)	3-state control of Bus lines can be under control of TSC input as well as under control of DMA control circuit or RUN/HALT switch

*If PROM is selected an external field at the same location will be selected too but does not come in conflict with system activity; because the Data Bus buffers on the CPU-1 will be in the 3-state mode.

PROM OPTION

As mentioned before the CPU-1 is provided with a selectable (On/Off) PROM field located from \$FFE0 - \$FFFF. Normally the CPU-1 will be delivered with a standard PROM of which the top 6 locations are preprogrammed. These preprogrammed Vectors are respectively:

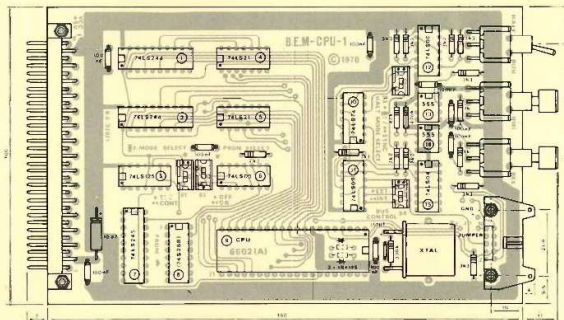
IRQ = \$0806 (\$FFFF = \$08, \$FFFE = \$06)
 RES = \$0803 (\$FFFD = \$08, \$FFFC = \$03)
 NMI = \$0800 (\$FFFB = \$08, \$FFFA = \$00)

These Vectors are pointing to a 9 byte field at the beginning of page 8 (3th K byte field) enabling the user to insert Jump Instructions on those locations (3 byte instruction) On request the CPU-1 can be delivered with PROM programmed to custom specifications at additional cost. Please contact factory or nearest representative for more details.

MECHANICAL SPECIFICATIONS

- 1) PRINTED CIRCUIT: 1.6 mm. epoxy glass fiber reinforced in EURO CARD format (100 X 160 mm.) Double sided metallized with plated through holes finally covered with an epoxy mask on both sides.
- 2) BUS-CONNECTOR: 31-pin (gold plated) indirect connector (DIN 41617)
- 3) HEADER: 10-pin Flat Cable Header accepting standard Female Socket connector designed for Flat Cable with 0.050" (1.27 mm.) conductor spacing.
- 4) STANDARD version with IC sockets
- 5) MAXIMUM THICKNESS all versions: 12.5 mm.
 Solder side :- 2.0 mm.
 Component side :- 8.8 mm.

MECHANICAL LAY-OUT (dimensions in mm.)



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