

M764

I/O-Karte 6522

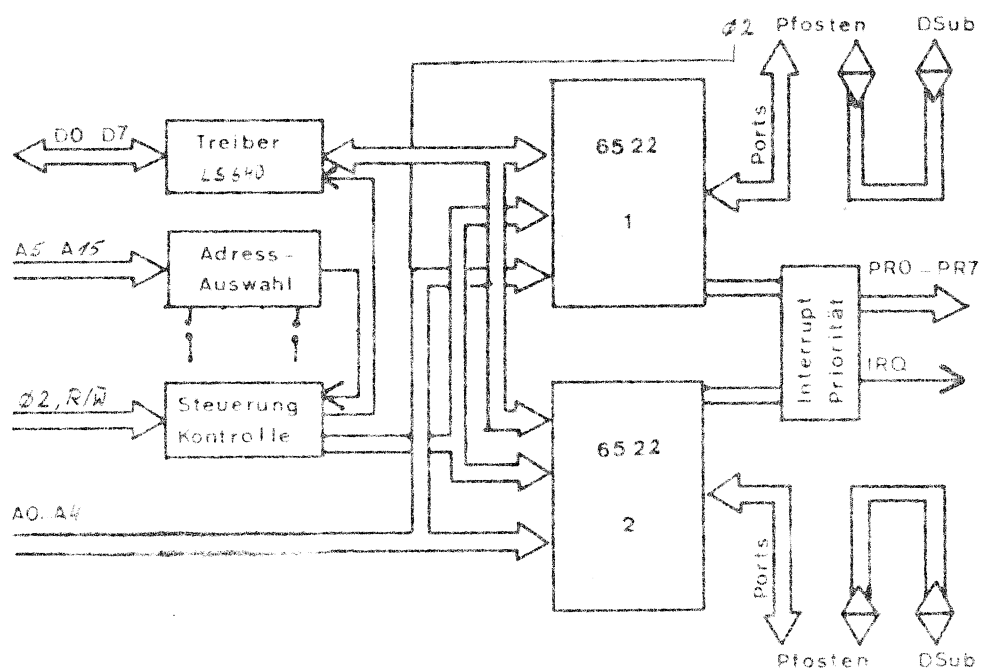
*Ausgabe
Jan. 81*

M 764

1. Allgemeines

Die Karte M764 arbeitet mit zwei universellen Interfacebausteinen vom Typ VIA 6522.

Im folgenden werden die Merkmale eines VIA Bausteins beschrieben. Bitte beachten Sie, daß Ihnen zwei Bausteine auf der Karte zur Verfügung stehen.



Die 16 Peripherieanschlüsse können völlig unabhängig voneinander durch Software als Ein- oder Ausgang programmiert werden (siehe Register 2 und 3).

Als Ausgang geschaltet können alle Ports eine TTL Last treiben. Die B-Seite kann im High-Zustand zusätzlich 1mA bei 1,5V liefern und so z.B. Darlington-Transistoren direkt treiben.

Bitte beachten Sie, daß beim Lesen der Ausgangsregister (Register 0 und 1) auf der B-Seite immer nur der vorher eingeschriebene Wert zurückgelesen wird, während bei der A-Seite der aktuelle an den Ausgangsports anliegende Wert gelesen wird. Das bedeutet, daß ein nach "High" programmierter Ausgang der extern nach "Low" gehalten wird, beim Lesen des Ausgangsregisters an dem entsprechenden Bit auch ein "Low" liefert.

Es besteht die Möglichkeit, beim Einschreiben in die A- oder B-Register über CA2 bzw. CB2 automatisch einen Quittungsimpuls zu erzeugen (siehe Register 12).

Als Eingang geschaltet stellen die Leitungen eine TTL-Last dar. Bitte beachten Sie, daß der Eingangspegel bei "Low" maximal 0,4V betragen darf.

Die Eingangszustände können über die CA1 bzw. CB1-Eingänge (siehe Register 11) abgespeichert werden. Nur die A-Seite bietet die Möglichkeit auch beim Lesen des Registers 1 automatisch einen Quittungsimpuls an CA2 zu erzeugen (Register 12).

In jeder VIA sind zwei sehr universell verwendbare 16 Bit-Timer untergebracht.

Timer 1 (Register 4,5,6 und 7) kann in vier verschiedenen Betriebsarten benutzt werden (Register 11) und zwar intern zum Erzeugen eines Interrupts nach Ablauf des geladenen Zählerwertes einmalig bzw. kontinuierlich. Weiterhin kann das Port PB7 als Ausgang dienen und der Timer erzeugt einen Puls (mono) bzw. einen kontinuierlichen Takt an diesem Ausgang.

Timer 2 (Register 8 und 9) ist ein Intervall-Zähler, der nicht kontinuierlich arbeiten kann. Er dient zum Betrieb des Schieberegisters, als Interrupt-Timer oder als Zähler von Impulsen, die über PB6 eingegeben werden.

Ein bidirektionales Schieberegister (Register 10) mit 7 verschiedenen Betriebsarten (Register 11) vervollständigt den Leistungsumfang der VIA.

Über CB2 kann der Inhalt des Registers 10 seriell ausgegeben werden und zwar unter Kontrolle von $\phi 2$, Timer 2 (hierbei wird an CB1 der Synchrontakt ausgegeben) oder durch einen externen Takt über CB1 als Eingang.

Einlaufende serielle Daten können an CB2 in das Register 10 eingetaktet werden. Drei Betriebsarten sind möglich: Timer 2 oder $\phi 2$ geben die Taktfrequenz an CB1 aus bzw. an CB1 liegt eine externe Taktfrequenz an. Hierbei unbedingt die Hinweise Kap. 3 beachten!

Die Interruptfreigabe von den Timern, den Cx-Eingängen und dem Schieberegister erfolgt in Register 14. Im Register 13 können die entsprechenden Statusbits ausgelesen werden.

2. Adreßdekodierung

Die I/O-Karte M764 benötigt 32 Byte des Prozessoradreibraums (16 Byte für jede VIA). Die Basisadresse wird durch 11 Dual-In-Line-Schalter (A5...A15) eingestellt. Die Registeradressen ergeben sich aus der Addition der Basisadresse und der Registeradressen. A0 bis A4 wählen die Register und Adreßbit 5 wählt VIA1 oder VIA2 aus.

In der Abbildung ist ein Beispiel zur Ermittlung der richtigen Schalterstellung für die Adresse \$0400 gezeigt. Dabei sind die letzten 5 Bits der Adresse nicht festlegbar, da diese - wie bereits beschrieben - zur internen Adressierung der Bausteine dienen.

1.
Schreiben Sie die gewünschte Adresse hexadezimal auf, z. B. \$0400.

0

4

0

2.
Schreiben Sie darunter das äquivalente Bitmuster.

0 0 0 0 0 1 0 0 0 0 0

3.
Schreiben Sie darunter wie folgt die Bezeichnung der 11 Dual-In-Line-Schalter

15	14	13	12	11	10	9	8	7	6	5	ADREßBIT
X	X	X	X	X	X	X	X	X	X	X	ON
					X						OFF
1	2	3	4	5	6	7	8	1	2	3	

Damit haben Sie elf Schalterstellungen ermittelt. Ist das zugehörige Adreßbit "1", schalten Sie auf "OFF"; wenn das zugehörige Adreßbit "0" ist, schalten Sie auf "ON".

Damit ergeben sich folgende Registeradressen:

Relative Adresse	Bezeichnung	Beschreibung	
		Schreiben	Lesen
00	ORB/IRB	Ausgangsregister B	Eingangsregister B
01	ORA/IRA	" A	" B
02	DDRB	Richtungsregister B	
03	DDRA	" A	
04	T1C-L	T1 LSByte-Speicher	T1 LSByte-Zähler
05	T1C-H	T1 MSByte-Zähler	
06	T1L-L	T1 LSByte-Speicher	
07	T1L-H	T1 MSByte-Speicher	
08	T2C-L	T2 LSByte-Speicher	T2 LSByte-Zähler
09	T2C-H	T2 MSByte-Zähler	
0A	SR	Schieberegister	
0B	ACR	Kontrollregister für Timer, Schieberegister, Eingangsspeicher	
0C	PCR	Kontrollregister für CA1, CA2, CB1, CB2	
0D	IFR	Interrupt Flag Register	
0E	IER	Interrupt Freigabe Register	
0F	ORA/IRA	wie Register 1 ohne Handshake	
10	ORB/IRB	Ausgangsregister B	Eingangsregister B
11	ORA/IRA	" A	" B
12	DDRB	Richtungsregister B	
13	DDRA	" A	
14	T1C-L	T1 LSByte-Speicher	T1 LSByte-Zähler
15	T1C-H	T1 MSByte-Zähler	
16	T1L-L	T1 LSByte-Speicher	
17	T1L-H	T1 MSByte-Speicher	
18	T2C-L	T2 LSByte-Speicher	T2 LSByte-Zähler
19	T2C-H	T2 MSByte-Zähler	
1A	SR	Schieberegister	
1B	ACR	Kontrollregister für Timer, Schieberegister, Eingangsspeicher	
1C	PCR	Kontrollregister für CA1, CA2, CB1, CB2	
1D	IFR	Interrupt Flag Register	
1E	IER	Interrupt Freigabe Register	
1F	ORA/IRA	wie Register 11 ohne Handshake	

Die absolute Registeradresse ergibt sich aus der Addition von eingestellter Basisadresse und der relativen Registeradresse.

Technische Daten

Format : Europakarte 100 x 160 mm

Anschluß : MCS-BUS über 64-pol. Messersteckverbinder
DIN 41612,
Bauform C, a+c bestückt

Peripherie- : 2 x 25 pol. D-Gerätestecker (Buchse)
anschluß Sandwichaufsatz über Buchsenleisten
Raster 2,54 mm möglich

Versorgung : über MCS-BUS-Anschluß
+ 5 V / ca. 300 mA

3. VIA Funktionsbeschreibung

Die folgenden Angaben sind dem Datenblatt der Firma Synertek entnommen (Stand April 1979).

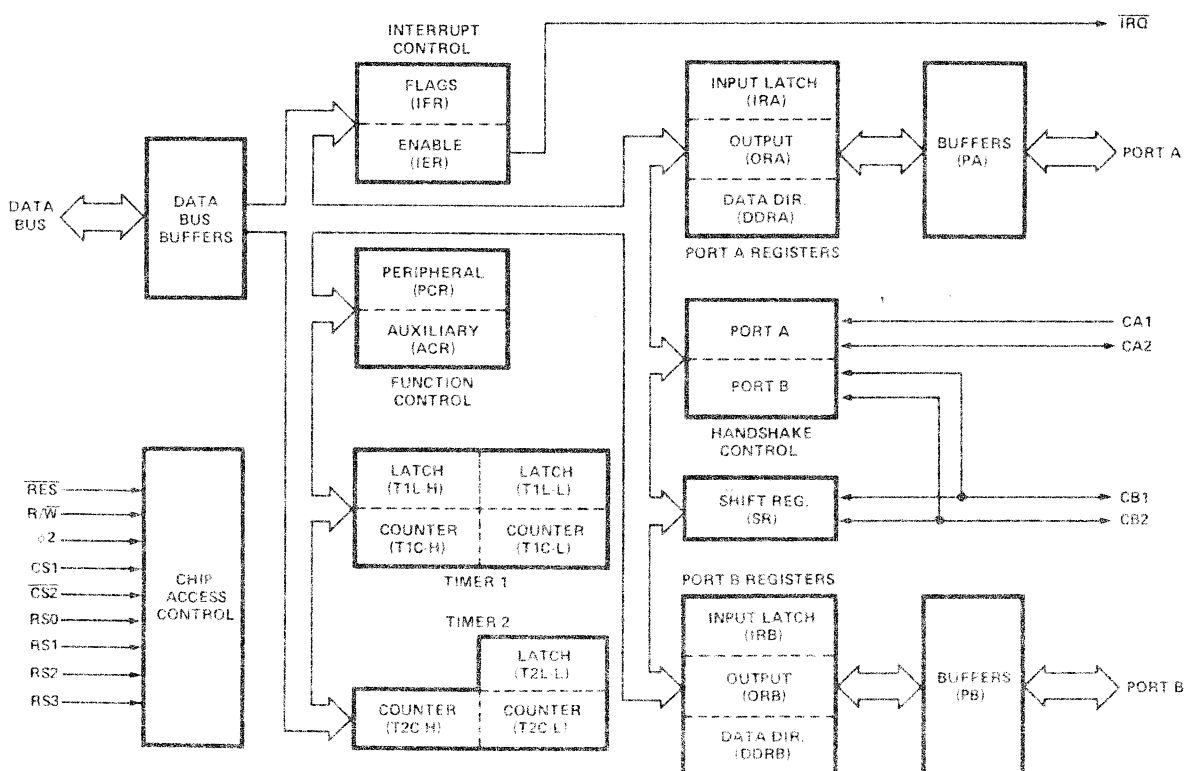
Bitte beachten Sie unbedingt die technischen Nachträge #38 und #106 der Firma Synertek am Ende des Kapitels.

PIN CONFIGURATION

VSS	1	40	CA1
PA0	2	39	CA2
PA1	3	38	RS0
PA2	4	37	RS1
PA3	5	36	RS2
PA4	6	35	RS3
PA5	7	34	RES
PA6	8	33	D0
PA7	9	32	D1
PB0	10	31	D2
PB1	11	30	D3
PB2	12	29	D4
PB3	13	28	D5
PB4	14	27	D6
PB5	15	26	D7
PB6	16	25	$\Phi 2$
PB7	17	24	CS1
CB1	18	23	CS2
CB2	19	22	R/W
VCC	20	21	IRQ

**Versatile
Interface Adapter
(VIA)**

**SY6522
SY6522A**



ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	V
Input Voltage	V_{IN}	-0.3 to +7.0	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages.

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0V \pm 5\%$, $T_A = 0-70^\circ\text{C}$ unless otherwise noted)

Symbol	Characteristic	Min.	Max.	Unit
V_{IH}	Input High Voltage (all except $\phi 2$)	2.4	V_{CC}	V
V_{CH}	Clock High Voltage	2.4	V_{CC}	V
V_{IL}	Input Low Voltage	-0.3	0.4	V
I_{IN}	Input Leakage Current — $V_{IN} = 0$ to 5 Vdc $R/\overline{W}$, $\overline{RES}$, RS0, RS1, RS2, RS3, CS1, $\overline{CS2}$, CA1, $\phi 2$	—	± 2.5	μA
I_{TSI}	Off-state Input Current — $V_{IN} = .4$ to 2.4V $V_{CC} = \text{Max}$, D0 to D7	—	± 10	μA
I_{IH}	Input High Current — $V_{IH} = 2.4V$ PA0-PA7, CA2, PB0-PB7, CB1, CB2	-100	—	μA
I_{IL}	Input Low Current — $V_{IL} = 0.4$ Vdc PA0-PA7, CA2, PB0-PB7, CB1, CB2	—	-1.6	mA
V_{OH}	Output High Voltage $V_{CC} = \text{min}$, $I_{load} = -100 \mu\text{A}$ PA0-PA7, CA2, PB0-PB7, CB1, CB2	2.4	—	V
V_{OL}	Output Low Voltage $V_{CC} = \text{min}$, $I_{load} = 1.6 \text{ mA}$	—	0.4	V
I_{OH}	Output High Current (Sourcing) $V_{OH} = 2.4V$ $V_{OH} = 1.5V$ (PB0-PB7)	-100 -1.0	— —	μA mA
I_{OL}	Output Low Current (Sinking) $V_{OL} = 0.4$ Vdc	1.6	—	mA
I_{OFF}	Output Leakage Current (Off state) $\overline{IRQ}$	—	10	μA
C_{IN}	Input Capacitance — $T_A = 25^\circ\text{C}$, $f = 1 \text{ MHz}$ ($R/\overline{W}$, $\overline{RES}$, RS0, RS1, RS2, RS3, CS1, $\overline{CS2}$, D0-D7, PA0-PA7, CA1, CA2, PB0-PB7) (CB1, CB2) ($\phi 2$ Input)	— — —	7.0 10 20	pF pF pF
C_{OUT}	Output Capacitance — $T_A = 25^\circ\text{C}$, $f = 1 \text{ MHz}$	—	10	pF
P_D	Power Dissipation	—	700	mW

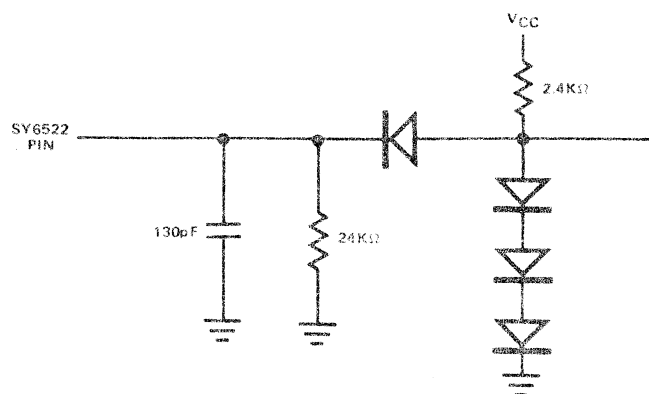


Figure 2. Test Load (for all Dynamic Parameters)

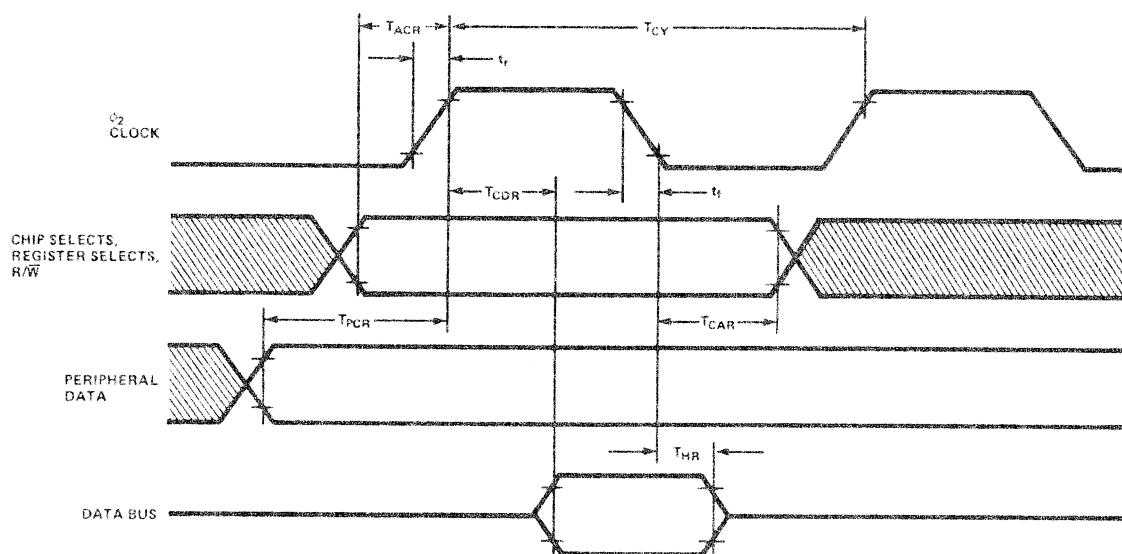


Figure 3. Read Timing Characteristics

READ TIMING CHARACTERISTICS (FIGURE 3)

Symbol	Parameter	SY6522		SY6522A		Unit
		Min.	Max.	Min.	Max.	
T_{CY}	Cycle Time	1	50	0.5	50	μs
T_{ACR}	Address Set-Up Time	180	—	90	—	ns
T_{CAR}	Address Hold Time	0	—	0	—	ns
T_{PCR}	Peripheral Data Set-Up Time	300	—	300	—	ns
T_{CDR}	Data Bus Delay Time	—	340	—	200	ns
T_{HR}	Data Bus Hold Time	10	—	10	—	ns

NOTE: $t_r, t_f = 10$ to $30ns$.

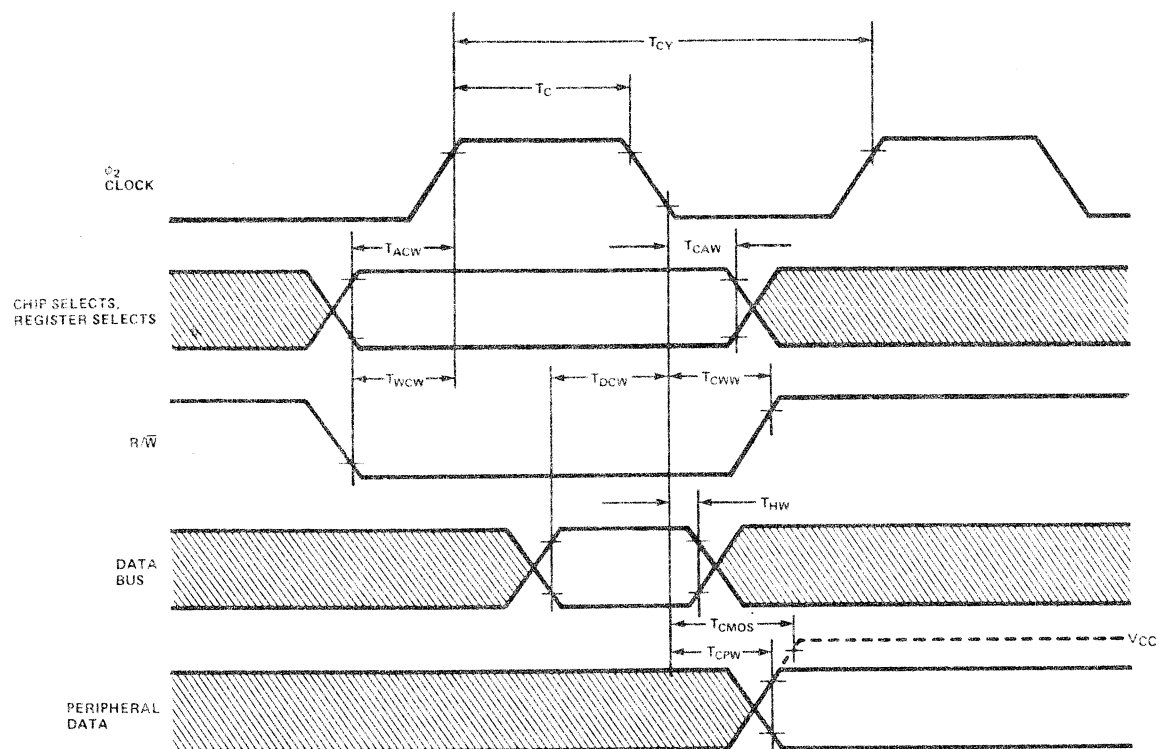


Figure 4. Write Timing Characteristics

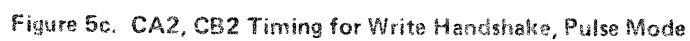
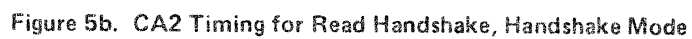
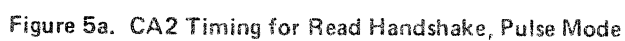
WRITE TIMING CHARACTERISTICS (FIGURE 4)

Symbol	Parameter	SY6522		SY6522A		Unit
		Min.	Max.	Min.	Max.	
T_{CY}	Cycle Time	1	50	0.50	50	μs
T_C	$\phi 2$ Pulse Width	0.44	25	0.22	25	μs
T_{ACW}	Address Set-Up Time	180	—	90	—	ns
T_{CAW}	Address Hold Time	0	—	0	—	ns
T_{WCW}	R/ $\bar{W}$ Set-Up Time	180	—	90	—	ns
T_{CWW}	R/ $\bar{W}$ Hold Time	0	—	0	—	ns
T_{DCW}	Data Bus Set-Up Time	300	—	200	—	ns
T_{HW}	Data Bus Hold Time	10	—	10	—	ns
T_{CPW}	Peripheral Data Delay Time	—	1.0	—	1.0	μs
T_{CMOS}	Peripheral Data Delay Time to CMOS Levels	—	2.0	—	2.0	μs

NOTE: t_r , t_f = 10 to 30ns.

PERIPHERAL INTERFACE CHARACTERISTICS

Symbol	Characteristic	Min.	Max.	Unit	Figure
t_r, t_f	Rise and Fall Time for CA1, CB1, CA2, and CB2 Input Signals	—	1.0	μs	—
T_{CA2}	Delay Time, Clock Negative Transition to CA2 Negative Transition (read handshake or pulse mode)	—	1.0	μs	5a, 5b
T_{RS1}	Delay Time, Clock Negative Transition to CA2 Positive Transition (pulse mode)	—	1.0	μs	5a
T_{RS2}	Delay Time, CA1 Active Transition to CA2 Positive Transition (handshake mode)	—	2.0	μs	5b
T_{WHS}	Delay Time, Clock Positive Transition to CA2 or CB2 Negative Transition (write handshake)	0.05	1.0	μs	5c, 5d
T_{DS}	Delay Time, Peripheral Data Valid to CB2 Negative Transition	0.20	1.5	μs	5c, 5d
T_{RS3}	Delay Time, Clock Positive Transition to CA2 or CB2 Positive Transition (pulse mode)	—	1.0	μs	5c
T_{RS4}	Delay Time, CA1 or CB1 Active Transition to CA2 or CB2 Positive Transition (handshake mode)	—	2.0	μs	5d
T_{21}	Delay Time Required from CA2 Output to CA1 Active Transition (handshake mode)	400	—	ns	5d
T_{IL}	Set-up Time, Peripheral Data Valid to CA1 or CB1 Active Transition (input latching)	300	—	ns	5e
T_{SR1}	Shift-Out Delay Time — Time from ϕ_2 Falling Edge to CB2 Data Out	—	300	ns	5f
T_{SR2}	Shift-In Setup Time — Time from CB2 Data In to ϕ_2 Rising Edge	300	—	ns	5g
T_{SR3}	External Shift Clock (CB1) Setup Time Relative To ϕ_2 Trailing Edge	100	T_{CY}	ns	5g
T_{IPW}	Pulse Width — PB6 Input Pulse	2	—	μs	5i
T_{ICW}	Pulse Width — CB1 Input Clock	2	—	μs	5h
I_{IPS}	Pulse Spacing — PB6 Input Pulse	2	—	μs	5i
I_{ICS}	Pulse Spacing — CB1 Input Pulse	2	—	μs	5h



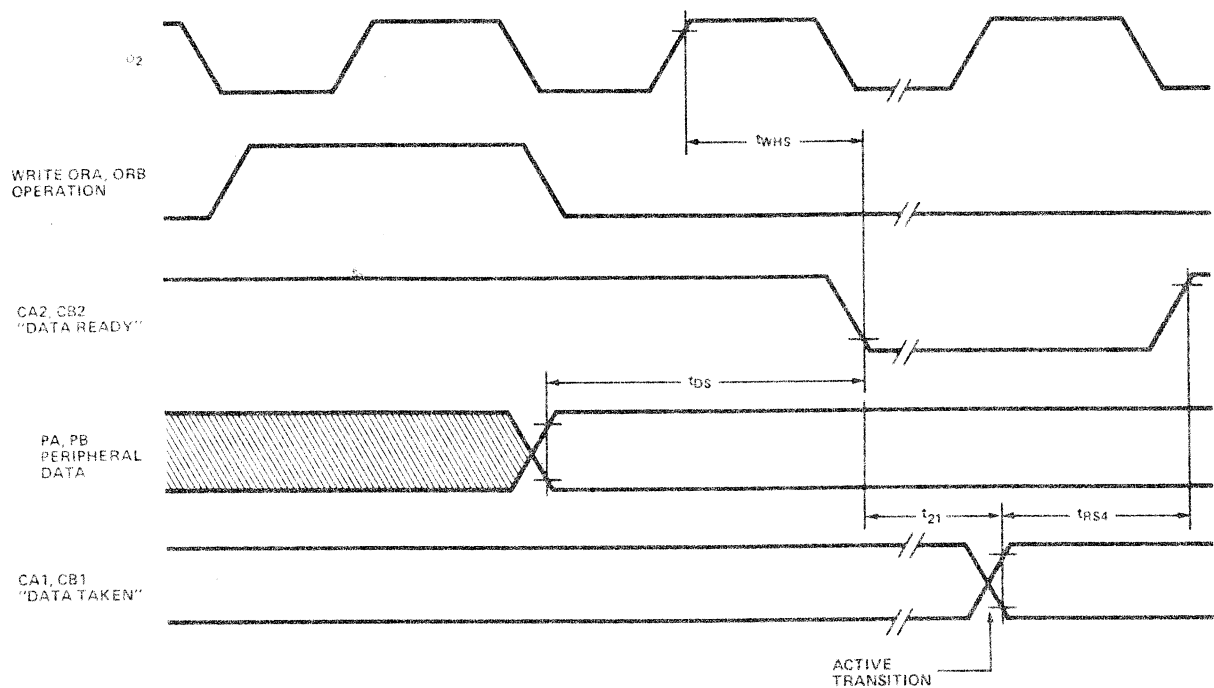


Figure 5d. CA2, CB2 Timing for Write Handshake, Handshake Mode

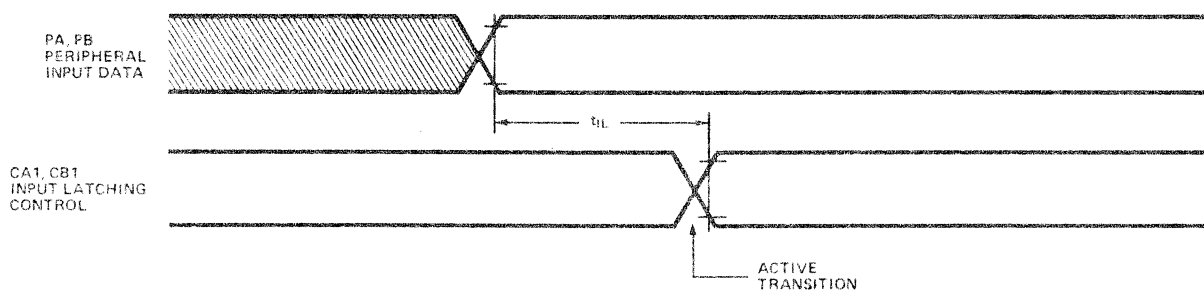


Figure 5e. Peripheral Data Input Latching Timing

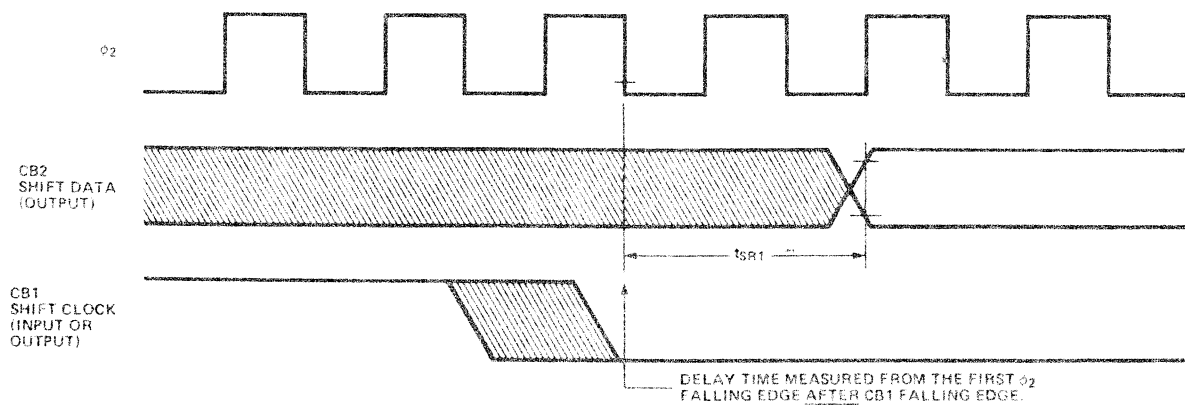
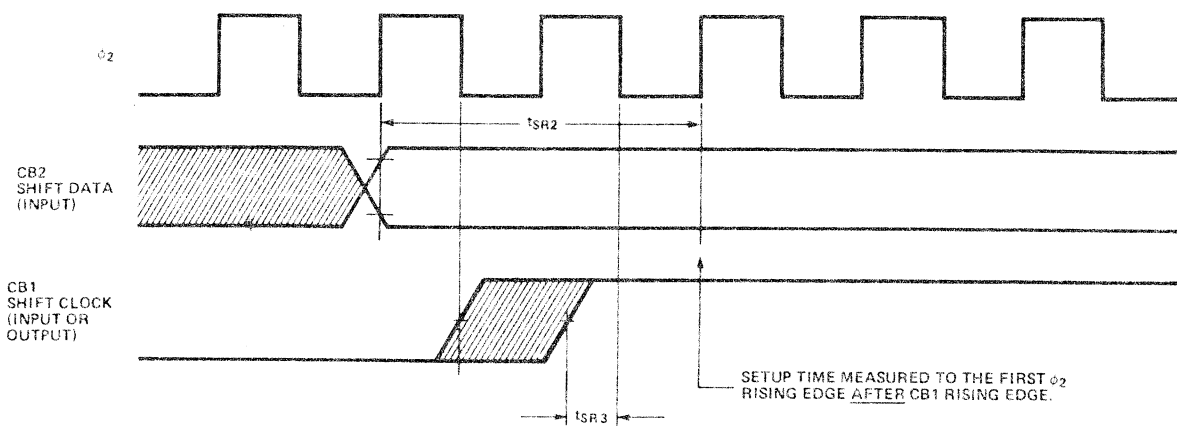


Figure 5f. Timing for Shift Out with Internal or External Shift Clocking



! Anhang beachten!

Figure 5g. Timing for Shift In with Internal or External Shift Clocking

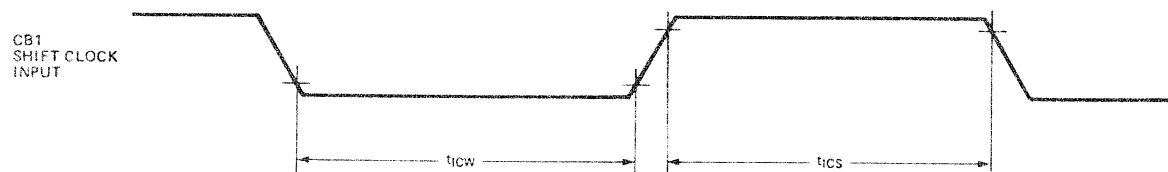


Figure 5h. External Shift Clock Timing

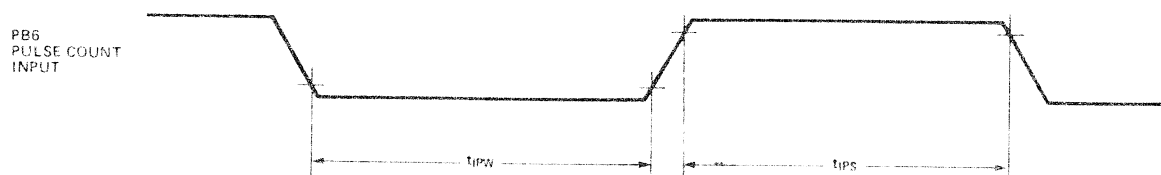


Figure 5i. Pulse Count Input Timing

PIN DESCRIPTIONS

RES (Reset)

The reset input clears all internal registers to logic 0 (except T1 and T2 latches and counters and the Shift Register). This places all peripheral interface lines in the input state, disables the timers, shift register, etc. and disables interrupting from the chip.

 $\phi 2$ (Input Clock)

The input clock is the system $\phi 2$ clock and is used to trigger all data transfers between the system processor and the SY6522.

R/W (Read/Write)

The direction of the data transfers between the SY6522 and the system processor is controlled by the R/W line. If R/W is low, data will be transferred out of the processor into the selected SY6522 register (write operation). If R/W is high and the chip is selected, data will be transferred out of the SY6522 (read operation).

DB0-DB7 (Data Bus)

The eight bi-directional data bus lines are used to transfer data between the SY6522 and the system processor. During read cycles, the contents of the selected SY6522 register are placed on the data bus lines and transferred into the processor. During write cycles, these lines are high-impedance inputs and data is transferred from the processor into the selected register. When the SY6522 is unselected, the data bus lines are high-impedance.

CS1, $\overline{\text{CS2}}$ (Chip Selects)

The two chip select inputs are normally connected to processor address lines either directly or through decoding. The selected SY6522 register will be accessed when CS1 is high and $\overline{\text{CS2}}$ is low.

RS0-RS3 (Register Selects)

The four Register Select inputs permit the system processor to select one of the 16 internal registers of the SY6522, as shown in Figure 6.

Register Number	RS Coding				Register Desig.	Description	
	RS3	RS2	RS1	RS0		Write	Read
0	0	0	0	0	ORB/IRB	Output Register "B"	Input Register "B"
1	0	0	0	1	ORA/IRA	Output Register "A"	Input Register "A"
2	0	0	1	0	DDRB	Data Direction Register "B"	
3	0	0	1	1	DDRA	Data Direction Register "A"	
4	0	1	0	0	T1C-L	T1 Low-Order Latches	T1 Low-Order Counter
5	0	1	0	1	T1C-H	T1 High-Order Counter	
6	0	1	1	0	T1L-L	T1 Low-Order Latches	
7	0	1	1	1	T1L-H	T1 High-Order Latches	
8	1	0	0	0	T2C-L	T2 Low-Order Latches	T2 Low-Order Counter
9	1	0	0	1	T2C-H	T2 High-Order Counter	
10	1	0	1	0	SR	Shift Register	
11	1	0	1	1	ACR	Auxiliary Control Register	
12	1	1	0	0	PCR	Peripheral Control Register	
13	1	1	0	1	IFR	Interrupt Flag Register	
14	1	1	1	0	IER	Interrupt Enable Register	
15	1	1	1	1	ORA/IRA	Same as Reg 1 Except No "Handshake"	

Figure 6. SY6522 Internal Register Summary

IRQ (Interrupt Request)

The Interrupt Request output goes low whenever an internal interrupt flag is set and the corresponding interrupt enable bit is a logic 1. This output is "open-drain" to allow the interrupt request signal to be "wire-or'ed" with other equivalent signals in the system.

PA0-PA7 (Peripheral A Port)

The Peripheral A port consists of 8 lines which can be individually programmed to act as inputs or outputs under control of a Data Direction Register. The polarity of output pins is controlled by an Output Register and input data may be latched into an internal register under control of the CA1 line. All of these modes of operation are controlled by the system processor through the internal control registers. These lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode. Figure 7 illustrates the output circuit.

CA1, CA2 (Peripheral A Control Lines)

The two Peripheral A control lines act as interrupt inputs or as handshake outputs. Each line controls an internal interrupt flag with a corresponding interrupt enable bit. In addition, CA1 controls the latching of data on Peripheral A port input lines. CA1 is a high-impedance input only while CA2 represents one standard TTL load in the input mode. CA2 will drive one standard TTL load in the output mode.

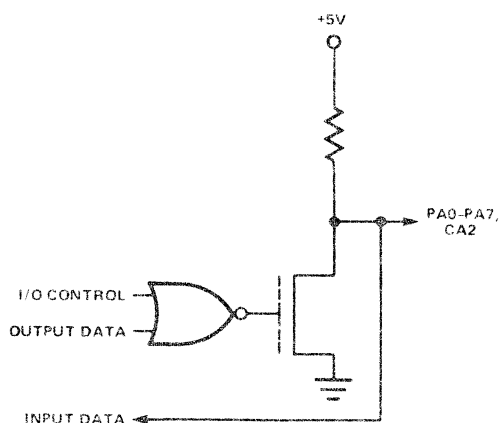


Figure 7. Peripheral A Port Output Circuit

PB0-PB7 (Peripheral B Port)

The Peripheral B port consists of eight bi-directional lines which are controlled by an output register and a data direction register in much the same manner as the

PA port. In addition, the polarity of the PB7 output signal can be controlled by one of the interval timers while the second timer can be programmed to count pulses on the PB6 pin. Peripheral B lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode. In addition, they are capable of sourcing 1.0mA at 1.5VDC in the output mode to allow the outputs to directly drive Darlington transistor circuits. Figure 8 is the circuit schematic.

CB1, CB2 (Peripheral B Control Lines)

The Peripheral B control lines act as interrupt inputs or as handshake outputs. As with CA1 and CA2, each line controls an interrupt flag with a corresponding interrupt enable bit. In addition, these lines act as a serial port under control of the Shift Register. These lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode. Unlike PB0-PB7, CB1 and CB2 cannot drive Darlington transistor circuits.

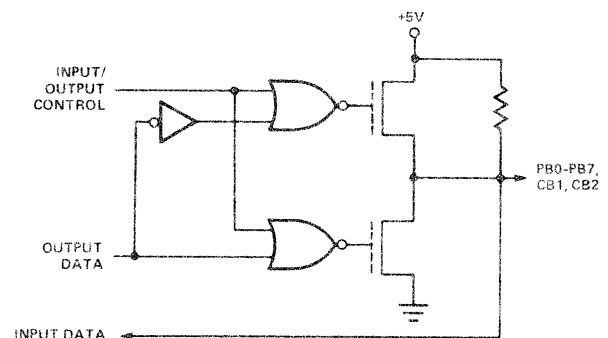


Figure 8. Peripheral B Port Output Circuit

FUNCTIONAL DESCRIPTION

Port A and Port B Operation

Each 8-bit peripheral port has a Data Direction Register (DDRA, DDRB) for specifying whether the peripheral pins are to act as inputs or outputs. A 0 in a bit of the Data Direction Register causes the corresponding peripheral pin to act as an input. A 1 causes the pin to act as an output.

Each peripheral pin is also controlled by a bit in the Output Register (ORA, ORB) and an Input Register (IRA, IRB). When the pin is programmed as an output, the voltage on the pin is controlled by the cor-

responding bit of the Output Register. A 1 in the Output Register causes the output to go high, and a "0" causes the output to go low. Data may be written into Output Register bits corresponding to pins which are programmed as inputs. In this case, however, the output signal is unaffected.

Reading a peripheral port causes the contents of the Input Register (IRA, IRB) to be transferred onto the Data Bus. With input latching disabled, IRA will always reflect the levels on the PA pins. With input latching enabled, IRA will reflect the levels on the PA pins at the time the latching occurred (via CA1).

The IRB register operates similar to the IRA register. However, for pins programmed as outputs there is a difference. When reading IRA, the level on the pin determines whether a 0 or a 1 is sensed. When reading IRB, however, the bit stored in the output register, ORB, is the bit sensed. Thus, for outputs which have large loading effects and which pull an output "1" down or which pull an output "0" up, reading IRA may result in reading a "0" when a "1" was actually programmed, and reading a "1" when a "0" was programmed. Reading IRB, on the other hand, will read the "1" or "0" level actually programmed, no matter what the loading on the pin.

Figures 9, 10, and 11 illustrate the formats of the port registers. In addition, the input latching modes are selected by the Auxiliary Control Register (Figure 16.)

Handshake Control of Data Transfers

The SY6522 allows positive control of data transfers between the system processor and peripheral devices

REG 0 – ORB/IRB

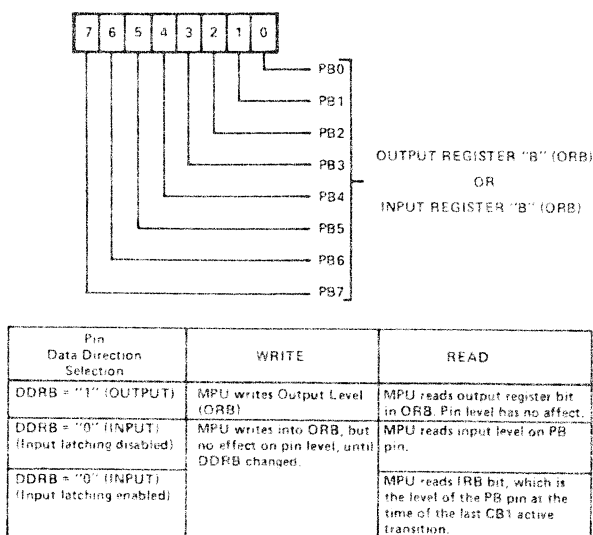
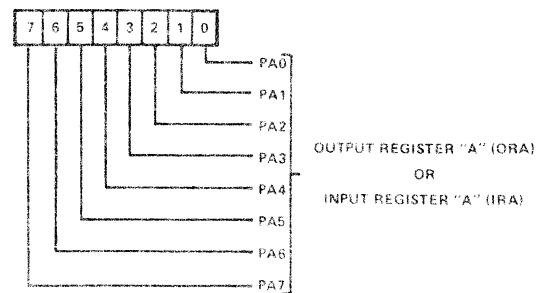


Figure 9. Output Register B (ORB), Input Register B (IRB)

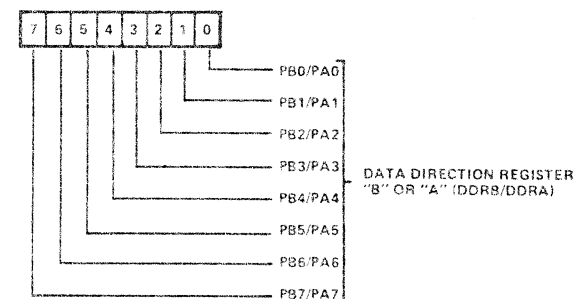
REG 1 – ORA/IRA



Pin Data Direction Selection	WRITE	READ
DDRA = "1" (OUTPUT) (Input latching disabled)	MPU writes Output Level (ORA)	MPU reads level on PA pin.
DDRA = "1" (OUTPUT) (Input latching enabled)		MPU reads IRA bit which is the level of the PA pin at the time of the last CA1 active transition.
DDRA = "0" (INPUT) (Input latching disabled)	MPU writes into ORA, but no effect on pin level, until DDRA changed.	MPU reads level on PA pin.
DDRA = "0" (INPUT) (Input latching enabled)		MPU reads IRA bit which is the level of the PA pin at the time of the last CA1 active transition.

Figure 10. Output Register A (ORA), Input Register A (IRA)

REG 2 (DDRB) AND REG 3 (DDRA)



- "0" ASSOCIATED PB/PA PIN IS AN INPUT (HIGH IMPEDANCE)
 "1" ASSOCIATED PB/PA PIN IS AN OUTPUT, WHOSE LEVEL IS DETERMINED BY ORB/ORA REGISTER BIT

Figure 11. Data Direction Registers (DDRB, DDRA)

through the operation of "handshake" lines. Port A lines (CA1, CA2) handshake data on both a read and a write operation while the Port B lines (CB1, CB2) handshake on a write operation only.

Read Handshake

Positive control of data transfers from peripheral devices into the system processor can be accomplished very effectively using Read Handshaking. In this case, the peripheral device must generate the equivalent of a "Data Ready" signal to the processor signifying that valid data is present on the peripheral port. This signal normally interrupts the processor, which then reads the data, causing generation of a "Data Taken" signal. The peripheral device responds by making new data available. This process continues until the data transfer is complete.

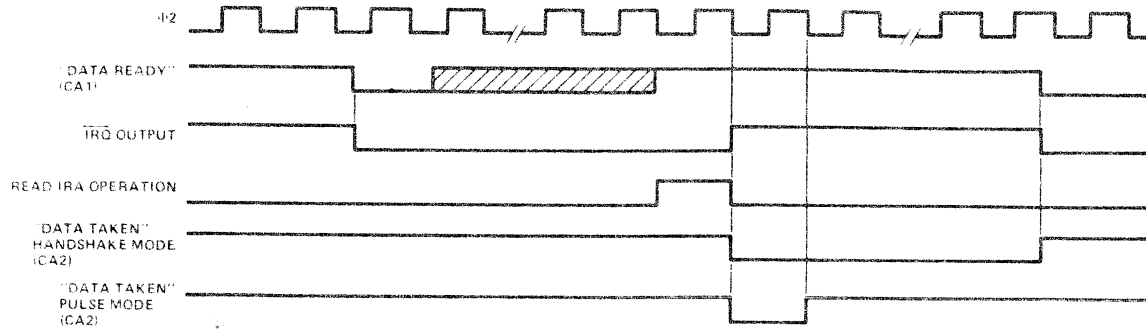


Figure 12. Read Handshake Timing (Port A, Only)

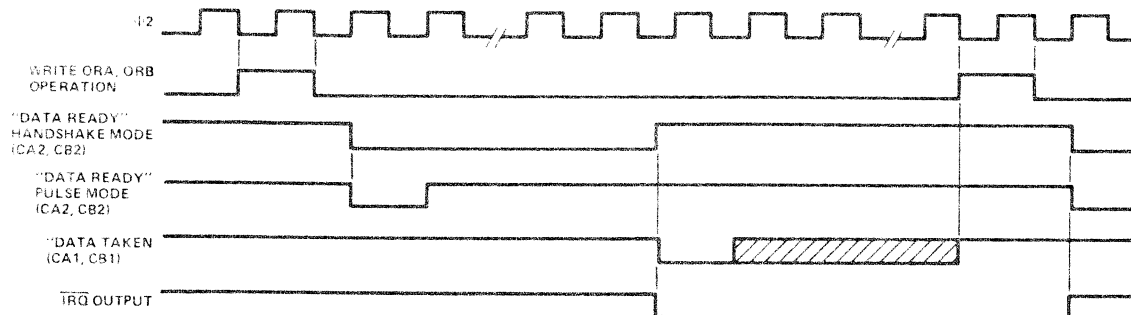


Figure 13. Write Handshake Timing

In the SY6522, automatic "Read" Handshaking is possible on the Peripheral A port only. The CA1 interrupt input pin accepts the "Data Ready" signal and CA2 generates the "Data Taken" signal. The "Data Ready" signal will set an internal flag which may interrupt the processor or which may be polled under program control. The "Data Taken" signal can either be a pulse or a level which is set low by the system processor and is cleared by the "Data Ready" signal. These options are shown in Figure 12 which illustrates the normal Read Handshaking sequence.

Write Handshake

The sequence of operations which allows handshaking data from the system processor to a peripheral device is very similar to that described for Read Handshaking. However, for Write Handshaking, the SY6522 generates the "Data Ready" signal and the peripheral device must respond with the "Data Taken" signal. This can be accomplished on both the PA port and the PB port on the SY6522. CA2 or CB2 act as a "Data Ready" output in either the handshake mode or pulse mode and CA1 or CB1 accept the "Data Taken" signal from the peripheral device, setting the interrupt flag and cleaning the "Data Ready" output. This sequence is shown in Figure 13.

Selection of operating modes for CA1, CA2, CB1, and CB2 is accomplished by the Peripheral Control Register (Figure 14).

Timer Operation

Interval Timer T1 consists of two 8-bit latches and a 16-bit counter. The latches are used to store data which is to be loaded into the counter. After loading, the counter decrements at $\phi 2$ clock rate. Upon reaching zero, an interrupt flag will be set, and $\overline{TRQ}$ will go low if the interrupt is enabled. The timer will then disable any further interrupts, or will automatically transfer the contents of the latches into the counter and will continue to decrement. In addition, the timer may be programmed to invert the output signal on a peripheral pin each time it "times-out". Each of these modes is discussed separately below.

The T1 counter is depicted in Figure 15 and the latches in Figure 16.

REG 12 - PERIPHERAL CONTROL REGISTER

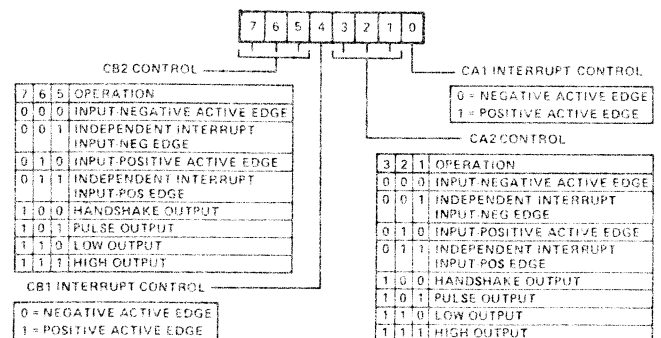
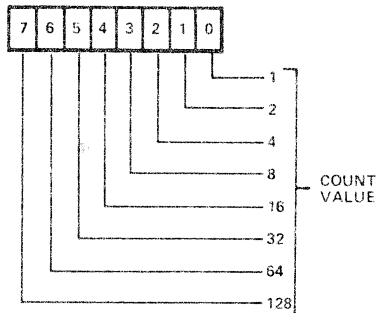


Figure 14. CA1, CA2, CB1, CB2 Control

Two bits are provided in the Auxiliary Control Register (bits 6 and 7) to allow selection of the T1 operating

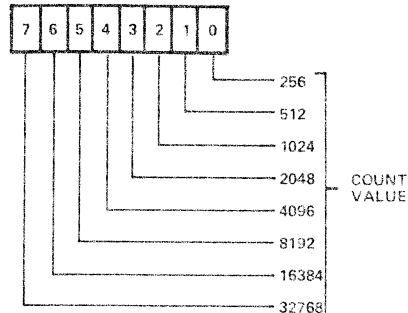
modes. The four possible modes are depicted in Figure 17.

REG 4 – TIMER 1 LOW-ORDER COUNTER



WRITE – 8 BITS LOADED INTO T1 LOW-ORDER LATCHES. LATCH CONTENTS ARE TRANSFERRED INTO LOW-ORDER COUNTER AT THE TIME THE HIGH-ORDER COUNTER IS LOADED (REG 5).
READ – 8 BITS FROM T1 LOW-ORDER COUNTER TRANSFERRED TO MPU. IN ADDITION, T1 INTERRUPT FLAG IS RESET (BIT 6 IN INTERRUPT FLAG REGISTER).

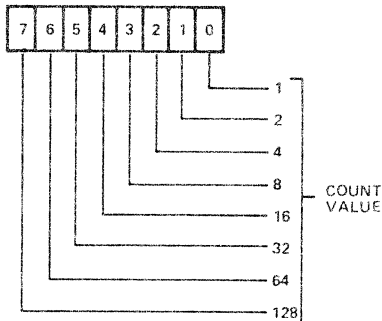
REG 5 – TIMER 1 HIGH-ORDER COUNTER



WRITE – 8 BITS LOADED INTO T1 HIGH-ORDER LATCHES. ALSO, AT THIS TIME BOTH HIGH AND LOW-ORDER LATCHES TRANSFERRED INTO T1 COUNTER. T1 INTERRUPT FLAG ALSO IS RESET.
READ – 8 BITS FROM T1 HIGH-ORDER COUNTER TRANSFERRED TO MPU.

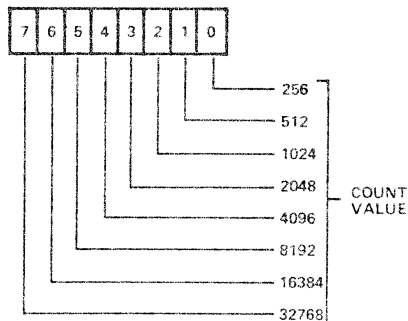
Figure 15. T1 Counter Registers

REG 6 – TIMER 1 LOW-ORDER LATCHES



WRITE – 8 BITS LOADED INTO T1 LOW-ORDER LATCHES. THIS OPERATION IS NO DIFFERENT THAT A WRITE INTO REG 4.
READ – 8 BITS FROM T1 LOW-ORDER LATCHES TRANSFERRED TO MPU. UNLIKE REG 4 OPERATION, THIS DOES NOT CAUSE RESET OF T1 INTERRUPT FLAG.

REG 7 – TIMER 1 HIGH-ORDER LATCHES



WRITE – 8 BITS LOADED INTO T1 HIGH-ORDER LATCHES. UNLIKE REG 4 OPERATION NO LATCH-TO-COUNTER TRANSFERS TAKE PLACE.
READ – 8 BITS FROM T1 HIGH-ORDER LATCHES TRANSFERRED TO MPU.

Figure 16. T1 Latch Registers

REG 11 – AUXILIARY CONTROL REGISTER

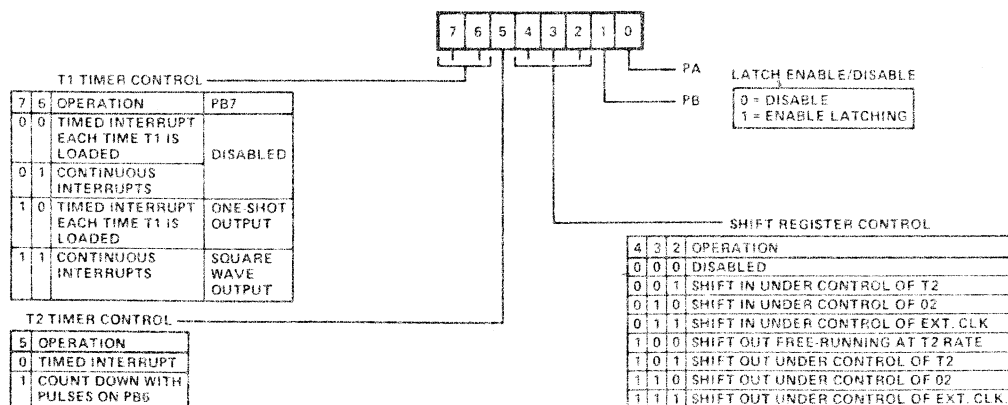


Figure 17. Auxiliary Control Register

Note: The processor does not write directly into the low order counter (T1C-L). Instead, this half of the counter is loaded automatically from the low order latch when the processor writes into the high order counter. In fact, it may not be necessary to write to the low order counter in some applications since the timing operation is triggered by writing to the high order counter.

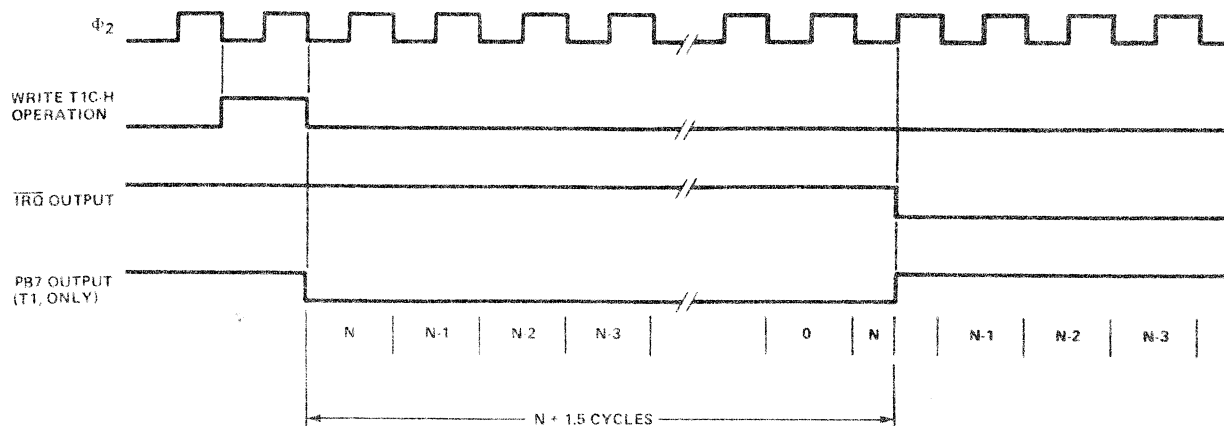


Figure 18. Timer 1 and Timer 2 One-Shot Mode Timing

Timer 1 One-Shot Mode

The interval timer one-shot mode allows generation of a single interrupt for each timer load operation. As with any interval timer, the delay between the "write T1C-H" operation and generation of the processor interrupt is a direct function of the data loaded into the timing counter. In addition to generating a single interrupt, Timer 1 can be programmed to produce a single negative pulse on the PB7 peripheral pin. With the output enabled (ACR7=1) a "write T1C-H" operation will cause PB7 to go low. PB7 will return high when Timer 1 times out. The result is a single programmable width pulse.

In the one-shot mode, writing into the high order latch has no effect on the operation of Timer 1. However, it will be necessary to assure that the low order latch contains the proper data before initiating the count-down with a "write T1C-H" operation. When the processor writes into the high order counter, the T1 interrupt flag will be cleared, the contents of the low order latch will be transferred into the low order counter, and the timer will begin to decrement at system clock rate. If the PB7 output is enabled, this signal will go low on the phase two following the write operation. When the counter reaches zero, the T1 interrupt flag will be set, the $\overline{\text{TRQ}}$ pin will go low (interrupt enabled), and the signal on PB7 will go high. At this time the counter will continue to decrement at system clock rate. This allows the system processor to read the contents of the counter to determine the time since interrupt. However, the T1 interrupt flag cannot be set again unless it has been cleared as described in this specification.

Timing for the SY6522 interval timer one-shot modes is shown in Figure 18.

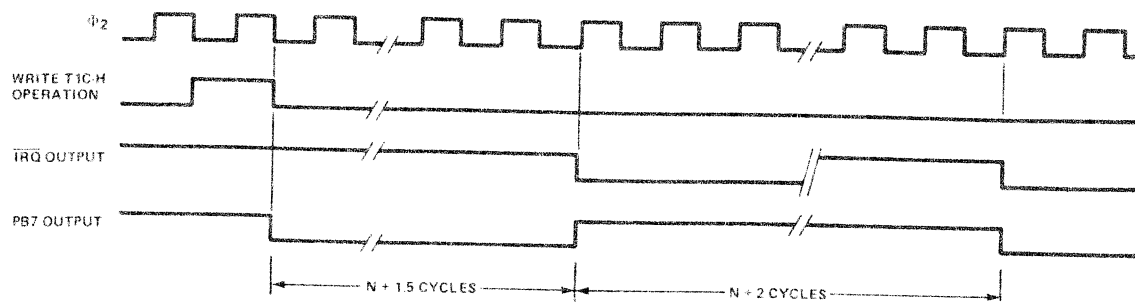
Timer 1 Free-Run Mode

The most important advantage associated with the latches in T1 is the ability to produce a continuous

series of evenly spaced interrupts and the ability to produce a square wave on PB7 whose frequency is not affected by variations in the processor interrupt response time. This is accomplished in the "free-running" mode.

In the free-running mode, the interrupt flag is set and the signal on PB7 is inverted each time the counter reaches zero. However, instead of continuing to decrement from zero after a time-out, the timer automatically transfers the contents of the latch into the counter (16 bits) and continues to decrement from there. The interrupt flag can be cleared by writing T1C-H, by reading T1C-L, or by writing directly into the flag as described later. However, it is not necessary to rewrite the timer to enable setting the interrupt flag on the next time-out.

All interval timers in the SY6522 are "re-triggerable". Rewriting the counter will always re-initialize the time-out period. In fact, the time-out can be prevented completely if the processor continues to rewrite the timer before it reaches zero. Timer 1 will operate in this manner if the processor writes into the high order counter (T1C-H). However, by loading the latches only, the processor can access the timer during each down-counting operation without affecting the time-out in process. Instead, the data loaded into the latches will determine the length of the next time-out period. This capability is particularly valuable in the free-running mode with the output enabled. In this mode, the signal on PB7 is inverted and the interrupt flag is set with each time-out. By responding to the interrupts with new data for the latches, the processor can determine the period of the next half cycle during each half cycle of the output signal on PB7. In this manner, very complex waveforms can be generated. Timing for the free-running mode is shown in Figure 19.



Note: A precaution to take in the use of PB7 as the timer output concerns the Data Direction Register contents for PB7. Both DDRB bit 7 and ACR bit 7 must be 1 for PB7 to function as the timer output. If one is 1 and the other is 0, then PB7 functions as a normal output pin, controlled by ORB bit 7.

Figure 19. Timer 1 Free-Run Mode Timing

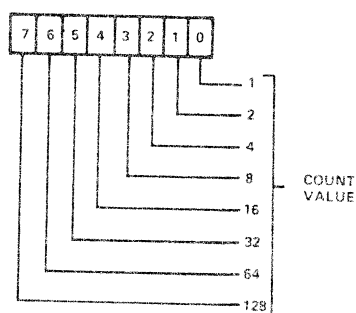
Timer 2 Operation

Timer 2 operates as an interval timer (in the "one-shot" mode only), or as a counter for counting negative pulses on the PB6 peripheral pin. A single control bit is provided in the Auxiliary Control Register to select between these two modes. This timer is comprised of a "write-only" low-order latch (T2L-L), a "read-only" low-order counter and a read/write high order counter. The counter registers act as a 16-bit counter which decrements at $\Phi 2$ rate. Figure 20 illustrates the T2 Counter Registers.

Timer 2 One-Shot Mode

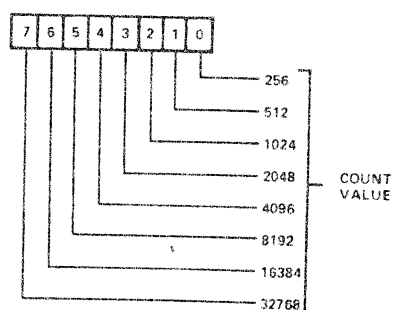
As an interval timer, T2 operates in the "one-shot" mode similar to Timer 1. In this mode, T2 provides a single interrupt for each "write T2C-H" operation. After timing out, the counter will continue to decrement. However, setting of the interrupt flag will be disabled after initial time-out so that it will not be set by the counter continuing to decrement through zero. The processor must rewrite T2C-H to enable setting of the interrupt flag. The interrupt flag is cleared by reading T2C-L or by writing T2C-H. Timing for this operation is shown in Figure 18.

REG 8 — TIMER 2 LOW-ORDER COUNTER



WRITE — 8 BITS LOADED INTO T2 LOW ORDER LATCHES
READ — 8 BITS FROM T2 LOW-ORDER COUNTER TRANSFERRED TO MPU. T2 INTERRUPT FLAG IS RESET.

REG 9 — TIMER 2 HIGH-ORDER COUNTER



WRITE — 8 BITS LOADED INTO T2 HIGH-ORDER COUNTER. ALSO, LOW-ORDER LATCHES TRANSFERRED TO LOW-ORDER COUNTER. IN ADDITION, T2 INTERRUPT FLAG IS RESET.
READ — 8 BITS FROM T2 HIGH-ORDER COUNTER TRANSFERRED TO MPU.

Figure 20. T2 Counter Registers

Timer 2 Pulse Counting Mode

In the pulse counting mode, T2 serves primarily to count a predetermined number of negative-going pulses on PB6. This is accomplished by first loading a number into T2. Writing into T2C-H clears the interrupt flag and allows the counter to decrement each time a pulse is applied to PB6. The interrupt flag will be set when T2 reaches zero. At this time the counter will continue to decrement with each pulse on PB6. However, it is necessary to rewrite T2C-H to allow the interrupt flag to set on subsequent down-counting operations. Timing for this mode is shown in Figure 21. The pulse must be low on the leading edge of Φ_2 .

Shift Register Operation

The Shift Register (SR) performs serial data transfers into and out of the CB2 pin under control of an internal modulo-8 counter. Shift pulses can be applied to the CB1 pin from an external source or, with the proper mode selection, shift pulses generated internally will appear on the CB1 pin for controlling external devices.

The control bits which select the various shift register operating modes are located in the Auxiliary Control Register. Figure 22 illustrates the configuration of the SR data bits and the SR control bits of the ACR.

Figures 23 and 24 illustrate the operation of the various shift register modes.

Interrupt Operation

Controlling interrupts within the SY6522 involves three principal operations. These are flagging the interrupts, enabling interrupts and signaling to the processor that an active interrupt exists within the chip. Interrupt flags are set by interrupting conditions which exist within the chip or on inputs to the chip. These flags normally remain set until the interrupt has been serviced. To determine the source of an interrupt, the microprocessor must examine these flags in order from highest to lowest priority. This is accomplished by reading the flag register into the processor accumulator, shifting this register either right or left and then using conditional branch instructions to detect an active interrupt.

Associated with each interrupt flag is an interrupt enable bit. This can be set or cleared by the processor to enable interrupting the processor from the corresponding interrupt flag. If an interrupt flag is set to a logic 1 by an interrupting condition, and the corresponding interrupt enable bit is set to a 1, the Interrupt Request Output ($\overline{\text{IRQ}}$) will go low. $\overline{\text{IRQ}}$ is an "open-collector" output which can be "wire-or'ed" with other devices in the system to interrupt the processor.

In the SY6522, all the interrupt flags are contained in one register. In addition, bit 7 of this register will be read as a logic 1 when an interrupt exists within the chip. This allows very convenient polling of several devices within a system to locate the source of an interrupt.

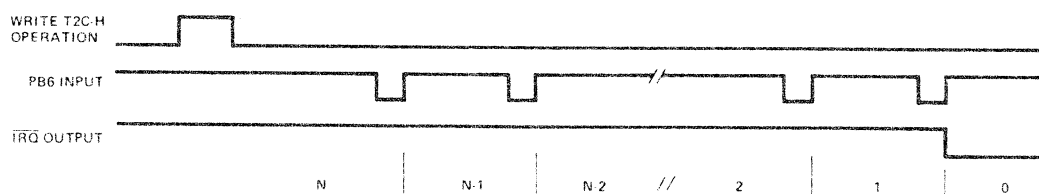
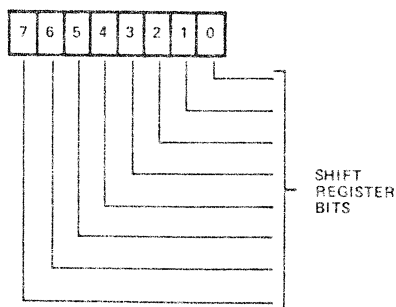


Figure 21. Timer 2 Pulse Counting Mode

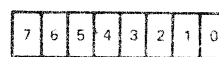
REG 10 – SHIFT REGISTER



NOTES:

1. WHEN SHIFTING OUT, BIT 7 IS THE FIRST BIT OUT AND SIMULTANEOUSLY IS ROTATED BACK INTO BIT 0.
2. WHEN SHIFTING IN, BITS INITIALLY ENTER BIT 0 AND ARE SHIFTED TOWARDS BIT 7.

REG 11 – AUXILIARY CONTROL REGISTER



4	3	2	OPERATION
0	0	0	DISABLED
0	0	1	SHIFT IN UNDER CONTROL OF T2
0	1	0	SHIFT IN UNDER CONTROL OF Φ_2
0	1	1	SHIFT IN UNDER CONTROL OF EXT CLK
1	0	0	SHIFT OUT FREE-RUNNING AT T2 RATE
1	0	1	SHIFT OUT UNDER CONTROL OF T2
1	1	0	SHIFT OUT UNDER CONTROL OF Φ_2
1	1	1	SHIFT OUT UNDER CONTROL OF EXT CLK

Figure 22. SR and ACR Control Bits

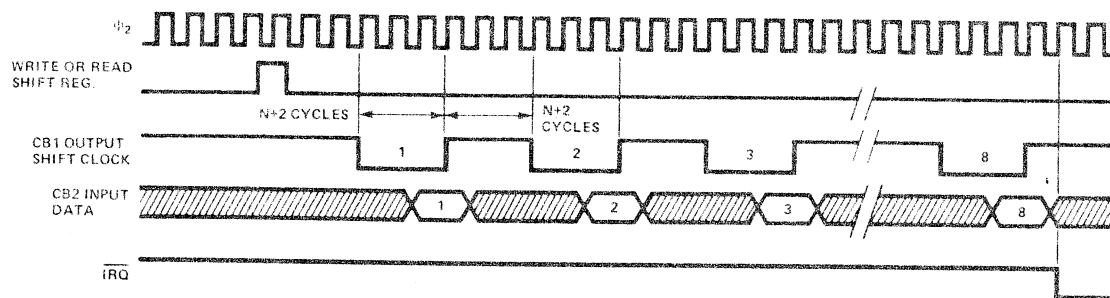
SR Disabled (000)

The 000 mode is used to disable the Shift Register. In this mode the microprocessor can write or read the SR, but the shifting operation is disabled and operation of CB1 and CB2 is controlled by the appropriate bits in the Peripheral Control Register (PCR). In this mode the SR Interrupt Flag is disabled (held to a logic 0).

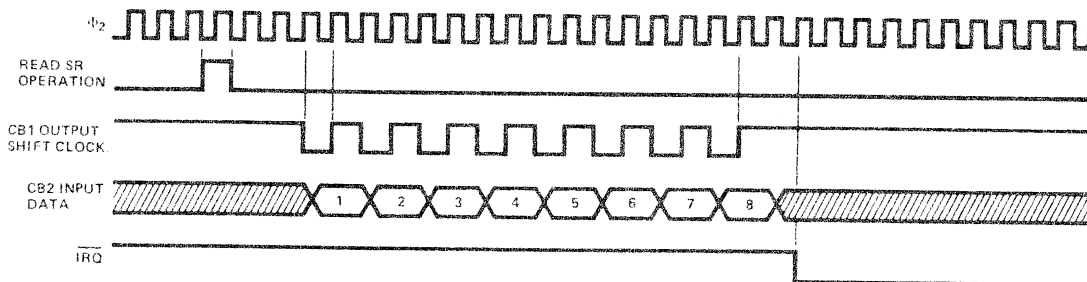
Shift in Under Control of T2 (001)

In the 001 mode the shifting rate is controlled by the low order 8 bits of T2. Shift pulses are generated on the CB1 pin to control shifting in external devices. The time between transitions of this output clock is a function of the system clock period and the contents of the low order T2 latch (N).

The shifting operation is triggered by writing or reading the shift register. Data is shifted first into the low order bit of SR and is then shifted into the next higher order bit of the shift register on the negative-going edge of each clock pulse. The input data should change before the positive-going edge of the CB1 clock pulse. This data is shifted into the shift register during the ϕ_2 clock cycle following the positive-going edge of the CB1 clock pulse. After 8 CB1 clock pulses, the shift register interrupt flag will be set and $\overline{\text{IRQ}}$ will go low.

**Shift in Under Control of ϕ_2 (010) ! Anhang beachten!**

In mode 010 the shift rate is a direct function of the system clock frequency. CB1 becomes an output which generates shift pulses for controlling external devices. Timer 2 operates as an independent interval timer and has no effect on SR. The shifting operation is triggered by reading or writing the Shift Register. Data is shifted first into bit 0 and is then shifted into the next higher order bit of the shift register on the trailing edge of each ϕ_2 clock pulse. After 8 clock pulses, the shift register interrupt flag will be set, and the output clock pulses on CB1 will stop.

**Shift in Under Control of External CB1 Clock (011) ! Anhang beachten!**

In mode 011 CB1 becomes an input. This allows an external device to load the shift register at its own pace. The shift register counter will interrupt the processor each time 8 bits have been shifted in. However, the shift register counter does not stop the shifting operation; it acts simply as a pulse counter. Reading or writing the Shift Register resets the Interrupt flag and initializes the SR counter to count another 8 pulses.

Note that the data is shifted during the first system clock cycle following the positive-going edge of the CB1 shift pulse. For this reason, data must be held stable during the first full cycle following CB1 going high.

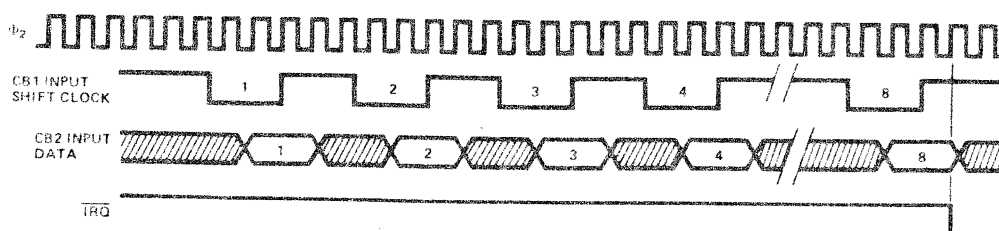
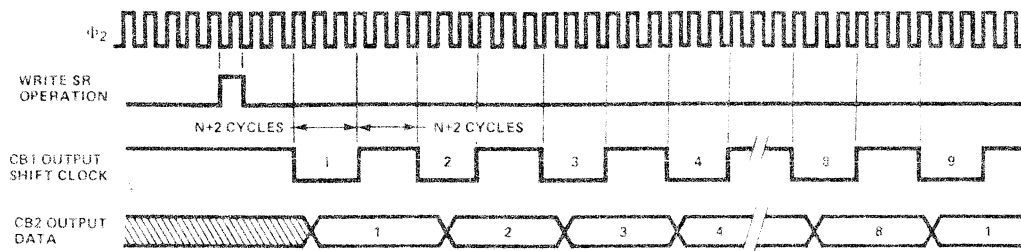


Figure 23. Shift Register Input Modes

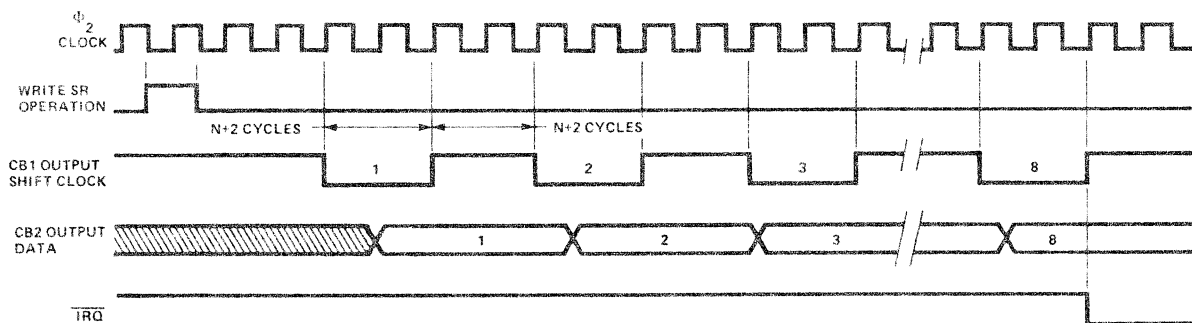
Shift Out Free-Running at T2 Rate (100)

Mode 100 is very similar to mode 101 in which the shifting rate is set by T2. However, in mode 100 the SR Counter does not stop the shifting operation. Since the Shift Register bit 7 (SR7) is recirculated back into bit 0, the 8 bits loaded into the shift register will be clocked onto CB2 repetitively. In this mode the shift register counter is disabled.



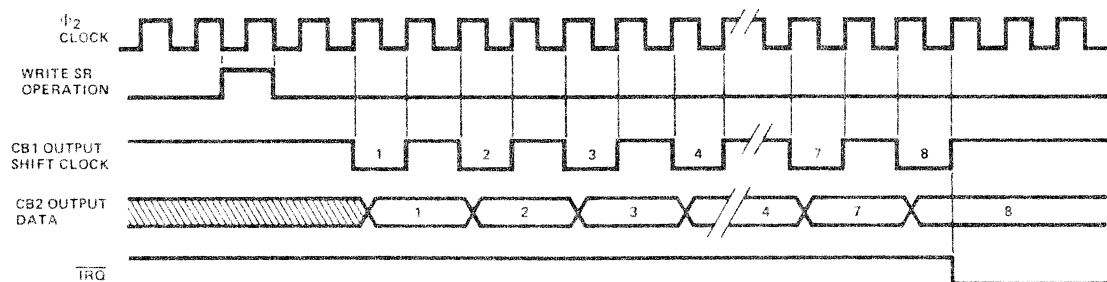
Shift Out Under Control of T2 (101)

In mode 101 the shift rate is controlled by T2 (as in the previous mode). However, with each read or write of the shift register the SR Counter is reset and 8 bits are shifted onto CB2. At the same time, 8 shift pulses are generated on CB1 to control shifting in external devices. After the 8 shift pulses, the shifting is disabled, the SR Interrupt Flag is set and CB2 remains at the last data level.



Shift Out Under Control of ϕ_2 (110)

In mode 110, the shift rate is controlled by the ϕ_2 system clock.



Shift Out Under Control of External CB1 Clock (111)

In mode 111 shifting is controlled by pulses applied to the CB1 pin by an external device. The SR counter sets the SR Interrupt flag each time it counts 8 pulses but it does not disable the shifting function. Each time the microprocessor writes or reads the shift register, the SR Interrupt flag is reset and the SR counter is initialized to begin counting the next 8 shift pulses on pin CB1. After 8 shift pulses, the interrupt flag is set. The microprocessor can then load the shift register with the next byte of data.

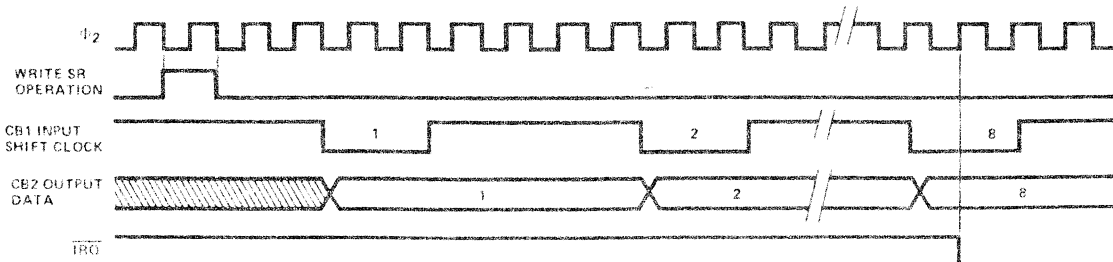


Figure 24. Shift Register Output Modes

SY6522-SHIFT REGISTER MODE PROBLEM

There are 7 shift register modes in the SY6522. One of the modes, mode 010, permits shifting data into the SY6522 under control of the $\phi 2$ system clock. It has been found that this mode does not function properly and this note is intended to describe the nature of the problem.

SYMPTOM

When the mode control (Auxiliary Control Register) is set up, the SY6522 device is ready to shift in data. The shift operation is initiated when the processor writes or reads the Shift Register in the SY6522. At this point, the SY6522 would normally generate a series of 8 clock pulses on the CB1 pin which would be used to clock an external shift register, whose output would tie directly into the CB2 pin of the SY6522. Figure 1 shows a typical arrangement.

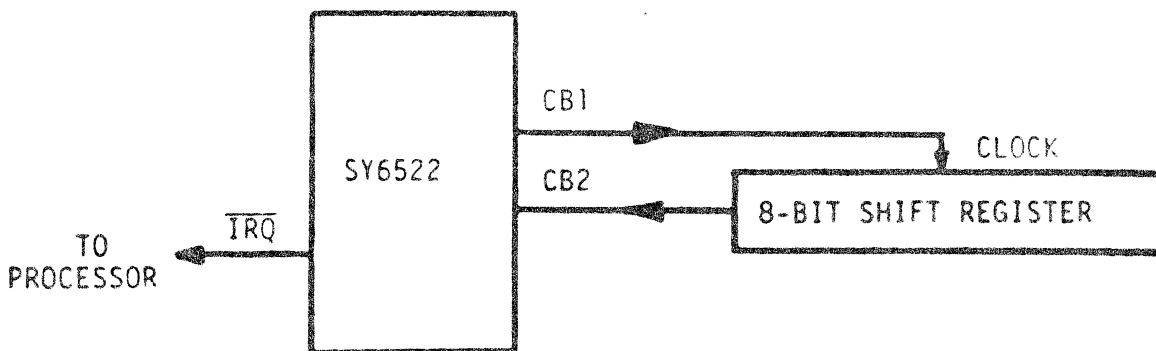


Figure 1 - Simplified Schematic

However, in this mode only, the SY6522 generates 9 clock pulses, instead of 8. As far as the external shift register is concerned, the 9th clock pulse is extraneous. However, the processor interrupt (signifying shift register full) does not occur until the 9th clock pulse has occurred. The actual waveforms are shown in Figure 2.

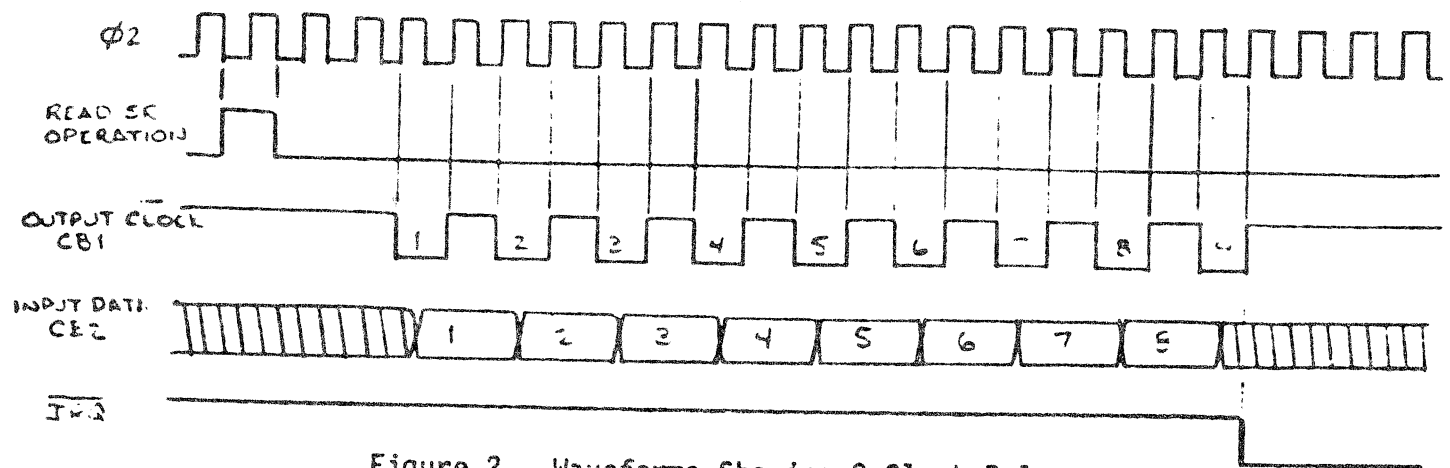


Figure 2 - Waveforms Showing 9 Clock Pulses

SOLUTIONS

There are three alternatives:

1. Shift in under control of T2 (mode 001). In this mode, The T2 timer on the SY6522 is used to generate the clocks.
2. Build some off-chip circuitry to block the 9th clock pulse from affecting the external shift register.

Figure 3 shows a sample circuit. Note that the circuit of Figure 3 must be disabled if it is desired to shift out, as well as to shift in. In this case, the circuit must only be enabled for shift in operation.

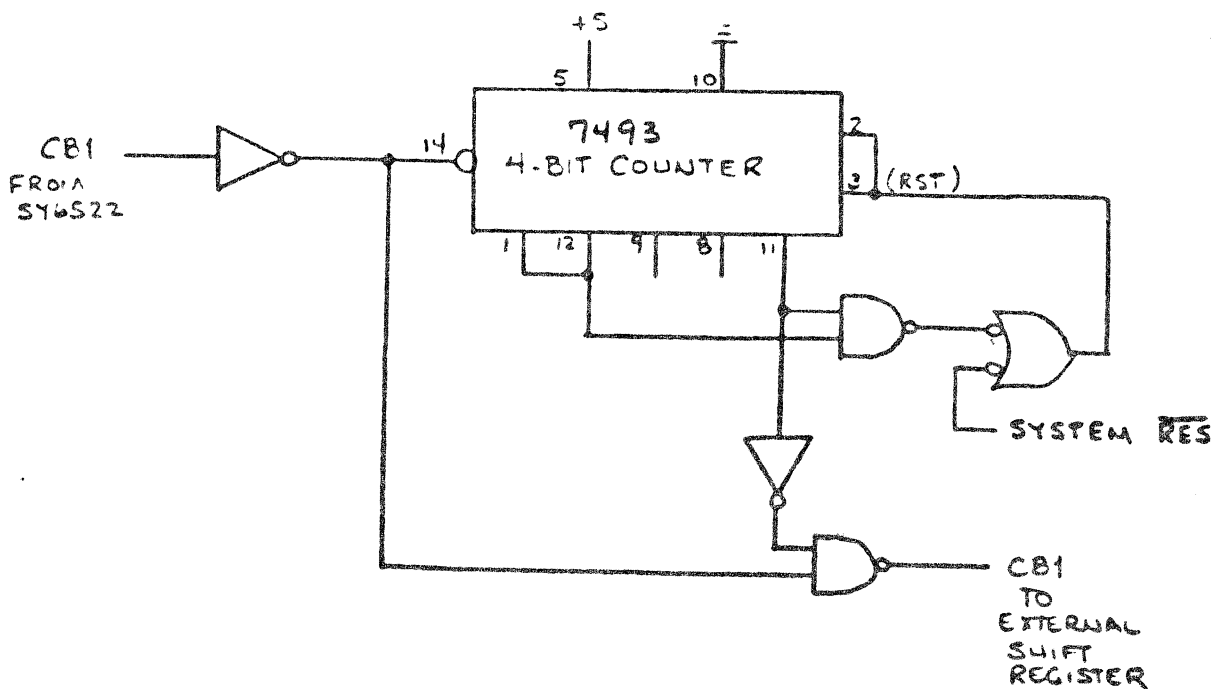
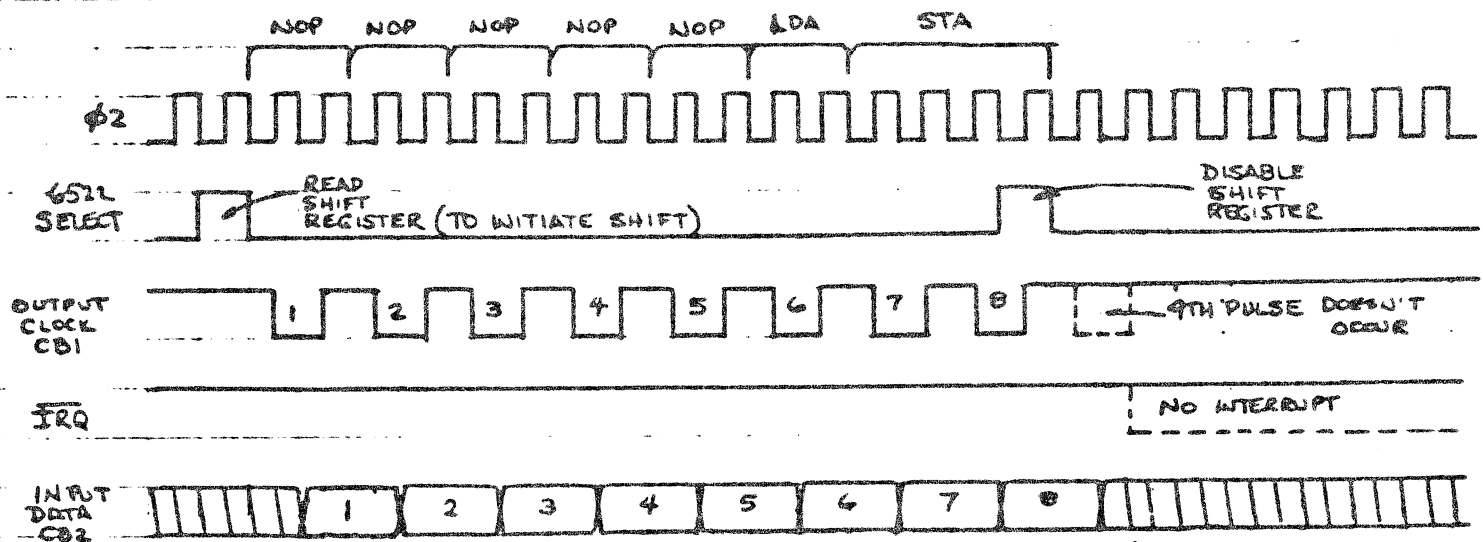


Figure 3 - Circuit to Block 9th Clock Pulse

3. Disable the shift register before the 9th clock pulse is generated. In this case, only 8 pulses will be generated and no interrupt will occur. This requires precise timing in the program. Figure 4 illustrates the program waveforms with a sample listing.



0024	AD 0A AB	LDA SR1	;START SHIFT
0027	EA	NOP	;DELAY 10 CLK CYCLES
0028	EA	NOP	
0029	EA	NOP	
002A	EA	NOP	
002B	EA	NOP	
002C	A9 00	LDA #00	;DISABLE SHIFT REG
002E	BD 0E AB	STA ACK1	
0031	AD 0A AB	LDA SR1	

FIGURE 4

Waveforms and Listing to Abort Shift After 8 Clocks

-SY6522 - TIMING PRECAUTIONS FOR EXTERNALLY CLOCKING SHIFT REGISTER

The SY6522 Versatile Interface Adapter has an internal 8-bit shift register which permits serial data communication with other units. One of the shift register modes permits shifting data into the SY6522 clocked by an external clock source. Figure 1 shows the timing waveforms.

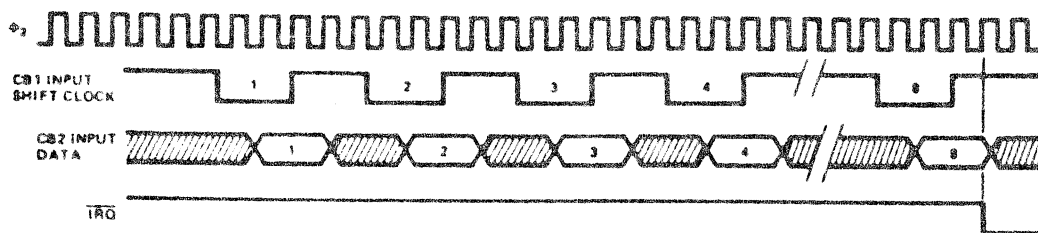


Figure 1 - Timing Waveforms to Shift In with External Clock

A potential problem exists with this scheme if the external clock is applied asynchronously to the $\phi 2$ clock of the SY6522. Specifically, care must be taken to ensure that the positive-going edge of the CB1 clock does not occur during the last 100 nsec of the $\phi 2$ time. Figure 2 illustrates this.

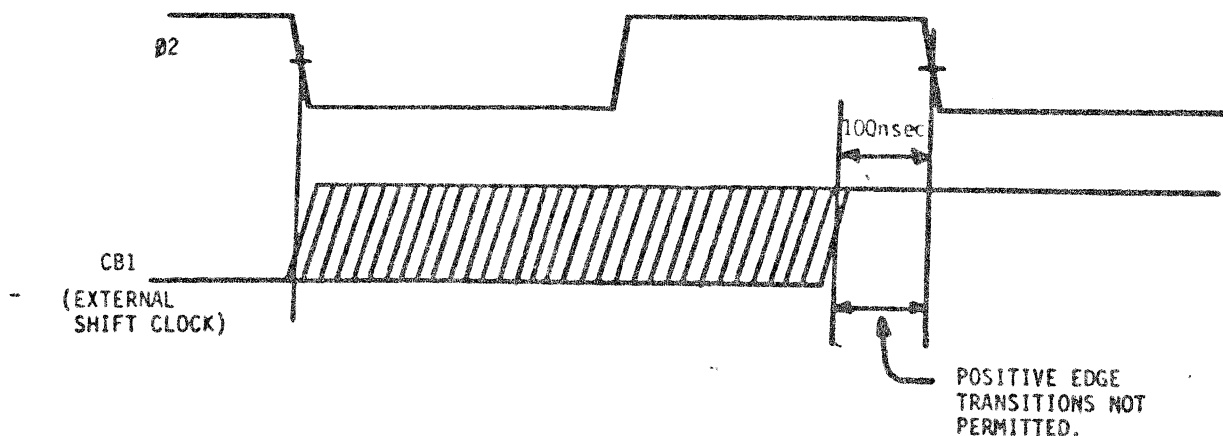


Figure 2 - CB1 Timing Restrictions

A clean solution is to clock the external clock with Ø2, as shown in Figure 3. In this way, both positive and negative transitions occur coincident with the Ø2 positive-going edge and proper operation is ensured.

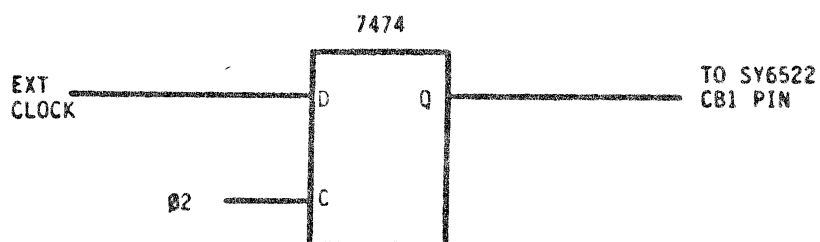
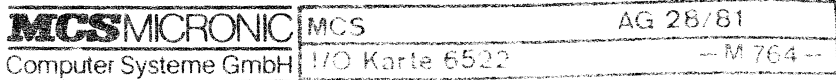


Figure 3 - Clocking Circuit for CB1 Input

CJB:jh
4/4/80



Belegung : Pfostenverbinder I/O Karte M764

VL-1

DSUB1/1	o	1	o	PA0	(6522/1)
2	o	2	o	PA1	
3	o	3	o	PA2	
4	o	4	o	PA3	
5	o	5	o	PA4	
6	o	6	o	PA5	
7	o	7	o	PA6	
8	o	8	o	PA7	
18	o	9	o	PB7	
11	o	10	o	PB0	
17	o	11	o	PB6	
12	o	12	o	PB1	
16	o	13	o	PB5	
13	o	14	o	PB2	
15	o	15	o	PB4	
14	o	16	o	PB3	
21	o	17	o	CA1	
22	o	18	o	CA2	
23	o	19	o	CB1	
24	o	20	o	CB2	
Ø2	o	21	o	S2	

VL-2

PA0	o	1	o	1/DSUB2
PA1	o	2	o	2
PA2	o	3	o	3
PA3	o	4	o	4
PA4	o	5	o	5
PA5	o	6	o	6
PA6	o	7	o	7
PA7	o	8	o	8
PB7	o	9	o	18
PB0	o	10	o	11
PB6	o	11	o	17
PB1	o	12	o	12
PB5	o	13	o	16
PB2	o	14	o	13
PB4	o	15	o	15
PB3	o	16	o	14
CA1	o	17	o	21
CA2	o	18	o	22
CB1	o	19	o	23
CB2	o	20	o	24
GND	o	21	o	Vcc

Beetückungsseite

Belegung Sockel SB

(Beschreibung gilt für eingelegte Brücke)

1/14	RES auf Pin 25 DSub	
2/13	NMI auf Pin 9 DSub	} alternativ
3/12	-12V auf Pin 9 DSub	
4/11	-12V auf Pin19 DSub	} alternativ
5/10	+12V auf Pin19 DSub	
6/9	+5V auf Pin 20 DSub	
7/8	GND auf Pin 10 DSub	

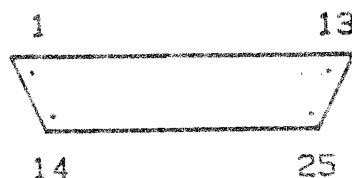
I/O Karte M 764

DSub - Stecker/Buchse 25polig

Spez. Bez. I/O Karte 6522 M764 Stecker 1

PIN	BELEGUNG	BEM.
1	VL-1 Pin 1o	PA0 (6522/1)
2	2o	1
3	3o	2
4	4o	3
5	5o	4
6	6o	5
7	7o	6
8	8o	7
9	-12V oder NMI	
10	GND	
11	VL-1 Pin 10o	PB0 (6522/1)
12	12o	1
13	14o	2
14	16o	3
15	15o	4
16	13o	5
17	11o	6
18	9o	7
19	+12V oder -12V	
20	+5V (Vcc)	
21	CA1	
22	CA2	
23	CB1	
24	CB2	
25	Reset	

Stecker - Sicht auf die Steckseite

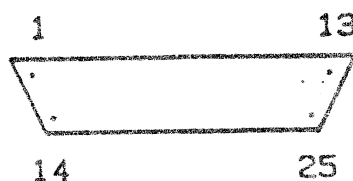


DSub - Stecker/Buchse 25polig

Spez. Bez. I/O Karte 6522 M764 Stecker 2

PIN	BELEGUNG	BEM.
1	VL-2 Pin1o	PA0 (6522/2)
2	2o	1
3	3o	2
4	4o	3
5	5o	4
6	6o	5
7	7o	6
8	8o	7
9	-12V oder NMI	
10	GND	
11	VL-2 Pin10o	PB0 (6522/2)
12	12o	1
13	14o	2
14	16o	3
15	15o	4
16	13o	5
17	11o	6
18	9o	7
19	+12V oder -12V	
20	+5V (Vcc)	
21	CA1	
22	CA2	
23	CB1	
24	CB2	
25	Reset	

Stecker - Sicht auf die Steekeseite



Anschlusszuordnung I/O-Karte 652

PIN	a	c
1		
2	S2	S2
3		
4	+12V	+12V
5	-12V	-12V
6	+5V (V _{cc})	+5V (V _{cc})
7	GND	GND
8	GND	GND
9	PR0	PR1
10	PR2	PR3
11	PR4	PR5
12	PR6	PR7 (R3)
13		
14	I/O-SEL	
15	R/W	
16	⌀2	
17	IRQ-REQ	
18	NMI	RESET
19		
20	DB7	DB6
21	DB5	DB4
22	DB3	DB2
23	DB1	DB0
24	←	→
25		
26		
27		
28	AB 9	AB 8
29	AB 7	AB 6
30	AB 5	
31		
32	AB 1	AB0