RM 65 FAMILY

Single Board Computer (SBC) Module

USER'S MANUAL

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Rockwell International

Document No. 29801 N09
Order No. 809
Rev. 1 October 1982

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SECTION 1

INTRODUCTION

1.1 PURPOSE/FUNCTION

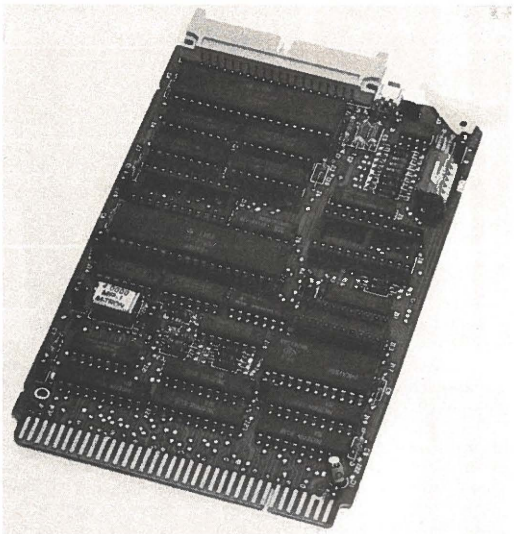
The RM 65 Single Board Computer module (SBC) is designed for user flexibility. There are provisions for all the necessary elements of single board operation - program memory, read/write memory, input, and output. Additionally there is expansion capability for multi-module applications - flexible memory mapping, bank addressing, and DMA compatability. Being similar both in hardware and software to the AIM 65, the SBC is well supported for system design and development using the AIM 65.

The SBC module allows users to design their products into compact, modular stacks. The SBC module plugs into a single slot in an RM 65 card cage/motherboard and controls other memory and I/O modules. The heart of the SBC module is an R6502 CPU, which is capable of addressing 65K bytes of memory. In addition, the SBC module contains bank address logic which allows addressing of one or two 65K byte memory banks. Sockets on the module accept up to 16K bytes of PROM/ROM. 2K bytes of static RAM are also provided. An R6522 Versatile Interface Adapter (VIA) provides two 8-bit parallel I/O data lines, two 2 bit control lines, two counter-timers and an 8-bit shift register. A base address selection header assigns memory sections to 4K byte blocks. All address, data and control lines are buffered.

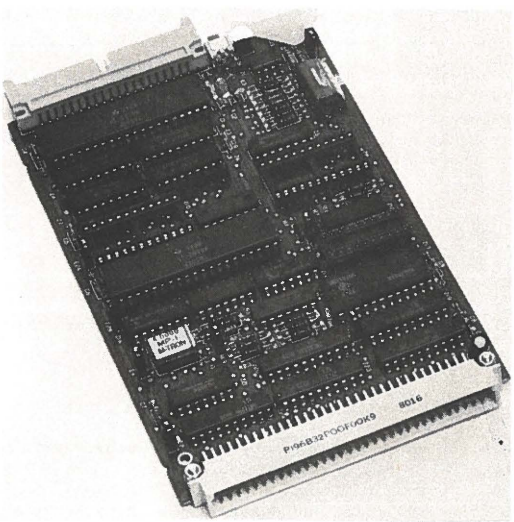
The SBC module is available in a 72-pin Edge Connector version (RM65-1000) and in a 64-pin Eurocard version (RM65-1000E). Both versions are shown in Figure 1-1. The pin assignments for the two versions are identical except the edge connector has four additional pins connected to +5 Vdc and four unused pins (see Table 3-1 for the pin assignments).

1.2 FEATURES

- o Rockwell RM 65 Bus compatible
- o Compact size - about 4" x 6-1/2" (100 mm x 160 mm)
- o Fully buffered address, data, and control lines for RM 65 Bus
- o R6502 CPU
- o 2K bytes of R2114 static RAM
- o Two sockets for up to 16K bytes of the following PROM/ROM or equivalents
  - TI TMS 2516, TMS 2532, and Motorola MCM 68764 PROMs
  - Rockwell R2316, R2332, or R2364 ROMs



a. Edge Connector Version



b. Eurocard Version

Figure 1-1. SBC Module

- o R6522 Versatile Interface Adapter (VIA) I/O Interface provides
  - Two 8-bit parallel bidirectional data ports
  - Four control lines
  - Two programmable 16-bit counter/timers
  - Shift register for serial communications
- o Separate switches allow RAM, PROM/ROM, and VIA to be individually dedicated to one or both 65K memory banks
- o Flexible selection of the following
  - 2K, 4K or 8K PROM/ROMs
  - RAM, PROM/ROM and I/O base address to any 4K byte boundary
  - On-board or external bank addressing source
  - Programmable DMA Terminate
  - On-board or external clock source
- o +5V operation
- o Fully assembled, tested and warranted

1.3 CHARACTERISTICS

The SBC module physical and electrical characteristics are defined in Table 1-1.

1.4 REFERENCE DOCUMENTS

Rockwell

Document No.	
29650N30	R6500 Programming Manual
29650N31	R6500 Hardware Manual
29650N36	AIM 65 Microcomputer User's Guide
29000D47	R6522 Versatile Interface Adapter (VIA)

Table 1-1. SBC Module Physical and Electrical Characteristics

Characteristics	Value
Physical Characteristics (See Figure 1-2)	
Edge Connector Version	
Width	3.9 in. (100 mm)
Length	6.5 in. (164 mm)
Height	0.56 in. (14 mm)
Weight	5.3 oz. (150 g)
Eurocard Version	
Width	3.9 in. (100 mm)
Length	6.3 in. (160 mm)
Height	0.56 in. (14 mm)
Weight	5.6 oz. (160 g)
Environment	
Operating Temperature	0° to 70°C
Storage Temperature	-40°C to 85°C
Relative Humidity	0% to 85% (without condensation)
Power Requirements	+5 Vdc $\pm$ 5% 0.75A (3.5W) - Typical
	+5 Vdc $\pm$ 5% 1.2A (6.0W) - Maximum
Interface Connectors	
RM 65 Bus Connection	
Edge Connector Version	72-pin edge connector (0.100 in. centers)
Eurocard Version	64-pin plug (0.10 in. centers) per DIN 41612 (Row b not installed)
I/O Connector	40-pin mass termination connector (0.100 in. centers) Mates to T&B/Ansley 609-4000M or equiv.
Remote RESET Connector	2 vertical pins (0.3 in. high) on 0.200 in. centers

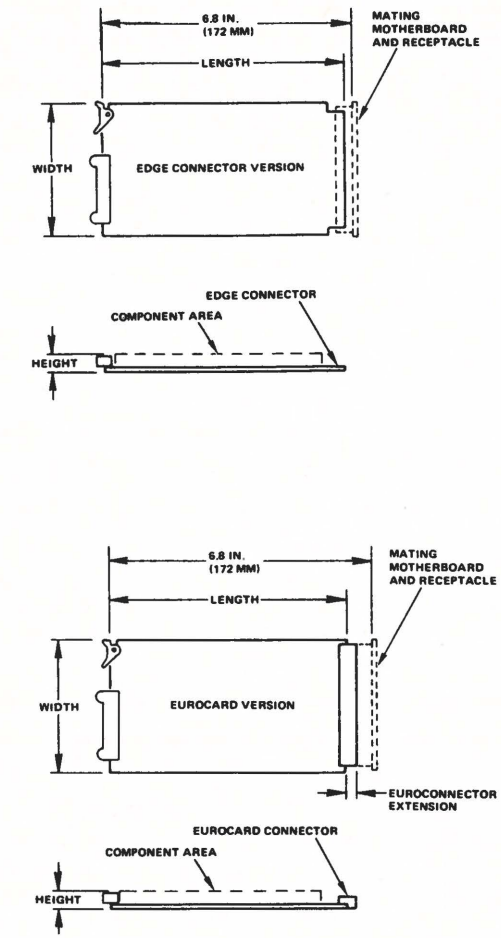


Figure 1-2. SBC Module Outline

SECTION 2

INSTALLATION AND OPERATION

2.1 UNPACKING

Unpack the SBC module from its shipping carton and, referring to the packing list, verify that all of the parts are included. Save the packing material for storing the module.

> **CAUTION**
>
> This module contains voltage sensitive items. The module should be stored in an anti-static container when not in use and anyone handling unit should observe anti-static precautions. Damage to the unit may result if anti-static protection is not maintained.

2.2 OPERATING OPTIONS

The switch, header or jumper selectable operating options are:

- o Base Address selection
- o Bank Address selection
- o PROM/ROM Size selection
- o Remote Reset
- o Clock Source selection
- o Bank Address Source
- o DMA Terminate Source

Figure 2-1 identifies the detail on the SBC module. The function of each switch, jumper and connector is identified in Table 2-1 along with reference to the section and/or table that describes its use.

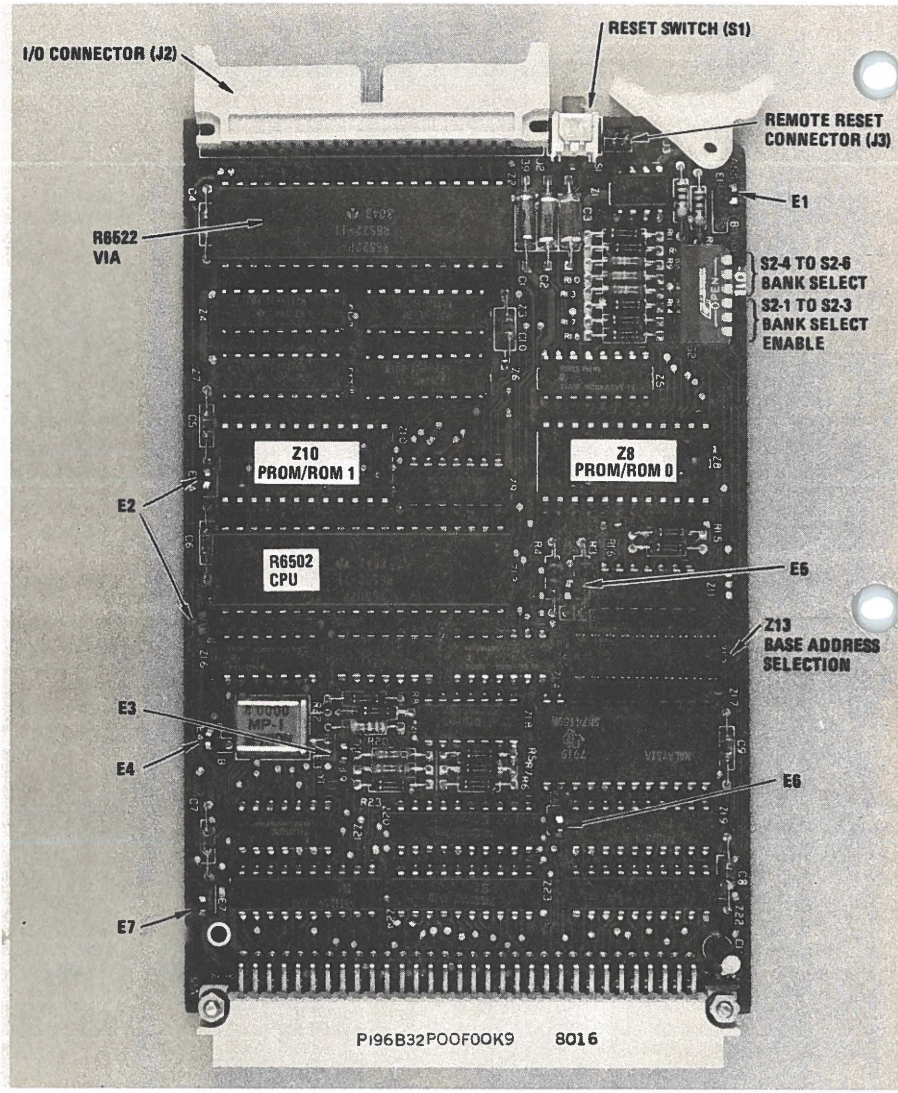


Figure 2-1. SBC Module Detail

Table 2-1. SBC Module Switches, Header, Jumpers and Connectors

Category	Item	Description	Reference
Switches	S1	RESET switch	Section 2.2.4
	S2 -1 -2 -3	Bank Select Enable switch for: I/O section RAM section PROM/ROM section	Section 2.2.2 Table 2-3
	S2 -4 -5 -6	Bank Select switch for: I/O section RAM section PROM/ROM sections	Section 2.2.2 Table 2-3
Header	Z13	Base Address Selection header	Section 2.2.1 Table 2-2 Figure 2-2
Jumpers	E1	Bank Address Control jumper	Section 2.2.6 Table 2-6
	E2	Size Selection (4K/8K) for PROM/ROM section 0 (Z8)	Section 2.2.3 Table 2-4
	E3	Size Selection (4K/8K) for PROM/ROM Section 1 (Z10)	
	E4	Size Selection (2K/4K) for PROM/ROM section 1 (Z10)	
	E5	External Clock Source selection	Section 2.2.5 Table 2-5
	E6	Bank Address Source jumper	Section 2.2.6 Table 2-6
	E7	DMA Terminate jumper	Section 2.2.7 Table 2-7
Connectors	P1	RM 65 bus connector	Tables 3-1 and 3-4
	J2	Parallel I/O connector	Tables 3-2 and 3-5
	J3	Remote RESET connector	Section 2.2.4 Table 3-3

2.2.1 Base Address Selection

The SBC module is segmented into four independent sections:

- 2K byte RAM section
- 1K byte I/O section
- Two 2K, 4K or 8K byte PROM/ROM sections

A base address that uniquely defines a 4K or 8K byte block must be assigned to each section (or any section may be disabled if not required). No two sections may be assigned a common base address (unless each are dedicated to a different memory bank - see Section 2.2.2). A section is assigned to a base address by installing a jumper between its Section pin and the desired Base Address pin of the Base Address header (Z13 - see Figure 2-1 and Table 2-2). A section is disabled by leaving the Section pin dissconnected.

The RAM section will always be assigned to the lower 2K bytes of the selected 4K block.

The I/O will always be assigned to the lower 1K bytes of the selected 4K block (the first 16 bytes are unique VIA registers, while the remaining locations are redundant).

PROM/ROM Section 1 can be assigned to a 4K or 8K byte block; A 2K PROM/ROM will reside in either the lower 2K bytes of the selected 4K block or in the entire 4K block with 2K images in both the upper and lower half, depending on the position of the 2K/4K Size Selection jumper. PROM/ROM Section 0 can be assigned to a 4K, or an 8K byte block; a 2K PROM/ROM will always reside in the lower 2K bytes of the selected 4K block. An 8k device in either section requires two Base Address jumpers, with one for each 4K segment.

2.2.2 Bank Selection

The SBC module supports RM 65 bank addressing for all on-board memory and I/O. The bank Select Enable switches (S2-1 to S2-3), in conjunction with the Bank Select switches (S2-4 to S2-6), allow the RAM, PROM/ROM, and I/O to be independently assigned common to both 65K memory banks (Bank 0 and Bank 1) or dedicated to a selected memory bank (Bank 0 or Bank 1). The RAM, I/O, and PROM/ROM (both sections together) are each provided with Bank Selection capability.

When OPEN, the Bank Select Enable switch assigns its section (I/O, RAM or PROM/ROM) common to both banks, regardless of the section's Bank Select switch. When the Bank Select Enable switch is CLOSED, the assigned bank is determined by the Bank Select switch. See Table 2-3 for switch assignments and positions.

The two bank structure of the SBC allows two sections to be assigned the same base address, with each in a different dedicated bank.

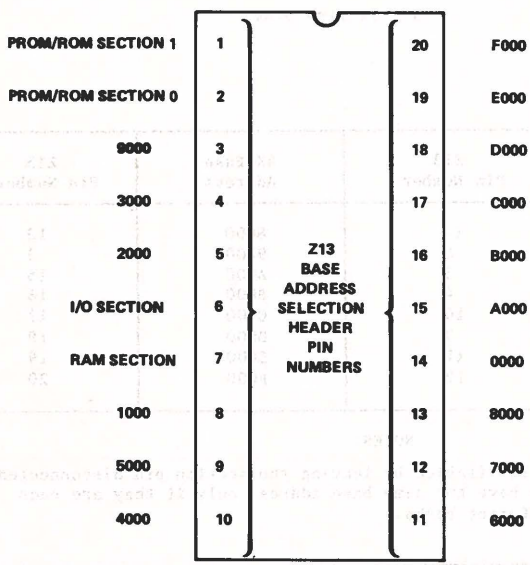


Figure 2-2. Base Address Selection Header

Table 2-2. Base Address Selection Header

Section	Z13 Pin Number
RAM	7
PROM/ROM Section 0(Z8)	2
PROM/ROM Section 1 (Z10)	1
I/O	6

a. Section pins

4K Base Address	Z13 Pin Number	4K Base Address	Z13 Pin Number
0000	14	8000	13
1000	8	9000	3
2000	5	A000	15
3000	4	B000	16
4000	10	C000	17
5000	9	D000	18
6000	11	E000	19
7000	12	F000	20

NOTES:

1. Any section may be disabled by leaving the section pin disconnected.
2. Two sections may have the same base address only if they are each dedicated to different banks.

b. Base Address pins

Table 2-3. Bank Selection Switch Positions

Memory Bank Selected:	Switch Position	
	Bank Select Enable Switch	Bank Select Switch
For RAM section	S2-2	S2-5
Bank 0 and 1 (common)	OPEN	EITHER
Bank 0 (lower 65K)	CLOSED	OPEN
Bank 1 (upper 65K)	CLOSED	CLOSED
For I/O section	S2-1	S2-4
Bank 0 and 1	OPEN	EITHER
Bank 0	CLOSED	OPEN
Bank 1	CLOSED	CLOSED
For both PROM/ROM sections	S2-3	S2-6
Bank 0 and 1	OPEN	EITHER
Bank 0	CLOSED	OPEN
Bank 1	CLOSED	CLOSED

2.2.3 PROM/ROM Size Selection

The following 2K, 4K, and 8K PROM/ROM devices (or equivalent) can be installed in PROM/ROM section 0 or section 1 (Z8, Z10):

Rockwell R2316 (2K x 8 ROM)
Intel 2716 (2K x 8 EPROM)

Rockwell R2332 (4K x 8 ROM)
Texas Instruments 2532 (4K x 8 EPROM)

Rockwell R2364A (8K X 8 ROM)
Motorola MCM68764 (8K x 8 EPROM)

The 4K/8K size selection for PROM/ROM section 0 (Z8) uses jumper E2. The 4K/8K size selection for PROM/ROM section 1 (Z10) uses jumper E3, while the 2K/4K selection uses jumper E4. The jumper positions are shown in Table 2-4.

Table 2-4. PROM/ROM Size Selection Jumper Positions

Section (Socket)	PROM/ROM	Edge Connector Version		Euroconnector Version	
		Jumper	Position	Jumper	Position
Section 0 (Z8)	2K (see note 1)	E2A	Off	E2A	On
		E2B	On	E2B	Off
	4K	E2A	Off	E2A	On
		E2B	On	E2B	Off
	8K	E2A	On	E2A	Off
		E2B	Off	E2B	On
Section 1 (Z10)	2K (see Note 2)	E3	B	E3	B
		E4	A or B	E4	A or B
	4K	E3	B	E3	B
		E4	A	E4	A
	8K	E3	A	E3	A
		E4	A	E4	A

1. Enabled in lower 2K-byte address space ($X000-$X7FF) only (pin 18 = A11 = 0)

2. Enabled in either half of the 4K-byte address space depending upon the position of jumper E4:

   E4 = A: Enabled in lower half of the 4K-byte address space ($X000-$X7FF) only (pin 18 = A11 = 0).
   E4 = B: Enabled in upper half of the 4K-byte address space ($X800-$XFFF) only (pin 18 = +5V = 1).

2.2.4 Remote RESET Option

The SBC module provides an on-board RESET switch. When depressed, a hardware reset is generated for the R6502 (CPU), R6522 (VIA), and driven onto the RM 65 bus. A remote reset connector (J3) is provided to allow an additional switch to be mounted separate from the module. This connector parallels the on-board RESET switch, so activating either, or both, will generate a RESET.

2.2.5 Clock Source Selection

The SBC module uses an on-board crystal controlled oscillator which provides a 1 MHz clock reference for the module and the RM 65 bus system clocks (BØ1, BØ2, BØ2/). An external clock from the RM 65 Bus (BØ0) can be selected as the clock reference by the Clock Source Selection jumper (E5). The positions for the Clock Source Selection jumper are shown in Table 2-5.

Table 2-5. Clock Source Selection Jumper Positions

Clock Source	Jumper Position
Internal Clock Reference BØ1 = 1 MHz	E5 = A
External Clock Source (BØ0) BØ1 $\leq$ 1 MHz	E5 = B

2.2.6 Bank Address Source and Control

The SBC module provides control of the source of the Bank Address signal (BADR/) on the RM 65 bus. The Bank Address Source jumper (E6) allows the bank address signal source to be changed, either generated by the SBC module to drive the RM 65 bus, or received from the bus. When the SBC module is the source of the bank address signal, the Bank Address Control jumper (E1) selects between always Bank 0, or bank switching using the VIA device (peripheral port A, bit 0). Table 2-6 summarizes the jumper positions.

> **NOTE**
>
> If the VIA device is chosen to control the bank address line, the I/O must be bank selected common to both banks.

Table 2-6. Bank Address Source and Control Jumper Positions

Bank Address Source	BADR/ Direction	Jumper Positions
Fixed to Bank 0 (from SBC module)	Output	E1 = B E6 INSTALLED
Controlled by VIA (from SBC module)	Output	E1 = A E6 INSTALLED
External Control (from RM 65 Bus)	Input	E1 = EITHER E6 REMOVED

2.2.7 DMA Terminate Control

The SBC module will always source the DMA Terminate (BDMT/) signal onto the RM 65 bus. The DMA Terminate Control Jumper (E7) allows this signal to be always inactive (forced to a logic 1) or to be controlled by the VIA device (peripheral port A, bit 1). Table 2-7 shows the possible jumper positions.

Table 2-7. DMA Terminate Control Jumper Positions

DMA Terminate Control (BDMT/)	Jumper Position
Fixed to inactive level (logic 1)	E7 REMOVED
Controlled by VIA	E7 INSTALLED

2.3 INSTALLING THE MODULE

Before installing the module, ensure that it is not damaged and is free of grease, dirt, or other foreign matter. Installation is accomplished as follows:

> **CAUTION**
>
> Prior to module installation, turn off power to the RM 65 Bus and to any interfacing external equipment.

a. Based on the system memory map and requirements (refer to Section 4), select the proper module operating options by performing the following steps:

   (1) Install the required PROM or ROM devices into sockets Z8 and Z10, and position jumpers E2, E3 and E4 as required (refer to Section 2.2.3, 2.2.4, and Table 2-4, 2-5).

   (2) Select the module base addresses with header Z13 (refer to Section 2.2.1, Table 2-2, and Figure 2-1).

   (3) Select common or dedicated memory bank operation for RAM, PROM/ROM, and I/O sections by positioning switches S2-1 to S2-6 (refer to Section 2.2.2 and Table 2-3).

   (4) Select the system clock source by positioning jumper E5 (refer to Section 2.2.5 and Table 2-6).

   (5) Select the proper bank addressing source by positioning jumpers E1 and E6 (refer to Section 2.2.6 and Table 2-6).

   (6) Select the proper DMA terminate source by positioning jumper E7 (refer to Section 2.2.7 and Table 2-7).

b. Align pin Wa (Edge Connector version) or pin 1a (Eurocard version) of the module with the corresponding pin on the mating RM 65 bus receptacle.

> **CAUTION**
>
> RM 65 connectors are keyed to prevent improper module connection. If the module does not insert into the receptacle with moderate pressure applied, check the orientation and connector alignment of the module. Forcing module improperly into the receptacle will damage the receptacle and/or the module.

c. Insert the module into the desired card slot and position it above the mating receptacle.

d. Press in firmly on the end of module until all pins are securely seated.

e. Connect the required cables to J2 (Parallel I/O) and J3 (Remote RESET) I/O connectors on the SBC module (see Figure 2-1).

> **NOTE**
>
> Interface cables that connect to the SBC module are supplied by the user.

f. Reapply power to the RM 65 bus.

2.4 REMOVING THE MODULE

a. Turn-off power to the RM 65 bus and any interfacing external equipment.

b. Disconnect the cables from the I/O connectors.

c. Lift up on the module ejector tab to release the module from the mating receptacle. Pull the module straight back until it is free from the card slot guides.

SECTION 3

FUNCTIONAL AND INTERFACE DESCRIPTION

3.1 FUNCTIONAL DESCRIPTION

The block diagram in Figure 3-1 identifies the SBC module functions and interface signals.

The R6502 Central Processing Unit (CPU) is the heart of the SBC module and any interfacing modules connected to the RM 65 Bus. The R6502 performs all program execution by means of the address, data, control, and timing lines.

The Clock Circuit uses a 4 MHz crystal-controlled oscillator which is divided by four to provide a stable 1 MHz clock reference. The Clock Source Selection jumper chooses between the internal clock reference or an external clock (BØO) as the source for the R6502 and the derived system clocks (BØ1,BØ2,BØ2/).

The Reset Control circuit conditions the Reset signal for the SBC module and the Bus. A reset can be generated either by the on-board RESET switch (S1) or by a remote RESET switch (connected to J3). This circuitry also generates a reset automatically, upon power-up. The Reset signal ($\overline{\text{RES}}$) is transferred to the R6502 CPU and R6522 VIA devices, as well as buffered and driven onto the Bus (BRES/).

The Bank Select Control circuit detects when the SBC module's assigned memory bank is addressed, by comparing the Bank Address signal (BADR/) to the Bank Select Enable (S2-1 to S2-3) and Bank Select (S2-4 to S2-6) switches. The Bank Select Enable Switches allow all on-board PROM/ROM, RAM, and VIA to be independently assigned common to both Bank 0 (lower 65K) and Bank 1 (upper 65K), or dedicated to either Bank 0 or Bank 1 as assigned by the Bank Select switches.

The Bank Address jumpers choose the source and control for BADR/. The Bank Address source jumper (E6) determines whether BADR/ is generated by the SBC module (driven onto the Bus) or generated by another module (received from the Bus). When the SBC module is the source, the Bank Address Control jumper (E1) allows BADR/ to be always in Bank 0 (forced to a logic 1) or to be selectable to either bank, under control of the VIA device (peripheral port A, bit 0).

The Base Address Decoder uses the six most significant address bits (BA0/ - BA15/), the bank address signal, and the Base Address Selection header (Z13) to generate chip selects for the on-board PROM/ROM ($\overline{\text{ROMSEL0}}$, $\overline{\text{ROMSEL1}}$), RAM ($\overline{\text{RAMSEL0}}$, $\overline{\text{RAMSEL1}}$), and VIA. The RAM and VIA can be independently mapped into any 4K block of the selected 65K bank. The PROM/ROMs may be mapped into any 4K or 8K block of the selected bank.

The 16K PROM/ROM section has two sockets which can accept 2K, 4K or 8K PROM/ROM devices. The size and type of PROM or ROM is specified by the Base Address Selection header and the PROM/ROM Size jumpers (E2,E3,E4).

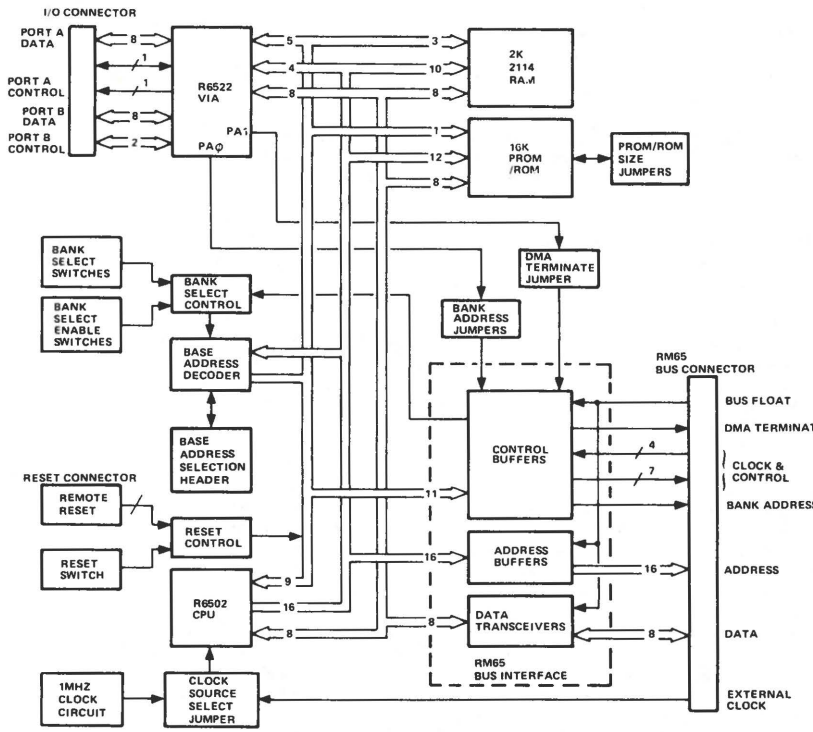


Figure 3-1. SBC Module Block Diagram

The 2K RAM section uses four 1K x 4 R2114 RAM devices to provide on-board read/write memory.

The R6522 Versatile Interface Adapter (VIA) provides input-output capability to the SBC Module. The VIA provides two 8-bit I/O ports, each with two control lines. Both ports and the control lines are brought out to a connector for user applications.

The SBC Module can control up to 15 additional support modules by means of the RM 65 Bus. There are three groups of signals on the RM 65 Bus: clock and control, data, and address.

The Data Transceivers invert and transfer eight bits of parallel data (BD0/-BD7/) between the SBC Module and the RM 65 bus. The direction of the transceivers is controlled by the read/write signal from the R6502. The transceivers are disabled (tri-stated) when the on-board PROM/ROM, RAM, or VIA is addressed or when the Bus Float signal (BFLT/) from the RM 65 Bus is active.

The Address Buffers invert and transfer 16 parallel address bits (BA0/-BA15/) from the SBC Module to the RM 65 bus. These buffers are disabled when BFLT/ is active.

The DMA Terminate jumper (E7) allows the DMA Terminate signal (BDMT/) to be always inactive (forced to a logic 1) or to be controlled by the VIA device (peripheral port A, bit 1).

The Control Buffers buffer all control and clock signals between the SBC Module and the RM 65 bus. The Non-Maskable Interrupt (BNMI/), Interrupt Request (BIRQ/), Set Overflow (BSO/), External Clock (BØ0), Ready (BRDY) and Bus Float (BFLT/) input lines are buffered coming from the RM 65 bus into the SBC Module. The DMA Terminate (BDMT/), Reset (BRES/) and Phase 1 Clock (BØ1) output lines are always driven from the SBC Module onto the RM 65 Bus. The other six output lines for Read/Write (BR/$\overline{W}$, BR/$\overline{W}$/), Phase 2 Clock (BØ2,BØ2/), Sync (BSYNC), and Bank Address (BADR/) are also buffered, but are disabled when BFLT/ is active.

3.2 INTERFACE DESCRIPTION

Table 3-1 lists pin connections for I/O signals transferred between the SBC module connector P1 and the RM 65 Bus.

Table 3-2 lists pin connections for the VIA device I/O signals transferred on connector J2.

Table 3-3 lists the pin connections for the remote RESET switch on connector J3.

Tables 3-4 and 3-5 describe all I/O signals (P1 and J2) in detail.

Table 3-1. Connector P1 (RM 65 Bus) Pin Assignments

Pin	Signal Mnemonic	Signal Name	P1 Input/Output
Wa		Not Connected (See Note)	
Wc		Not Connected (See Note)	
Xa	+5V	+5 Vdc (See Note)	
Xc	+5V	+5 Vdc (See Note)	
1a	GND	Ground	
1c	+5V	+5 Vdc	
2a	BADR/	Buffered Bank Address	I/O
2c	BA15/	Buffered Address Bit 15	O
3a	GND	Ground	
3c	BA14/	Buffered Address Bit 14	O
4a	BA13/	Buffered Address Bit 13	O
4c	BA12/	Buffered Address Bit 12	O
5a	BA11/	Buffered Address Bit 11	O
5c	GND	Ground	
6a	BA10/	Buffered Address Bit 10	O
6c	BA9/	Buffered Address Bit 9	O
7a	BA8/	Buffered Address Bit 8	O
7c	BA7/	Buffered Address Bit 7	O
8a	GND	Ground	
8c	BA6/	Buffered Address Bit 6	O
9a	BA5/	Buffered Address Bit 5	O
9c	BA4/	Buffered Address Bit 4	O
10a	BA3/	Buffered Address Bit 3	O
10c	GND	Ground	
11a	BA2/	Buffered Address Bit 2	O
11c	BA1/	Buffered Address Bit 1	O
12a	BA0/	Buffered Address Bit 0	O
12c	BØ1	Buffered Phase 1 Clock	O
13a	GND	Ground	
13c	BSYNC	Buffered Sync	O
14a	BSO	Buffered Set Overflow	I

Table 3-1. Connector P1 (RM 65 Bus) Pin Assignments (Continued)

Pin	Signal Mnemonic	Signal Name	P1 Input/Output
14c	BDRQ1/	Buffered DMA Request 1	Not Used
15a	BRDY	Buffered Ready	I
15c	GND	Ground	
16a		User Spare 1	Not Used
16c	-12V/-V	-12 Vdc/-V	Not Used
17a	+12V/+V	+12 Vdc/+V	Not Used
17c		User Spare 2	Not Used
18a	GND	Ground	
18c	BFLT/	Buffered Bus Float	I
19a	BDMT/	Buffered DMA Terminate	O
19c	BØ0	Buffered External Phase 0 Clock	I
20a		User Spare 3	Not Used
20c	GND	Ground	
21a	BR/$\overline{W}$/	Buffered Read/Write "Not"	O
21c		System Spare	Not Used
22a	BDRQ2/	Buffered DMA Request 2	Not Used
22c	BR/$\overline{W}$	Buffered Read/Write	O
23a	GND	Ground	
23c	BACT/	Buffered Bus Active	Not Used
24a	BIRQ/	Buffered Interrupt Request	I
24c	BNMI/	Buffered Non-Maskable Interrupt	I
25a	BØ2/	Buffered Phase 2 "Not" Clock	O
25c	GND	Ground	
26a	BØ2	Buffered Phase 2 Clock	O
26c	BRES/	Buffered Reset	O
27a	BD7/	Buffered Data Bit 7	I/O
27c	BD6/	Buffered Data Bit 6	I/O
28a	GND	Ground	
28c	BD5/	Buffered Data Bit 5	I/O
29a	BD4/	Buffered Data Bit 4	I/O
29c	BD3/	Buffered Data Bit 3	I/O

Table 3-1. Connector P1 (RM 65 Bus) Pin Assignments (Continued)

Pin	Signal Mnemonic	Signal Name	P1 Input/Output
30a	BD2/	Buffered Data Bit 2	I/O
30c	GND	Ground	
31a	BD1/	Buffered Data Bit 1	I/O
31c	BD0/	Buffered Data Bit 0	I/O
32a	+5V	+5 Vdc	
32c	GND	Ground	
Ya	+5V	+5 Vdc (See Note)	
Yc	+5V	+5 Vdc (See Note)	
Za		Not Connected (See Note)	
Zc		Not Connected (See Note)	

NOTE

Pins Wa, Wc, Xa, Xc, Ya, Yc, Za and Zc are not used on the Eurocard version.

Table 3-2. Connector J2 (Parallel I/O) Pin Assignments

Pin	Signal Mnemonic	Signal Name	Input/Output
1	CB2	Peripheral B, Control No. 2	I/O
3	CB1	Peripheral B, Control No. 1	I/O
5	PB7	Peripheral B Port, Bit 7	I/O
7	PB6	Peripheral B Port, Bit 6	I/O
9	PB5	Peripheral B Port, Bit 5	I/O
11	PB4	Peripheral B Port, Bit 4	I/O
13	PB3	Peripheral B Port, Bit 3	I/O
15	PB2	Peripheral B Port, Bit 2	I/O
17	PB1	Peripheral B Port, Bit 1	I/O

Table 3-2. Connector J2 (Parallel I/O) Pin Assignments (Continued)

Pin	Signal Mnemonic	Signal Name	Input/Output
19	PB0	Peripheral B Port, Bit 0	I/O
21	PA7	Peripheral A Port, Bit 7	I/O
23	PA6	Peripheral A Port, Bit 6	I/O
25	PA5	Peripheral A Port, Bit 5	I/O
27	PA4	Peripheral A Port, Bit 4	I/O
29	PA3	Peripheral A Port, Bit 3	I/O
31	PA2	Peripheral A Port, Bit 2	I/O
33	PA1	Peripheral A Port, Bit 1	I/O
35	PA0	Peripheral A Port, Bit 0	I/O
37	CA2	Peripheral A, Control No. 2	I/O
39	CA1	Peripheral A, Control No. 1	I

NOTE

All even pins 2-40 are connected to Ground.

Table 3-3. Connectors J3 (Remote RESET) Pin Assignments

Pin	Signal Name	Input/Output
1	RESET	I
2	Ground	

NOTES

1. The Remote RESET switch is in parallel with the on-board reset switch.
2. Pin 1 is the pin closest to the ejector tab.

Table 3-4. Connector P1 (RM 65 Bus) Signal Description

Mnemonic	Signal Name and Signal Description	Type of Drive
	NOTE: All signals interfaced to and from the SBC module are driven at TTL voltage levels.	
+5V	+5V dc supplied to the SBC module via the RM 65 Bus.	
GND	Ground System ground.	
BA0/ - BA15/	Buffered Address Bits 0-15 Sixteen address lines transfer an inverted 16-bit parallel address from the Address Buffers in the SBC module onto the Bus. The Address Buffers are disabled (tri-state) when BFLT/ is active.	TS
BD0/ - BD7/	Buffered Data Bits 0-7 Eight bidirectional inverted data lines 8-bit data bytes between the Data Transceivers in the SBC module and the Bus. The Data Transceivers are disabled (tri-state) when BFLT/ is active.	TS
BADR/	Buffered Bank Address If on-board bank addressing is used, this line transfers the BADR/ signal from the SBC module onto the Bus. The level of BADR/ is either programmed into the VIA device or is fixed to a high level (Bank 0). BADR/ is disabled (tri-state) when BFLT/ is active. If external bank addressing is used, this line transfers the BADR/ signal from the Bus into the SBC module. A high BADR/ signal addresses the lower 65K (Bank 0) memory bank; a low BADR/ signal addresses the upper 65K (Bank 1) memory bank.	TS

Table 3-4. Connector P1 (RM 65 Bus) Signal Description (Continued)

Mnemonic	Signal Name and Signal Description	Type of Drive
BØ1	Buffered Phase 1 Clock The BØ1 signal is the system clock generated by the SBC module for the Bus.	TP
BSYNC	Buffered Sync The BSYNC signal from a tri-state buffer on the SBC module onto the Bus. The BSYNC signal goes high during the positive portion of a Ø1 clock signal when the CPU is performing an op code fetch and stays high for the remainder of that cycle. The BSYNC signal is disabled (tri-state) when BFLT/ is active.	TS
BSO	Buffered Set Overflow The BSO signal is received from the Bus by the SBC module. A negative transition on this line sets the overflow flag in the R6502 CPU.	OC
BRDY	Buffered Ready This line transfers the BRDY signal from the Bus to the input of a totem-pole buffer on the SBC module. When the R6502 CPU receives a low BRDY, the CPU will stop execution in the next read cycle. Execution will resume when BRDY is brought high.	OC
BFLT/	Buffered Bus Float The BFLT/ signal is received from the Bus by the SBC module. This line is brought low (active) to disable SBC control of the bus for DMA transfers on the Bus.	TP

Table 3-4. Connector P1 (RM 65 Bus) Signal Description (Continued)

Mnemonic	Signal Name and Signal Description	Type of Drive
BDMT/	Buffered DMA Terminate	
	The BDMT/ signal is driven from the SBC module onto the Bus. For DMA terminate control, the level of BDMT is programmed into the VIA device. A low (active) BDMT/ signal terminates the DMA operation. When control is not required, the BDMT/ is forced high (inactive).	TP
BØO	Buffered External Phase Ø Clock	
	The Phase 0 clock is generated external to the SBC module. This line transfers the BØO clock signal from the Bus into the SBC module. If used, signal BØO is the system clock for the CPU.	TP
BR/$\overline{W}$	Buffered Read/Write	
	The BR/$\overline{W}$ signal is generated by the SBC module to control the direction of data transfer on the Bus. A high BR/$\overline{W}$ (read operation) enables the SBC module to receive data from the bus. A low BR/$\overline{W}$ (write operation) enables the SBC module to transmit data onto the bus. BR/$\overline{W}$ is disabled (tri-state) when BFLT/ is active.	TS
BR/$\overline{W}$/	Buffered Read/Write "Not"	
	The BR/$\overline{W}$/ signal is generated by the SBC module to control the direction of data transfer on the Bus (the logical inverse of BR/$\overline{W}$). A low BR/$\overline{W}$/ indicates a read operation. A high BR/$\overline{W}$/ indicates a write operation. BR/$\overline{W}$/ is disabled (tri-state) when BFLT/ is active.	TS

Table 3-4. Connector P1 (RM 65 Bus) Signal Description (Continued)

Mnemonic	Signal Name and Signal Description	Type of Drive
BØ2	Buffered Phase 2 Clock The BØ2 signal is generated by the SBC module to synchronize data transfers on the bus. The address and read/write lines are set-up in the negative portion of BØ2. The data lines are set-up in the positive portion of BØ2. BØ2 is disabled (tri-state) when BFLT/ is active.	TS
BØ2/	Buffered Phase 2 Clock "NOT" The BØ2/ signal is generated by the SBC module to synchronize data transfers on the Bus (the logical inverse of BØ2). The address and read/write lines are set-up in the positive portion of BØ2/. The data lines are set-up in the negative portion BØ2/. BØ2/ is disabled when BFLT/ is active.	TS
BIRQ/	Buffered Interrupt Request The BIRQ/ signal is received by the SBC module from the Bus. BIRQ/ is forced low by any module to request service. This interrupt corresponds to the $\overline{IRQ}$ signal of the R6502 CPU and can be masked.	OC
BNMI/	Buffered Non-Maskable Interrupt The BNMI/ signal is received by the SBC module from the Bus. BNMI/ is forced low by any module to request service. This interrupt corresponds to the $\overline{NMI}$ signal of the R6502 CPU and cannot be masked.	OC
BRES/	Buffered Reset The BRES/ signal is generated by the SBC module for the Bus. BRES/ is pulsed low for 100 milliseconds at power-on. BRES/ is held low while the RESET switch is depressed and remains	TP

Table 3-4. Connector P1 (RM 65 Bus) Signal Description (Continued)

Mnemonic	Signal Name and Signal Description	Type of Drive
BRES/	Buffered Reset (continued) and remains low for 100 milliseconds after release. BRES/ provides a hardware reset to the modules on the bus and to as the VIA on the SBC module.	

NOTE

TP = Totem Pole

TS = Tri-State

OC = Open Collector

Table 3-5. Connector J2 (Parallel I/O) Signal Descriptions

Mnemonic	Signal Name and Signal Description	Type of Drive
PA0-PA7	Peripheral A Port, I/O Bits 0-7 These eight bidirectional lines can be individually programmed to act as an input or output under control of the Port A Data Direction Register. The level of the PA0-PA7 lines can be controlled by the Port A Output Register.	Passive Pull-Up
CA1	Peripheral A Control No. 1 This unidirectional line can be used as an interrupt input or can be used in conjunction with CA2 as the input line for handshaking Port A. This line also controls the latching of data on PA0-PA7 lines.	No Internal Pull-Up
CA2	Peripheral A Control No. 2 This bidirectional line can be used as an interrupt input, an output, or can be used in conjunction with CA1 as the output line for hankshaking Port A.	Passive Pull-Up
PB0-PB7	Peripheral B Port, I/O Bits 0-7 These eight bidirectional lines can be individually programmed to act as an input or output under control of the Port B Data Direction Register. The level of the PB0-PB7 lines can be controlled by the Port B Output Register. Lines PB6 and PB7 can also be used with the internal timers.	Active Pull-Up
CB1	Peripheral B Control No. 1 This bidirectional line can be used as an interrupt input, an output, or can be used in conjunction with CB2 as the input line for handshaking Port B. This line can also control the latching of data on PB0-PB7, or be a clock line for shift register operation.	Active Pull-Up

Table 3-5. Connector J2 (Parallel I/O) Signal Descriptions (Continued)

Mnemonic	Signal Name and Signal Description	Type of Drive
CB2	Peripheral B, Control No. 2 This bidirectional line can be used as an interrupt input, an output, or can be used in conjunction with CB1 as the output line for handshaking Port B. This is also the serial data line for shift register operation.	Active Pull-Up

SECTION 4

PROGRAMMING CONSIDERATIONS

4.1 GENERAL CONSIDERATIONS

To design a system around the SBC module requires a thorough knowledge of what the final system must do. For this information, certain design factors should be considered, such as:

- Are there sufficient on-board resources?
  - Program memory (PROM/ROM)?
  - Read/Write memory (RAM)?
  - Input and Output (I/O)?
- What are the on-board I/O requirements?
  - Which lines should be inputs or outputs?
  - Which functions will be required (i.e., timers or shift register)?
  - Polling or interrupt driven modes of operation?
- Is there a need for specialized I/O (e.g., buffered outputs)?
- What human interface will be required (i.e., keyboard and display)?
- Will bank addressing be needed?
- Will there be mass storage requirements (e.g., tape recorder or floppy disc)?

When the software and hardware requirements have been described, the program must be developed. A typical design approach is to write and de-bug the software, as well as check-out any hardware, using an AIM 65 (which can replace the SBC module on an RM 65 Bus). This makes many existing design aids available (Assembler, Debug Monitor, PROM Programmer, etc.). The completed software can be programmed into a PROM and put into the SBC for the final testing.

4.2 SBC MODULE MEMORY MAP

The SBC module is factory configured with base addresses to simulate the AIM 65 (RAM = $0000, ROM 0 = $E000, ROM 1 = $F000, I/O = $A000) as shown in Table 4-1. This simplifies the transfer of programs developed on the AIM 65 to the SBC. This standard configuration provides RAM for page 0 and page 1 (stack), ROM for page 255 (interrupt vectors), and I/O at the AIM 65 USER VIA location.

Table 4-1. Standard SBC Module Memory Map

Hexidecimal Address	Function	Hexidecimal Address	Function
	2K Bytes - RAM		
$0000		$8000	available for user
$1000		$9000	
$2000		$A000	1K bytes - I/O
$3000		$B000	available for user
$4000	available for user	$C000	
$5000		$D000	
$6000		$E000	4K bytes - PROM/ROM (Z8)
$7000		$F000	4K bytes - PROM/ROM (Z10)

NOTE

Bank Select Enable switches (S2-1,2,3) should be set common (OPEN) and Bank Select switches (S2-3,4,5) can be set to either bank (EITHER).

4.2.1 On-Board RAM

The 2K bytes of read/write memory always resides in the lower half of the assigned 4K block. The upper half of the 4K block is not useable by the SBC module, but is available to other modules on the RM 65 bus. In applications where additional RAM modules are required, the on-board RAM can be reassigned to the top of available RAM or disabled to provide a contiguous read/write memory segment.

> **NOTE**
>
> Because the R6502 CPU uses page 1 ($0100) for a data stack, read/write memory is almost always required at this page. Be sure to always assign RAM to this location.

4.2.2 On-Board PROM/ROM

The two PROM/ROM sockets (Z8 and Z10) are the same with the exception that PROM/ROM section 1 (Z10) can also map a 2K PROM/ROM into both the upper and lower half of the selected 4K block (usually resides in only the lower half). This allows a 2K device to hold both program code and interrupt vectors, with the program addressed as the lower 2K bytes, and the vectors in the upper locations. Both PROM/ROM sockets must always be assigned unique base addresses or disabled. For 8K PROM/ROM applications, the base address assigned to the lower 4K of the device must be an even hex digit (2, 4, 6, 8, A, C, E).

> **NOTE**
>
> Because the R6502 CPU uses the top 6 address locations for reset and interrupt vectors, non-volatile (e.g., PROM/ROM) memory must always be there. Be sure to always assign PROM/ROM to these locations.

4.2.3 On-Board I/O

The SBC module I/O consists of a VIA device assigned to the lower 1K bytes of the selected 4K block. The upper 3K is not usable by the SBC module, but is available to the other modules on the Bus. Although an entire 1K segment is dedicated to the VIA device, only the first 16 bytes are unique, while the remaining 1008 bytes are redundant (copies of the first 16 bytes). Table 4-2 relates the base address to the internal registers.

4.2.4 Bank Addressing

The bank address signal (BADR/) allows the CPU to address either of two 64K banks, for a full 128K addressing range. If BADR/ is to be selectable, sourced by the SBC module (jumpers E1=A, E6 Installed), BADR/ is controlled by the VIA peripheral A port, bit 0 (logic 1 for Bank 0, logic 0 for Bank 1). In this mode, the I/O must be assigned common to both banks (S2-1=OPEN, S2-4=EITHER) to allow control of BADR/ within either bank.

4.3 INITIALIZATION SOFTWARE

Any time the RESET switch or remote RESET switch are depressed, and at initial power-on, a reset is generated on-board ($\overline{\text{RES}}$) and driven onto the Bus (BRES/). After receiving a reset, the CPU will fetch the RESET vector (stored at $FFFC,$FFFD) and begin executing the reset routine at this address. The VIA also receives any reset, and is initialized to a reset condition with all registers cleared (except for the Shift Register and Timers). The user reset routine must now configure the VIA for the required application by the following steps:

a. The two Data Direction Registers determine for each peripheral port line if it will be an input (default by reset) or an output.

b. The Peripheral Control Register determines the polarity of transition for input mode control lines, handshake operation, or the output level of the control lines.

c. The Auxiliary Control Register determines if either of the VIA ports are latched, and how the timers and shift registers will operate.

Once these initialization steps are completed, the I/O is configured for the users application. The operating modes and initialization procedures are described more completely in the R6500 Hardware Manual (Section 6) and the AIM 65 Microcomputer User's Manual (Section 8).

The reset routine must also initalize any external modules that would be affected by BRES/.

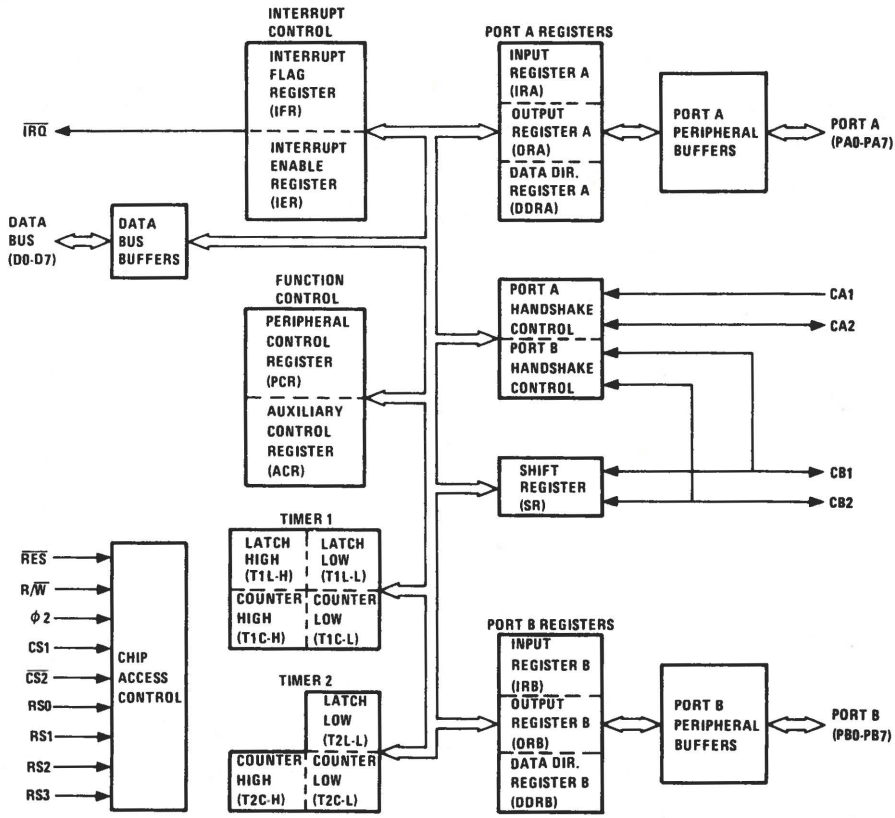


Figure 4-1. Versatile Interface Adapter Block Diagram

Table 4-2. Memory Map for SBC I/O (VIA)

Address	Port/Operation/Register	
	Write (R/$\overline{W}$ = Low)	Read (R/$\overline{W}$ = High)
XYZ0	(ORB) Peripheral Port B	(IRB)
XYZ1	(ORA) Peripheral Port A	(IRA)
XYZ2	Port B Data Direction Register (DDRB)	
XYZ3	Port A Data Direction Register (DDRA)	
	Timers (T1 and T2)	
XYZ4	Write T1L-L	Read T1C-L Clear T1 Interrupt Flag
XYZ5	Write T1L-H & T1C-H T1L-L to T1C-L Clear T1 Interrupt Flag	Read T1C-H
XYZ6	Write T1L-L	Read T1L-L
XYZ7	Write T1L-H Clear T1 Interrupt Flag	Read T1L-H
XYZ8	Write T2L-L	Read T2C-L Clear T1 Interrupt Flag
XYZ9	Write T2C-H T2L-L to T2C-L Clear T2 Interrupt Flag	Read T2C-H
XYZA	Shift Register (SR)	
XYZB	Auxiliary Control Register (ACR)	
XYZC	Peripheral Control Register (PCR)	
XYZD	Interrupt Flag Register (IFR)	
XYZE	Interrupt Enable Register (IER)	
XYZF	(ORA) Port A with no handshaking	(IRA)

NOTES

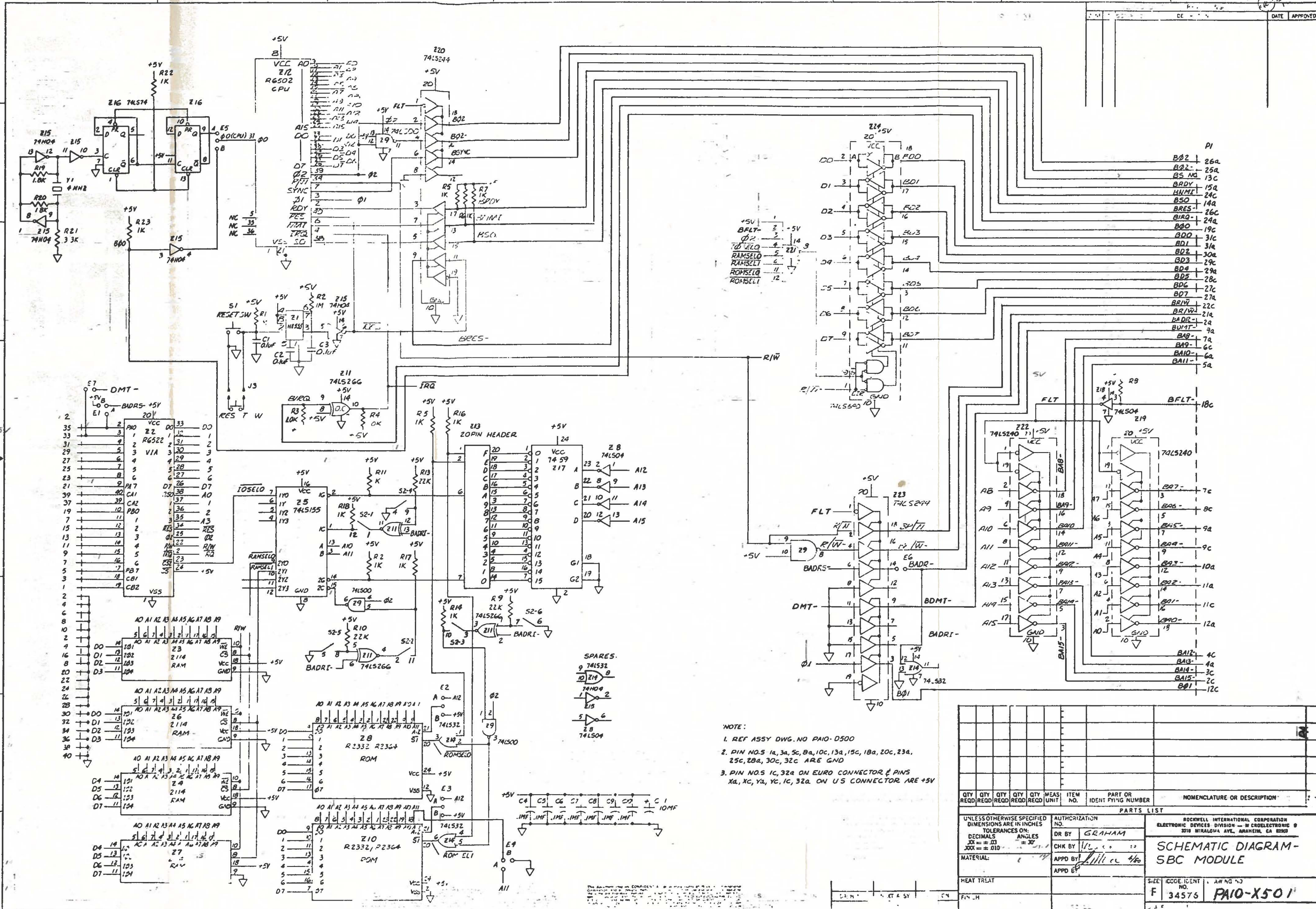
1. X corresponds to the assigned I/O Base Address.
2. Y can be 0, 1, 2, or 3 (lowest 1K of the 4K block).
3. Z can be any hexadecimal value.

4.4 DMA CONSIDERATIONS

The SBC has provision for an alternate RM 65 bus controller, such as a DMA Controller. The bus float (BFLT/) and DMA Terminate (BDMT/) signals are provided for this purpose.

When the SBC receives a bus float (BFLT/ at logic 0), only off-board signals are inhibited - the CPU continues execution. In normal applications, both a not ready (BRDY at logic 0) and a bus float is generated by the DMA Controller to stop CPU operations (CPU hold) until the Bus is again available. In special applications, however (e.g., a real time clock), the CPU must be allowed to continue operation (CPU active). In this case, only a bus float is generated by the DMA controller, but the CPU must never try to access off-board memory while bus float is active.

When the CPU has released control of the RM 65 bus in response to an active bus float, there are two methods of regaining control (other than by a hardware reset). The normal process would be an orderly release of the Bus by the DMA controller after a specified time. The other process is by the CPU issuing a DMA Terminate signal (BDMT/ at logic 0), to which the DMA controller must release all bus lines and remove the bus float (BFLT/ at logic 1). The DMA terminate can only be accomplished in a CPU active mode, and would generally disrupt the results of the DMA transfer in progress.



NOTE:

1. REF ASSY DWG. NO PA10-D500
2. PIN NO.S 1a, 3a, 5c, 8a, 10c, 13a, 15c, 18a, 20c, 23a, 25c, 28a, 30c, 32c ARE GND
3. PIN NO.S 1c, 32a ON EURO CONNECTOR & PINS Xa, Xc, Ya, Yc, 1c, 32a ON U.S CONNECTOR ARE +5V

QTY REQD	QTY REQD	QTY REQD	QTY REQD	QTY REQD	MEAS UNIT	ITEM NO.	PART OR IDENT FYING NUMBER	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON: DECIMALS .XX = ± .03 .XXX = ± .010 ANGLES ± 30'

MATERIAL

HEAT TREAT

FINISH

AUTHORIZATION NO.

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CHK BY

APPD BY

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SCHEMATIC DIAGRAM - SBC MODULE

SIZE F | CODE IDENT NO. 34576 | DWG NO PA10-X501

10-X501

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