RM 65 FAMILY

General Purpose Input/Output (I/O) & Timer Module

USER'S MANUAL

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Rockwell International

Document No. 29801 N01
Order No. 801
Rev. 1 October 1982

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$2.00
Document No. 29801 N01
Order No. 801
Rev. 1 October 1982

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SECTION 1

INTRODUCTION

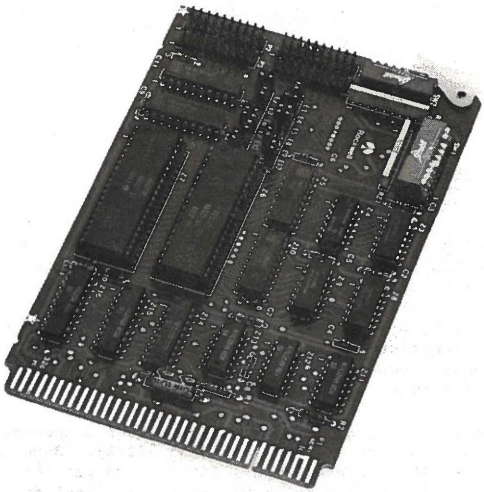
1.1 PURPOSE/FUNCTION

The RM65-5222 General Purpose Input/Output & Timer (GPIO & Timer) Module provides a powerful parallel I/O interface to the RM 65 Bus. All I/O port and control lines have TTL buffering. Two R6522 Versatile Interface Adapter (VIA) devices provide four 8-bit bidirectional I/O data ports and four 2-bit I/O control ports; 40 I/O lines in all. Eight switches allow the address to be set to any page (256 bytes). Eight switches (2 per I/O port) allow for manual setting of direction for I/O transceivers or software control by I/O port handshake lines. Jumpers are provided to allow configuration of handshake buffer direction.

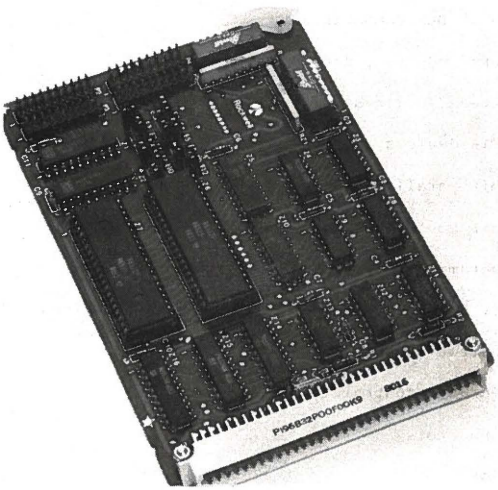
The GPIO & Timer module is available in a 72-pin Edge Connector version (RM65-5222) and a 64-pin Eurocard version (RM65-5222E). Both versions are shown in Figure 1-1. The pin assignments for the two versions are identical except that the edge connector version has four additional pins connected to +5V dc, and four unused pins (see Table 3-1 for pin assignments).

1.2 FEATURES

- o Rockwell RM 65 Bus compatible.
- o Fully buffered address, data and control lines
- o Fully buffered I/O lines
- o Two R6522 VIA devices provide
  - Four 8-bit parallel bidirectional data ports
  - Four 2-bit control ports
  - Four programmable 16-bit counter/timers
  - Two 8-bit shift registers for serial communications
- o Manual or Software control of I/O data direction
- o Jumper-selectable control line direction
- o Four I/O connectors
- o +5V operation
- o Base Address Select switches assign the GPIO & Timer module I/O addresses to one of 256 pages within the 65K byte bank.
- o Bank Select Enable switch assigns the module I/O common to both 65K byte memory banks or allows dedication to one memory bank.



a. Edge Connector Version



b. Eurocard Version

Figure 1-1. GPIO & Timer Module

- o Bank Select switch assigns the module I/O to one of two 65K byte memory banks.
- o Edge Connector and Eurocard versions.
- o Fully assembled, tested and warranted.

1.3 CHARACTERISTICS

The GPIO & Timer Module physical and electrical characteristics are defined in Table 1-1.

1.4 REFERENCE DOCUMENTS

Available from Rockwell

Document No.	
29650N30	R6500 Programming Manual
29650N31	R6500 Hardware Manual
29650N36	AIM 65 Microcomputer User's Guide
29650N82	RM 65 Bus Description
29000D47	R6522 Versatile Interface Adapter (VIA) Data Sheet

Table 1-1. GPIO & Timer Module Physical and Electrical Characteristics

Characteristics	Value
Physical Characteristics (See Figure 1-2)	
Edge Connector Version	
Width	3.9 in. (100 mm)
Length	6.5 in. (164 mm)
Height	0.56 in. (14 mm)
Weight	4.9 oz. (135 g)
Eurocard Version	
Width	3.9 in. (100 mm)
Length	6.3 in. (160 mm)
Height	0.56 in. (14 mm)
Weight	5.2 oz. (145 g)
Environment	
Operating Temperature	0° to 70°C
Storage Temperature	-40°C to 85°C
Relative Humidity	0% to 85% (without condensation)
Power Requirements	+5.0 $\pm$ 5% Vdc 0.87A (4.35W) - Maximum
Interface Connection (PI)	
RM 65 Bus Connection	
Edge Connector Version	72-pin edge connector (0.10 in. centers)
Eurocard Version	64-pin plug (0.10 in. centers) per DIN 41612 (Row b not installed)
I/O Connection (P2-P5)	20-pin mass terminating connector (0.10 in. centers) Mates to T&B Ansley 609-2000M or equiv.

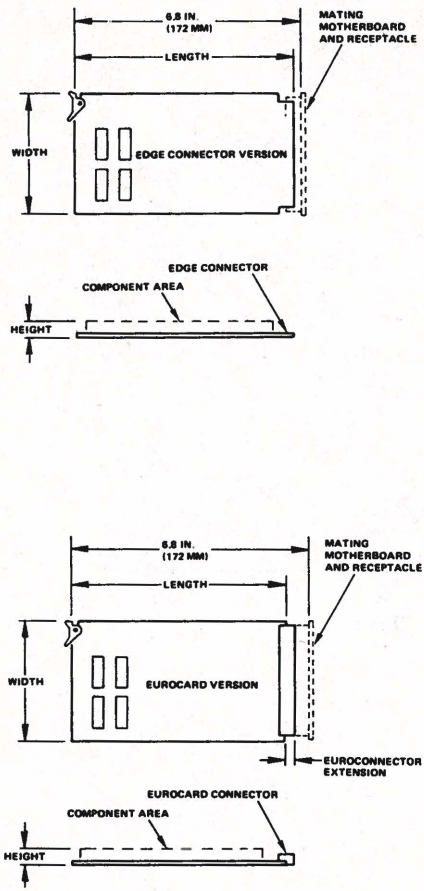


Figure 1-2. GPIO & Timer Module Outline

SECTION 2

INSTALLATION AND OPERATION

2.1 UNPACKING

Unpack the GPIO & Timer module from its shipping carton and, referring to the packing list, verify that all of the parts are included. Save the packing material for storing the module.

> **CAUTION**
>
> This module contains voltage sensitive items. The module should be stored in an anti-static container when not in use and anyone handling unit should observe anti-static precautions. Damage to the unit may result if anti-static protection is not maintained.

2.2 OPERATING OPTIONS

The switch or jumper selectable operating options are:

- Base Address selection
- Bank selection
- Program or Manual Direction control
- Control buffer direction

Figure 2-1 identifies the detail on the GPIO & Timer module. The function of each switch, jumper, or connector is identified in Table 2-1 along with reference to the section and table that describes its use.

2.2.1 Base Address Selection

The GPIO & Timer module with its associated VIA R6522 device registers are I/O locations in the system memory map. A base address that uniquely defines a page of 256 locations must be assigned to the GPIO & Timer module (the first 32 locations are unique while the remaining locations are redundant). The selected base address must correspond to the base address implemented by the system software (see Section 4.2). Set switches SW1-1 through SW1-8 to the positions listed in Table 2-2 to correspond to the required GPIO & Timer module base address.

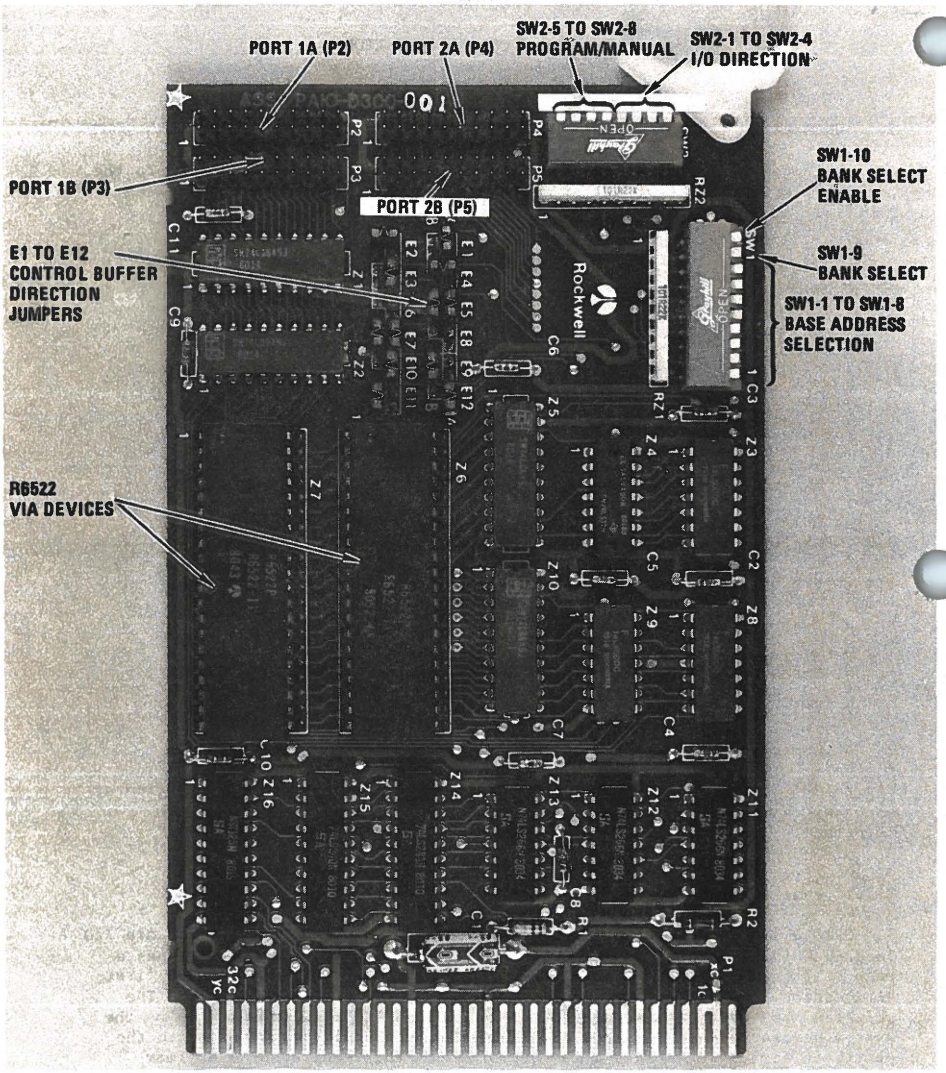


Figure 2-1. GPIO & Timer Module Detail

Table 2-1. GPIO & Timer Module Switches, Jumpers and Connectors

Category	Item	Description	Reference
Switches	SW1-1 to SW1-8	Base Address Select	Table 2-2 Section 2.2.1
	SW1-9	Bank Select	Table 2-3 Section 2.2.2
	SW1-10	Bank Select Enable	Table 2-3 Section 2.2.2
	SW2-1 to SW2-4	I/O Direction	Table 2-4 Section 2.2.3
	SW2-5 to SW2-8	Program/Manual Select	Table 2-4 Section 2.2.3
Jumpers	E1 to E12	Control Buffer Direction	Table 2-5 Section 2.2.4
Connectors	P1	RM 65 Bus Connection	Tables 3-1 and 3-3
	P2 to P5	Buffered I/O Connection	Tables 3-2 and 3-5

Table 2-2. Base Address Select Switch Positions

Switch SW1-5 - SW1-8 Positions					Switch SW1-1 - SW1-4 Positions				
Hex Value	SW1-8	SW1-7	SW1-6	SW1-5	Hex Value	SW1-4	SW1-3	SW1-2	SW1-1
0XXX	OPEN	OPEN	OPEN	OPEN	X0XX	OPEN	OPEN	OPEN	OPEN
1XXX	OPEN	OPEN	OPEN	CLOSED	X1XX	OPEN	OPEN	OPEN	CLOSED
2XXX	OPEN	OPEN	CLOSED	OPEN	X2XX	OPEN	OPEN	CLOSED	OPEN
3XXX	OPEN	OPEN	CLOSED	CLOSED	X3XX	OPEN	OPEN	CLOSED	CLOSED
4XXX	OPEN	CLOSED	OPEN	OPEN	X4XX	OPEN	CLOSED	OPEN	OPEN
5XXX	OPEN	CLOSED	OPEN	CLOSED	X5XX	OPEN	CLOSED	OPEN	CLOSED
6XXX	OPEN	CLOSED	CLOSED	OPEN	X6XX	OPEN	CLOSED	CLOSED	OPEN
7XXX	OPEN	CLOSED	CLOSED	CLOSED	X7XX	OPEN	CLOSED	CLOSED	CLOSED
8XXX	CLOSED	OPEN	OPEN	OPEN	X8XX	CLOSED	OPEN	OPEN	OPEN
9XXX	CLOSED	OPEN	OPEN	CLOSED	X9XX	CLOSED	OPEN	OPEN	CLOSED
AXXX	CLOSED	OPEN	CLOSED	OPEN	XAXX	CLOSED	OPEN	CLOSED	OPEN
BXXX	CLOSED	OPEN	CLOSED	CLOSED	XBXX	CLOSED	OPEN	CLOSED	CLOSED
CXXX	CLOSED	CLOSED	OPEN	OPEN	XCXX	CLOSED	CLOSED	OPEN	OPEN
DXXX	CLOSED	CLOSED	OPEN	CLOSED	XDXX	CLOSED	CLOSED	OPEN	CLOSED
EXXX	CLOSED	CLOSED	CLOSED	OPEN	XEXX	CLOSED	CLOSED	CLOSED	OPEN
FXXX	CLOSED	CLOSED	CLOSED	CLOSED	XFXX	CLOSED	CLOSED	CLOSED	CLOSED

NOTES

1. The Most Significant Digit (MSD) corresponds to address lines BA15/ - BA12/.

2. The Least Significant Digit (LSD) corresponds to address lines BA11/ - BA8/.

2.2.2 Bank Selection

The Bank Select Enable switch (SW1-10), in conjunction with the Bank Select switch (SW1-9), allows the GPIO & Timer module to be assigned common to both memory banks (Bank 0 and Bank 1) or to be dedicated to a selected memory bank (either Bank 0 or Bank 1).

When OPEN, the Bank Select Enable switch assigns the GPIO & Timer module common to both banks, regardless of the position of the Bank Select switch. When the Bank Select Enable switch is CLOSED, the assigned bank is determined by the position of the Bank Select switch. See Table 2-3 for the switch positions.

In applications where the module is to be addressed by devices that do not have bank addressing capabilities, the module must be assigned common to Bank 0 and Bank 1, or dedicated to Bank 0.

Table 2-3. Bank Select Switch Positions

Memory Bank Selected	Switch Position	
	Bank Select Enable Switch SW1-10	Bank Select Switch SW1-9
Bank 0 and 1	OPEN	EITHER
Bank 0 (Lower 65K)	CLOSED	OPEN
Bank 1 (Upper 65K)	CLOSED	CLOSED

2.2.3 Program/Manual and I/O Direction Selection

The Program/Manual switches (SW2-5 to SW2-8) choose the source of the I/O Direction control for each of the four 8-bit I/O peripheral ports. When in the Program position, the direction of each port's I/O transceiver is set through software, by a control line. When in the Manual position, the direction of the I/O transceiver is controlled manually by the port's I/O Direction switch (SW2-1 to SW2-4).

When a Program/Manual switch is CLOSED, the associated port's I/O transceiver is in Manual Mode. This makes the direction dependent on the port's I/O Direction switch, with an OPEN making the port an input, and a CLOSED defining an output port.

When a Program/Manual switch is OPEN, the associated I/O transceiver is in the Program controlled mode. This makes the direction independent of the I/O Direction switch and dependent on the level of the control line 2 for the associated port. When this control line is set LOW (0), the port will receive input data. When this control line is HIGH (1), the port will send output data. Control line 2 can be set or reset from the RM 65 bus, which makes the direction of the I/O transceivers selectable under program control. See Table 2-4 for switch positions.

CAUTION

The Program/Manual and I/O Direction switches control direction of the Buffers only. To configure a port for input or output, the VIA device must also be initialized properly (see section 4.3). If the Buffers and the VIA are not initialized correctly, damage may occur to the VIA device.

Table 2-4. Program/Manual and I/O Direction Switch Positions

I/O Port Function	Switch Position	
	I/O Direction	Program/Manual
VIA No. 1, Port A	SW2-1	SW2-5
Manual Input	OPEN	CLOSED
Manual Output	CLOSED	CLOSED
Program Control (CA2)	EITHER	OPEN
VIA No. 1, Port B	SW2-2	SW2-6
Manual Input	OPEN	CLOSED
Manual Output	CLOSED	CLOSED
Program Control (CB2)	EITHER	OPEN
VIA No. 2, Port A	SW2-3	SW2-7
Manual Input	OPEN	CLOSED
Manual Output	CLOSED	CLOSED
Program Control (CA2)	EITHER	OPEN
VIA No. 2, Port B	SW2-4	SW2-8
Manual Input	OPEN	CLOSED
Manual Output	CLOSED	CLOSED
Program Control (CB2)	EITHER	OPEN

NOTE

Program Control direction is set for each port by it's associated control line 2. (0 = Input; 1 = Output.)

2.2.4 Control Buffer Direction Selection

The Control Buffer Selection Jumpers (E1-E12) allow the bidirectional control lines to be buffered as either input or output lines. If the control signal is desired to be bidirectional, the buffer can be bypassed and a direct connection made between the VIA and the I/O connector.

Table 2-5. Control Buffer Direction Jumper Positions

Control Signal	Jumper Position		
	Input	Output	Bidirectional
1CA2	E1 = A E2 = B	E1 = B E2 = A	E1 = A & B E2 = NONE
2CA2	E3 = A E4 = B	E3 = B E4 = A	E3 = A & B E4 = NONE
1CB1	E7 = A E8 = B	E7 = B E8 = A	E7 = A & B E8 = NONE
2CB1	E9 = A E10 = B	E9 = B E10 = A	E9 = A & B E10 = NONE
1CB2	E5 = A E6 = B	E5 = B E6 = A	E5 = A & B E6 = NONE
2CB2	E11 = A E12 = B	E11 = B E12 = A	E11 = A & B E12 = NONE

CAUTION

For every mode, there are two jumpers. The two jumpers are ALWAYS paired, one A and one B. If any control signal has two A or two B jumpers, the line is configured wrong and may cause damage to the VIA device.

The Control Buffer Direction Jumpers control the direction of the Buffers only. The VIA control signals must still be initialized to the proper operating mode (see Section 4.3). If the VIA device is not initialized to match the control buffering, damage may result.

An example of using jumpers to select different Control Buffer directions an is shown in Table 2-6 and Figure 2-2.

2.3 INSTALLING THE MODULE

Prior to installing the module, ensure that it is not damaged and is free of grease, dirt, or other foreign matter. Install the module as follows:

CAUTION

Before installing the module, turn off power to the RM 65 Bus interface and to any interfacing external equipment.

Table 2-6. Example Placement of Control Buffer Jumpers

Control Signal	Buffer Direction	Jumper Positions
1CA1	Input	None
2CA1	Input	None
1CA2	Input	E1 = A E2 = B
2CA2	Input	E3 = A E4 = B
1CB1	Bidirectional	E7 = A & B E8 = NONE
2CB1	Output	E9 = B E10 = A
1CB2	Bidirectional	E5 = A & B E6 = NONE
2CB2	Output	E11 = B E12 = A

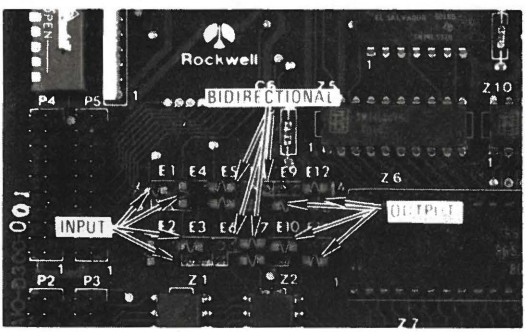


Figure 2-2. Example of Control Buffer Jumper Positions

a. Select the proper module operating options by performing the following steps:

   (1) Select the module base address by positioning switches SW1-1 through SW1-8 (refer to Section 2.2.1 and Table 2-2). Consult the system software memory map for the base address requirement.

   (2) Select common or dedicated memory bank operation by positioning switches SW1-9 and SW1-10 (refer to Section 2.2.2 and Table 2-3).

   (3) Select the proper I/O Direction Control by setting switches SW2-1 through SW2-8 (refer to Section 2.2.3 and Table 2-4 for the desired mode.

   (4) Select the proper Control Buffer Direction by installing jumpers E1 through E12 (refer to Section 2.2.4 and Table 2-5) as required.

b. Align pin Wa (Edge Connector version) or pin 1a (Eurocard version) of the module with the corresponding pin on the mating RM 65 bus receptacle.

CAUTION

RM 65 bus connectors are keyed to prevent improper module connection. If the module does not insert into the receptacle with moderate pressure applied, check the orientation and connector alignment of the module. Forcing module improperly into the receptacle will damage the receptacle and/or the module.

c. Insert the module into the desired card slot (if a card cage is used) and position it in front of the mating receptacle.

d. Connect the cables from the external equipment to I/O connectors on the GPIO & Timer module as appropriate (see Figure 2-1).

e. Press in firmly on the end of module until all pins are securely seated.

NOTE

Interface cables that connects the GPIO & Timer module to the external devices are supplied by the user.

f. Reapply power to the system, card cage, or motherboard.

2.4 REMOVING THE MODULE

a. Turn-off power to the RM 65 bus and the interfacing external equipment.

b. Disconnect the cables from the I/O connectors.

c. If the module is installed in a card cage, lift up on the module ejector tab to release the module from the mating receptacle. Pull the module straight back until it is free from the card slot guides.

d. If the module is installed in a single card adapter, or in a motherboard without a card cage, pull back on the module while moving it slightly from side to side until it is free from the mating receptacle.

SECTION 3

FUNCTIONAL AND INTERFACE DESCRIPTION

3.1 FUNCTIONAL DESCRIPTION

The heart of the GPIO & Timer module is two R6522 Versatile Interface Adapter (VIA) devices. Each VIA provides two 8-bit bidirectional input/output ports, four I/O control lines, two fully programmable 16-bit timer/counters and an 8-bit shift register for serial interface. There is also control of interrupt generation from independent I/O conditions.

The two 8-bit input/output peripheral ports are fully bidirectional. Data Direction registers allow each peripheral pin to independently act as either an input or an output, although in the module all lines of a port must be set in the same direction. The four control lines can also be used for I/O or can provide handshaking for the associated data ports. Each control input can be programmed to interrupt the microprocessor on detection of a rising or falling edge.

The two 16-bit counter/timers are capable of many complex timing and counting functions. One timer provides four modes of operation: free running, with a pulsed or toggled output on a peripheral port line, one-shot interval timer with a pulsed output on a peripheral port line, or one-shot interval timer with a toggle output on a peripheral port line. The three modes of the second 16-bit timer provide a one-shot interval timer, a count of external pulses, or a clock for the serial shift register. The shift register can shift data in or out at the system clock rate, the timer clock rate, or an external clock rate. Both timers and the shift register can be programmed to interrupt the microprocessor upon time-out or shift completion.

The Data Transceivers invert and buffer 8-bits of parallel data (BD0/-BD7/) between the RM 65 Bus and the two R6522 VIA devices. The Data Transceivers are enabled when a valid address is present at the Base Address Decoders. During a read operation, data is transferred from the addressed R6522 to the RM 65 Bus. During a write operation, data is transferred from the RM 65 Bus to the addressed R6522.

The Address Buffers invert and transfer the five least significant address bits (BA0/-BA4/) from the RM 65 Bus. The four LSB bits select the R6522 registers, while the remaining line selects one of the two VIA devices.

The Bank Select Controller detects when the GPIO & Timer Module's assigned memory bank is addressed by comparing the level of the bank address signal (BADR/) from the RM 65 Bus to the Bank Select Enable (SW1-10) and Bank Select switches (SW1-9). The Bank Select Enable switch allows the module to be assigned common to both banks, or to Bank 0 (lower 65K) or Bank 1 (upper 65K) depending on the Bank Select switch. If the BADR/ signal level matches the assigned memory bank, the Bank Select Controller enables the Base Address Decoders.

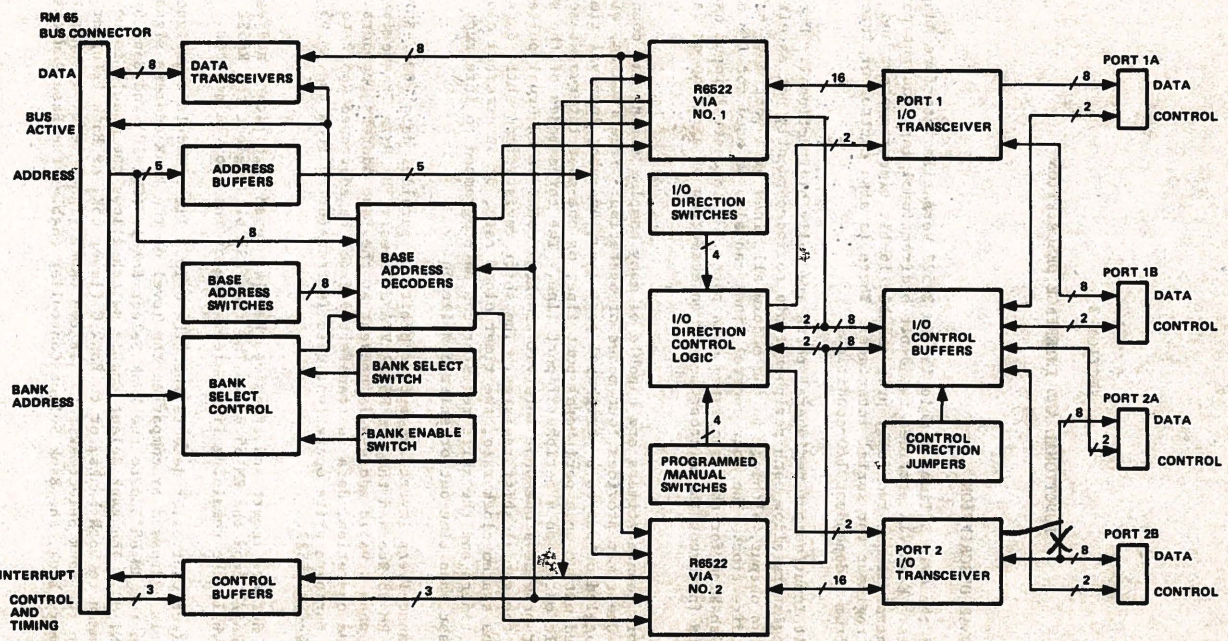


Figure 3-1. GPIO & Timer Module Block Diagram

The Control Buffers drive read/write (BR/$\overline{W}$/), phase 2 clock (BØ2/), and reset (BRES/) signals from the RM 65 Bus to the GPIO & Timer Module. The interrupt request (BIRQ/) and bus active (BACT/) signals are driven onto the Bus from the Module.

The Base Address Decoders use the eight most significant address lines (BA8/-BA15/) to assign the 32 I/O addresses to a page (256 bytes) boundary. When an address is within range of the Base Address switches (SW1-8 to SW1-1) and the Bank Select Control is enabled, one of the two chip selects is generated to the R6522 devices.

Four I/O Direction switches (SW2-1 to SW2-4) provide direction control to each of the Port I/O transceivers. Four Programmed/Manual Select switches (SW2-5 to SW2-8) allow the direction control to be established from the Direction Control switches in the Manual mode or from a R6522 VIA control line (Control 2) in the Programmed mode.

The I/O Transceivers buffer each of four 8-bit I/O ports. The direction is determined by the Direction Control logic. There are also eight buffers provided for the control lines (2 per I/O port), six of which can be configured for input or output as determined by the Handshake Direction Buffers.

Twelve Control Direction jumpers (E1-E12) allow the three bidirectional control lines (CA2, CB1, and CB2) on each R6522 to be configured for either input or output mode.

3.2 INTERFACE DESCRIPTION

Table 3-1 lists pin connections for I/O signals transferred between GPIO & Timer module connector P1 and the RM 65 Bus.

Table 3-2 lists pin connection for the Buffered I/O Data and Control signals.

Tables 3-3 and 3-4 describe all I/O signals in detail.

All I/O Data and Control signals are brought to four connectors that will each accept a 20-pin receptacle mass terminated on a ribbon cable (cable and mass terminated connectors are not supplied with the GPIO & Timer). Each connector is dedicated to one port with 8 Data, 2 Control and 10 ground lines.

Table 3-1. Connector P1 (RM 65 Bus) Pin Assignments

Pin	Signal Mnemonic	Signal Name
Wa		Not Connected (See Note)
Wc		Not Connected (See Note)
Xa	+5V	+5 Vdc (See Note)
Xc	+5V	+5 Vdc (See Note)
1a	GND	Ground
1c	+5V	+5 Vdc
2a	BADR/	Buffered Bank Address
2c	BA15/	Buffered Address Bit 15
3a	GND	Ground
3c	BA14/	Buffered Address Bit 14
4a	BA13/	Buffered Address Bit 13
4c	BA12/	Buffered Address Bit 12
5a	BA11/	Buffered Address Bit 11
5c	GND	Ground
6a	BA10/	Buffered Address Bit 10
6c	BA9/	Buffered Address Bit 9
7a	BA8/	Buffered Address Bit 8
7c	BA7/	Not Used
8a	GND	Ground
8c	BA6/	Not Used
9a	BA5/	Not Used
9c	BA4/	Buffered adress Bit 4
10a	BA3/	Buffered Address Bit 3
10c	GND	Ground
11a	BA2/	Buffered Address Bit 2
11c	BA1/	Buffered Address Bit 1
12a	BA0/	Buffered Address Bit 0
12c		Not Used
13a	GND	Ground
13c		Not Used
14a		Not Used

Table 3-1. Connector P1 (RM 65 Bus) Pin Assignments (Continued)

Pin	Signal Mnemonic	Signal Name
14c		Not Used
15a		Not Used
15c	GND	Ground
16a		Not Used
16c		Not Used
17a		Not Used
17c		Not Used
18a	GND	Ground
18c		Not Used
19a		Not Used
19c		Not Used
20a		Not Used
20c	GND	Ground
21a	BR/$\overline{W}$/	Buffered Read/Write "Not"
21c		Not Used
22a		Not Used
22c		Not Used
23a	GND	Ground
23c	BACT/	Buffered Bus Active
24a	BIRQ/	Buffered Interrupt Request
24c		Not Used
25a	BØ2/	Buffered Phase 2 "Not" Clock
25c	GND	Ground
26a		Not Used
26c	BRES/	Buffered Reset
27a	BD7/	Buffered Data Bit 7
27c	BD6/	Buffered Data Bit 6
28a	GND	Ground
28c	BD5/	Buffered Data Bit 5
29a	BD4/	Buffered Data Bit 4
29c	BD3/	Buffered Data Bit 3

Table 3-1. Connector P1 (RM 65 Bus) Pin Assignments (Continued)

Pin	Signal Mnemonic	Signal Name
30a	BD2/	Buffered Data Bit 2
30c	GND	Ground
31a	BD1/	Buffered Data Bit 1
31c	BD0/	Buffered Data Bit 0
32a	+5V	+5 Vdc
32c	GND	Ground
Ya	+5V	+5 Vdc (See Note)
Yc	+5V	+5 Vdc (See Note)
Za		Not Connected (See Note)
Zc		Not Connected (See Note)

NOTE

Pins Wa, Wc, Xa, Xc, Ya, Yc, Za and Zc are not used on the Eurocard version.

Table 3-2. Connector P2-P5 (Buffered I/O) Pin Assignments

Pin	Signal
1	Port data 0
3	Port data 1
5	Port data 2
7	Port data 3
9	Port data 4
11	Port data 5
13	Port data 6
15	Port data 7
17	Port control C1
19	Port control C2

NOTES

1. Similar for all ports; 1A(P2), 1B(P3), 2A(P4), and 2B(P5).
2. Even pins 2-20 are ground.

Table 3-3. Connector P1 (RM 65) Signal Descriptions

Signal Mnemonic	Signal Name and Signal Description
	NOTE: All signals interfaced to and from the system bus driven at TTL voltage levels.
+5V	+5V dc supplied to the GPIO & Timer module from the RM 65 Bus.
GND	Ground System ground.
BA0/-BA15/	Buffered Address Bits 0-15 Sixteen address lines transfer a 16-bit address from the Bus to the GPIO & Timer module.
BD0/-BD7/	Buffered Data Bits 0-7 Eight bidirectional data lines for transferring 8-bit data bytes between tri-state Data Transceivers in the GPIO & Timer module and the Bus.
BACT/	Buffered Bus Active A low BACT/ indicates that the GPIO & Timer module has been addressed and the Data Tranceivers are enabled in either the receive (write operation) or transmit (read operation) direction. A high BACT/ indicates that the Data Transceivers are disabled.
BADR/	Buffered Bank Address A high BADR/ addresses the lower 65K (Bank 0) memory bank; a low BADR/ addresses the upper 65K (Bank 1) memory bank.
BR/$\overline{W}$/	Buffered Read/Write "NOT" A low BR/$\overline{W}$/ (read operation) to an addressed GPIO & Timer module enables the Data Transceivers to transfer the 8-bit data from the module onto the Bus. A high BR/$\overline{W}$/ (write operation) to an addressed module enables the Data Transceivers to transfer data from the Bus onto the Module. The BR/$\overline{W}$/ also provides control for the VIA devices.
BØ2/	Buffered Phase 2 Clock "NOT" VIA device addressing and data transfers are synchronized to the negative portion of the BØ2/ clock.

Table 3-3. Connector P1 (RM 65) Signal Descriptions (Cont)

Signal Mnemonic	Signal Name and Signal Description
BRES/	Buffered Reset This line transfers the BRES/ reset signal from the to the two R6522 devices. A low BRES/ signal clears all the internal registers in the R6522 devices to logic 0 (except T1, T2 and SR).
BIRQ/	Buffered Interrupt Request This line transfers the BIRQ/ interrupt signal from both of the R6522 devices onto the Bus. BIRQ/ is normally a high level and goes low when the R6522 requests service due to any of the enabled interrupt conditions being valid.

Table 3-4. Connector P2-P5 (Buffered I/O) Signal Definitions

Signal Mnemonic	Signal Name and Signal Description
B1PA0 - B1PA7 (P2) B1PB0 - B1PB7 (P3) B2PA0 - B2PA7 (P4) B2PB0 - B2PB7 (P5)	Buffered I/O Port Data Bits 7-0 These are the buffered I/O port Data lines for the VIA devices. P2 corresponds to VIA 1-Port A, P3 to Port B. P4 corresponds to VIA 2-Port A, P5 to Port B. The buffering direction for each port is dependent on the respective Direction and Program/Manual Switch positions, and the port's control line 2. Because of the buffering, any port must be completely input or output (all bits must be the same direction at any time).
B1CA1 (P2) B1CB1 (P3) B2CA1 (P4) B2CB1 (P5)	Buffered I/O Port Control 1 These are the buffered I/O port control 1 lines. The control lines are available for handshaking and perhipheral control. The buffering direction of port B control 1 for both VIA devices must be set by the Control Buffer Direction Jumpers. The buffering direction of port A control 1 is fixed as an input because there is no output mode for this line of the VIA devices.
B1CA2 (P2) B1CB2 (P3) B2CA2 (P4) B2CB2 (P5)	Buffered I/O Port Control 2 These are the buffered I/O port control 2 lines. The control lines are available for handshaking and peripheral control. These lines are also used to control the direction of the Buffered I/O Port Data lines when the Programmed/Manual Switch is in the Programmed mode. The buffering direction of Control 2 for both VIA devices port A and port B must be set by the Control Buffer Direction Jumpers.

SECTION 4

PROGRAMMING CONSIDERATIONS

4.1 GENERAL CONSIDERATIONS

The GPIO & Timer module provides many powerful features for the user. To configure the module to the required I/O functions, it is important to keep in mind the features and limitations of the module and the VIA devices. Typical design decisions for the module include:

- Which ports are to be inputs or outputs?
- The direction, polarity (i.e., active high or active low), and transition sensitivity (i.e., rising or falling edge) of the control signals?
- Which functions will be required on each device (i.e., timers or shift register)?
- Polling or Interrupt driven modes of operation?

Figure 4-1 shows a block diagram of the VIA.

4.2 GPIO & TIMER MODULE MEMORY MAP

The R6522 VIA devices on the module are designated a page (256 bytes) of address space within the RM 65 memory map. The module is assigned a base address (on any page boundary) and all internal registers are accessed relative to this base address. Since there are two VIA devices, there are 32 unique registers within the module (16 per VIA). Although an entire page is dedicated to the module, only the first 32 bytes are unique, while the remaining 224 bytes are redundant (copies of the first 32 bytes). Table 4-1 relates the address mapping of the module to the various I/O functions.

If bank addressing is used, BADR/ must be driven under software control. BADR/ must be controlled to select the desired bank before that bank is addressed.

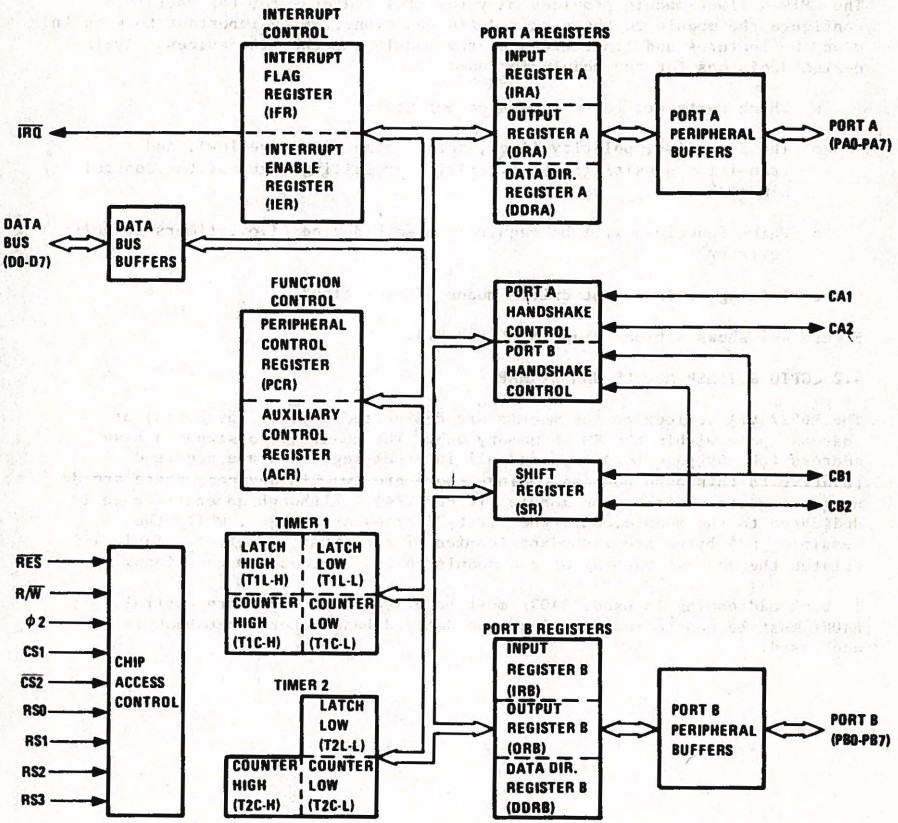


Figure 4-1. Versatile Interface Adapter Block Diagram

Table 4-1. GPIO & Timer Memory Mapping

Address	Port/Operation/Register	
	Write (BR/$\overline{W}$/ = High)	Read (BR/$\overline{W}$/ = Low)
XYZ0	(ORB) Peripheral Port B	(IRB)
XYZ1	(ORA) Peripheral Port A	(IRA)
XYZ2	Port B Data Direction Register (DDRB)	
XYZ3	Port A Data Direction Register (DDRA)	
	Timers (T1 and T2)	
XYZ4	Write T1L-L	Read T1C-L Clear T1 Interrupt Flag
XYZ5	Write T1L-H & T1C-H Transfer T1L-L to T1C-L Clear T1 Interrupt Flag	Read T1C-H
XYZ6	Write T1L-L	Read T1L-L
XYZ7	Write T1L-H Clear T1 Interrupt Flag	Read T1L-H
XYZ8	Write T2L-L	Read T2C-L Clear T1 Interrupt Flag
XYZ9	Write T2C-H Transfer T2L-L to T2C-L Clear T2 Interrupt Flag	Read T2C-H
XYZA	Shift Register (SR)	
XYZB	Auxiliary Control Register (ACR)	
XYZC	Peripheral Control Register (PCR)	
XYZD	Interrupt Flag Register (IFR)	
XYZE	Interrupt Enable Register (IER)	
XYZF	(ORA) Port A with no handshaking	(IRA)

NOTES

1. XY corresponds to the assigned Base Address
2. For VIA 1, Z is any even hexadecimal value (0, 2, 4, 6, 8, A, C, E).
3. For VIA 2, Z is any odd hexadecimal value (1, 3, 5, 7, 9, B, D, F).

4.3 INITIALIZATION SOFTWARE

Any time the GPIO & Timer Module receives a RESET from the RM 65 bus (BRES/), the VIA devices are initialized to a reset condition, with all registers cleared to a logic 0 (except for Timer 1, Timer 2, and the Shift Register). The RESET places all VIA peripheral interface lines in the input state, disables the timers and shift registers, and disables interrupts from the module. The RESET will also cause any I/O Transceiver in the PROGRAM mode to become an output, though not affecting any I/O Transceiver in the MANUAL mode or any of the control buffers.

After receiving a RESET, each VIA device must be configured for the required application by the following steps:

a. The Data Direction Registers determine if a VIA peripheral port (PA0-PA7 or PB0-PB7) will be an input (default by RESET) or an output.

   Although the VIA devices allow independent direction control of each bit line, the I/O Transceivers require all bit lines of a port to be the same direction, corresponding to the I/O Transceiver direction.

> **CAUTION**
>
> Prior to this programmed initialization, the Program/Manual and Direction switches must be properly set for each VIA port.

   When an I/O Transceiver is in the MANUAL mode, the corresponding Data Direction Register must reflect the I/O Direction switch position, with a $00 for Input and an $FF for Output.

   When an I/O Transceiver is in the PROGRAM mode, the Data Direction Register should reflect the programmed direction, which is set by the corresponding Control 2 line. When Control 2 is a logic 1 (default by RESET), the I/O direction will be Output and the Data Direction Register should be set to $FF for Output. When Control 2 is a logic 0, the Data Direction Register must be $00 for Input.

b. The Peripheral Control Registers determine the functions associated with the peripheral control lines (input by default after RESET).

   The Control 1 lines (CA1,CB1) can both be set to input mode, with the choice of active transition level (positive or negative edge), while CB1 also has an output mode when used with the shift register. The Control 2 lines (CA2, CB2) can be set to input mode, with the selection of active transition level and handshake operation, as well as to output mode, with the selection of a steady output level (high or low), pulsed output, or handshake output. The Control Buffer Direction jumpers must always be set to reflect the operating mode of the associated control line.

CAUTION
Prior to this programmed initialization, the Control Buffer Direction jumpers must be properly configured for each control line.

c. The Auxiliary Control Register determines the timer and shift register operations, and enables latching of the VIA peripheral ports (both timers, the shift register, and port latching are disabled by RESET). Because both timers use the peripheral B port (T1 uses PB7, T2 uses PB6) in certain modes, the I/O Transceiver must be configured to match the selected mode. When active, the shift register uses the B port control lines (CB2 is serial data, CB1 is the clock), so the associated Control Buffer Direction jumpers must be set for the required mode.

d. The Interrupt Enable Register allows all VIA interrupts - the four peripheral control lines, both timers, and the shift register - to be independently enabled (all interrupts are disabled by RESET).

Once these initialization steps are completed, the GPIO & Timer module is configured for the users application. The operating modes and initialization procedures are described more completely in the R6500 Hardware Manual (Section 6) and the AIM 65 Microcomputer User's Manual (Section 8).

4.4 MAIN-LINE SOFTWARE

The main-line software will always be unique to a given application. There are certain operating procedures that should be considered:

a. When an I/O Data Port is to be used in the PROGRAM mode, the procedure to change direction is important.

   To change an input port to an output port, first change the I/O Transceiver to an output (Control 2 line is a logic 1), then set the VIA port to the output mode (Data Direction Register is $FF).

   To change an output port to an input port, first change the VIA port to the input mode (Data Direction Register is $00), then make the I/O Transceiver an input (Control 2 line is a logic 0).

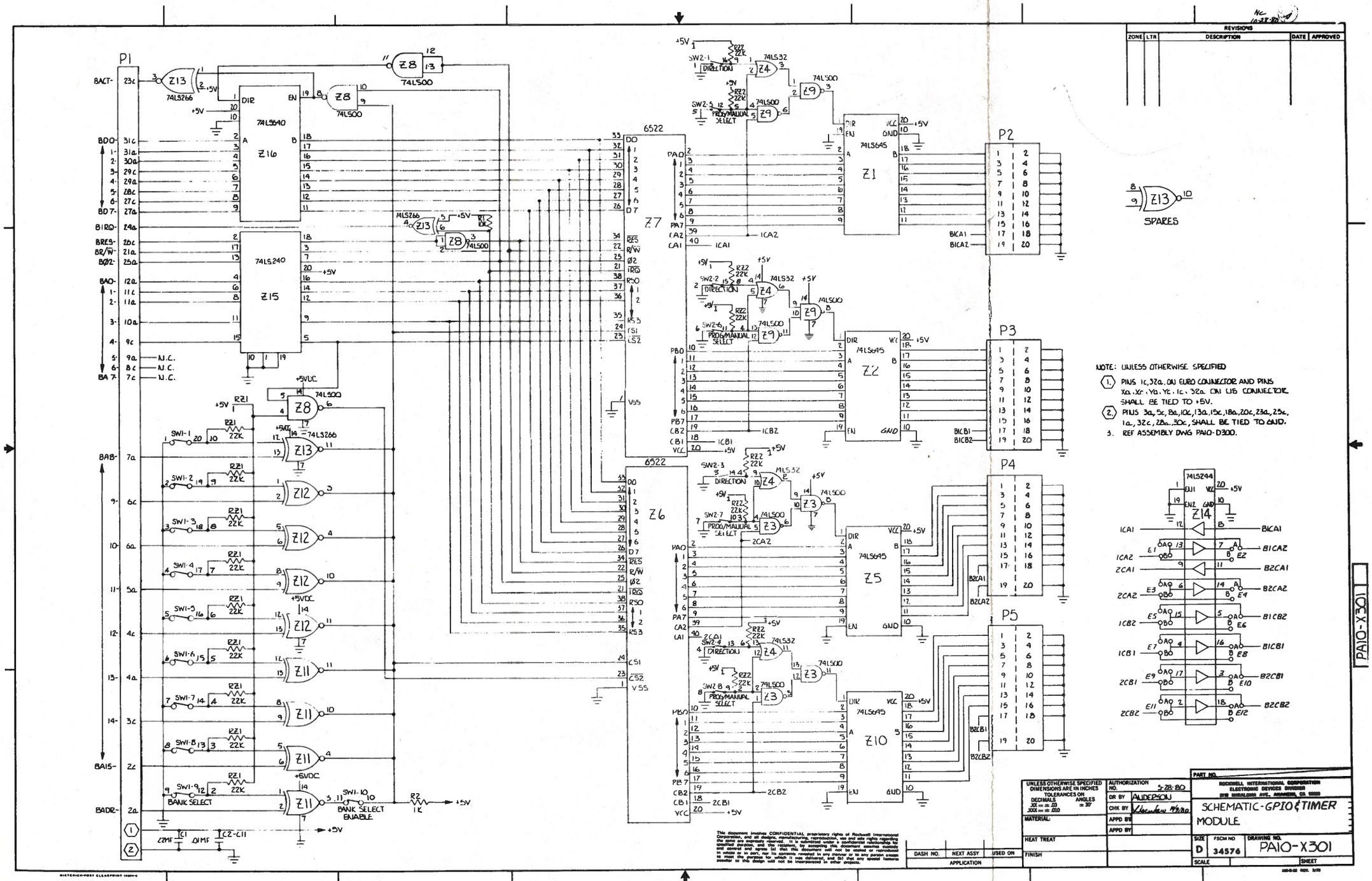
b. To use Timer 1 with the output to port B bit 7 enabled, the entire port B and the I/O Transceiver must be set for output. Care must be taken because this mode overrides the Data Direction Register.

c. To use Timer 2 in the count mode, the entire port B and the I/O Transceiver must be set for input.

d. When the Shift register is used, the B control lines 1 and 2 must always be set for the corresponding mode.

e. During software development or when a port is not being used, the I/O Transceiver may be placed in the MANUAL mode, output direction, to ensure that no inadvertant write will be able to damage the VIA device.

f. Damage can occur only if a VIA peripheral line is in the output mode while the associated buffer is an input. This situation can always be avoided by careful programming.


P1
P2
P3
P4
P5
Z1
Z2
Z3
Z4
Z5
Z6
Z7
Z8
Z9
Z10
Z11
Z12
Z13
Z14
Z15
Z16
6522
74LS640
74LS240
74LS645
74LS595
74LS244
74LS266
74LS32
74LS00
SPARES
DIRECTION
PROG/MANUAL SELECT
BANK SELECT
BANK SELECT ENABLE
NOTE: UNLESS OTHERWISE SPECIFIED
1. PINS 1c,32a..0N EURO CONNECTOR AND PINS 2a..2c,4a..4c,6a..6c,8a..8c,10a..10c,12a..12c,14a..14c,16a..16c,18a..18c,20a..20c,22a..22c,24a..24c,26a..26c,28a..28c,30a..30c, ON U15 CONNECTOR, SHALL BE TIED TO +5V.
2. PINS 3a,5c,8a,10c,13a..15c,18a..20c,23a..25c, 1a..3c,28a..30c, SHALL BE TIED TO GND.
3. REF ASSEMBLY DWG PA10-D300.
REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
PA10-X301
SCHEMATIC-GPIO&TIMER MODULE
ROCKWELL INTERNATIONAL CORPORATION
ELECTRONIC DEVICES DIVISION
AUTHORIZATION 5-28-80
DR BY AUDERSON
SIZE D
FSCM NO 34576
DRAWING NO. PA10-X301
SCALE
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