Rockwell

RM65-5101E
RM 65 FLOPPY DISK CONTROLLER (FDC) MODULE

RM 65 MICROCOMPUTER MODULES

The RM65-5101E Floppy Disk Controller Module is one of the hardware options available for the RM 65 Microcomputer Module family.

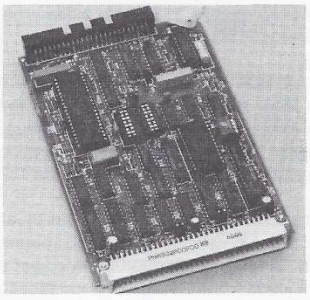
RM 65 Microcomputer Module products are designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

RM 65 modules use a motherboard interconnect concept and accept any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A selection of card cages provides packaging flexibility. RM 65 products may also be used with Rockwell AIM 65 and AIM 65/40 Microcomputers for product development and for a broad variety of portable or desktop microcomputer applications.

PRODUCT OVERVIEW

The RM 65 Floppy Disk Controller (FDC) Module controls up to four standard (8") or mini- (5¼") floppy disk drives, single or double sided, soft sectored with either single density (FM) or double density (MFM) format. Software control of media density allows single or double density disks to be used in any connected drives.

Two DIP headers configure the FDC to interface with either standard or mini-floppy disk drives. An on-board jumper selects single or double sided drives and a switch disables on-board ROM. The FDC directly interfaces to most popular drives with only switch and/or header changes. Bank Select and Bank Select Enable switches allow the FDC module to be dedicated to one of two 65K memory banks or assigned common to both banks. The FDC module I/O can be assigned to any page (256 bytes) using a standard PROM if the ROM is deselected.



RM65-5101E Floppy Disk Controller (FDC) Module

FEATURES

- Compact size—about 4" × 6¼" (100 mm × 160 mm)
- Pin and socket bus connection
- RM 65 Bus compatible
- Buffered address, data and control lines
- Supports single or double sided, standard or mini-floppy disk drives
- Controls up to four disk drives
- Interfaces directly to Shugart SA-850 or SA-450 disk drives, with user options for other popular floppy disk drives
- Supports single-density IBM 3740 (FM) or double-density IBM System 34 (MFM) formats
- DMA data transfer capability
- Supports interrupt-driven or polled operation
- Bipolar PROM Base Address decoding
- Switches or jumpers for
  - —Bank Selection to one or two banks
  - —Double or Single sided operation
  - —Select or deselect ROM
  - —Module disable
- On-board header configures I/O for 8" or 5¼" drive interface
- Fully assembled, tested and warranted

ORDERING INFORMATION

Part No.	Description
RM65-5101E	Floppy Disk Controller (FDC) Module with on-board ROM*
RM65-5101NE	Floppy Disk Controller (FDC) Module without on-board ROM
A65-090	AIM 65 DOS 1.0 ROM**
A65/40-7090	AIM 65/40 DOS 1.0 ROM**
Order No.	**Description**
802	FDC Module User's Manual (included with RM65-5101E, RM65-5101NE, A65-090 and A65/40-7090)

*ROM contains FDC module primitive subroutines only.
**ROM contains FDC module primitive subroutines and operator selectable file management functions integrated with host computer I/O functions.

FUNCTIONAL DESCRIPTION

The Data Transceivers invert and transfer 8-bits of parallel data between the FDC module and the RM 65 bus, based on control signals from the Base Address Decoder and the Control Buffers. The read/write control line determines the direction, while the bus active enables the Data Transceivers.

The Address Buffers invert and transfer 12 of the 16 parallel address lines from the RM 65 bus to the Base Address Decoder, the Program ROM and the Floppy Disk Controller (FDC) device.

The Control Buffers invert and transfer phase 2 clock, reset, and read/write control signals from the RM 65 bus onto the module.

The Bank Select Control circuit detects when the module's assigned memory bank is addressed by comparing the bank address signal from the RM 65 bus to the Bank Select and Bank Select Enable switches. The Bank Select Enable switch assigns the module to be active in common memory (both Bank 0 and Bank 1) or only in the Bank set by the Bank Select switch (either Bank 0 or Bank 1).

The Interrupt and DMA Control circuit enables operation in either an interrupt driven mode or under DMA control. Both Interrupt generation and DMA requests can be disabled under program control. The DMA request is jumper selectable for either of two DMA request lines connected to the RM 65 bus.

The Base Address Decoder, with the Base Address Select PROM, the Bank Select Control circuit, the ROM Disable switch, and the phase 2 and read/write signals control device selection on the module. The Base Address Select PROM compares the eight most significant address lines to the programmed addresses to generate device select signals to the Program ROM and the I/O devices. The ROM Disable switch assigns the module to be active either in a 256 byte page (disabled) or in a 4K byte block (enabled). A separate Module Disable switch allows the entire module to be disabled.

When the ROM is disabled, only the I/O devices are active, in the 256 byte page that matches all eight Base Address Select bits. For the I/O devices, the three least significant address lines, along with the phase 2 clock and read/write control signals, drive register select lines to the FDC device, and device select lines to the Drive Status Buffer and Drive Control Register.

When the ROM is enabled, the module is active in the 4K byte block that matches the four most significant Base Address select bits. The program ROM is selected except when the address matches the four least significant Base Address Select bits, in which case the I/O device select lines are selected.

The Controller Clock derives a reference frequency for the FDC device from a crystal controlled oscillator. The frequency is 1 MHz or 2 MHz, depending on the Drive Configuration Header position.

The FDC device, in conjunction with the Data Separator and Precompensation Circuitry, interfaces the RM 65 bus to the Floppy Disk medium. The circuitry supports 5¼" or 8", single or double sided disk drives, with choice of single or double density, soft sector formats. The FDC features powerful commands, including single or multiple record read/write with selectable record lengths. Write precompensation circuitry ensures reliable data recovery in double density formats. The Precompensation jumper selects precompensation on all tracks, only on tracks 44 and greater, or no precompensation at all.

The Drive Configuration header selects the I/O connector and FDC circuitry for either 5¼" mini-floppy or 8" standard floppy disk formats. The 50-pin I/O receptacle connects the FDC module to a mass terminated cable connected to the installed disk drives. A 34-pin cable and mating connector can be used to connect the 5¼" mini-floppy drives while a 50-pin cable and mating connector is needed to connect to the 8" floppy drives.

The Drive Status Buffer allows detection of the Drive Configuration header and Single/Double Sided Drive jumper positions, as well as selected density and side information.

The Drive Control Register provides control of the side and drive selection, motor on, head load, double density, and interrupt disable. The Active Side 0 Level jumper allows the use of various drives without modification.

The Ready State Generator provides wait states as required by the FDC device.

The Program ROM contains primitive subroutines to support operations with up to four disk drives (single or double side, single or double density), including:

Format a Disk	Read or Write Multiple Sectors
Read or Write a Sector	Read or Write a Track
Seek or Verify Seek of a Track	Turn Motors On or Off
Restore the Head	Select or De-select any Drive

A user-provided program may call these subroutines to build an application dependent file-handling system.

OPTIONAL DISK OPERATING SYSTEM (DOS) FIRMWARE

Two optional ROMs are available that integrate the FDC primitive subroutines with operator selectable file management functions for operation on the AIM 65 and AIM 65/40 microcomputers. Either of these ROMs may be installed into the PROM/ROM socket on the FDC module to provide a firmware based Disk Operating System (DOS).

This version 1.0 ROM-based system offers the same convenience as the other AIM 65 and AIM 65/40 firmware in that it is immediately available for use through the Debug Monitor/Text Editor upon power turn-on. Mass storage operation may, therefore, proceed without waiting for loading of the DOS into RAM.

Text and program source code may be written to, and read from, disk with the Editor LIST (L) and READ (R) commands, respectively. Similarly, binary data and program object code may be written to, and loaded from, disk using the Monitor DUMP (D) and LOAD (L) commands, respectively. AIM 65 and AIM 65/40

Assembler and PL/65 files, both source and object code, are therefore supported. AIM 65 and AIM 65/40 BASIC programs may also be saved on, and loaded from disk.

The primary DOS commands are:

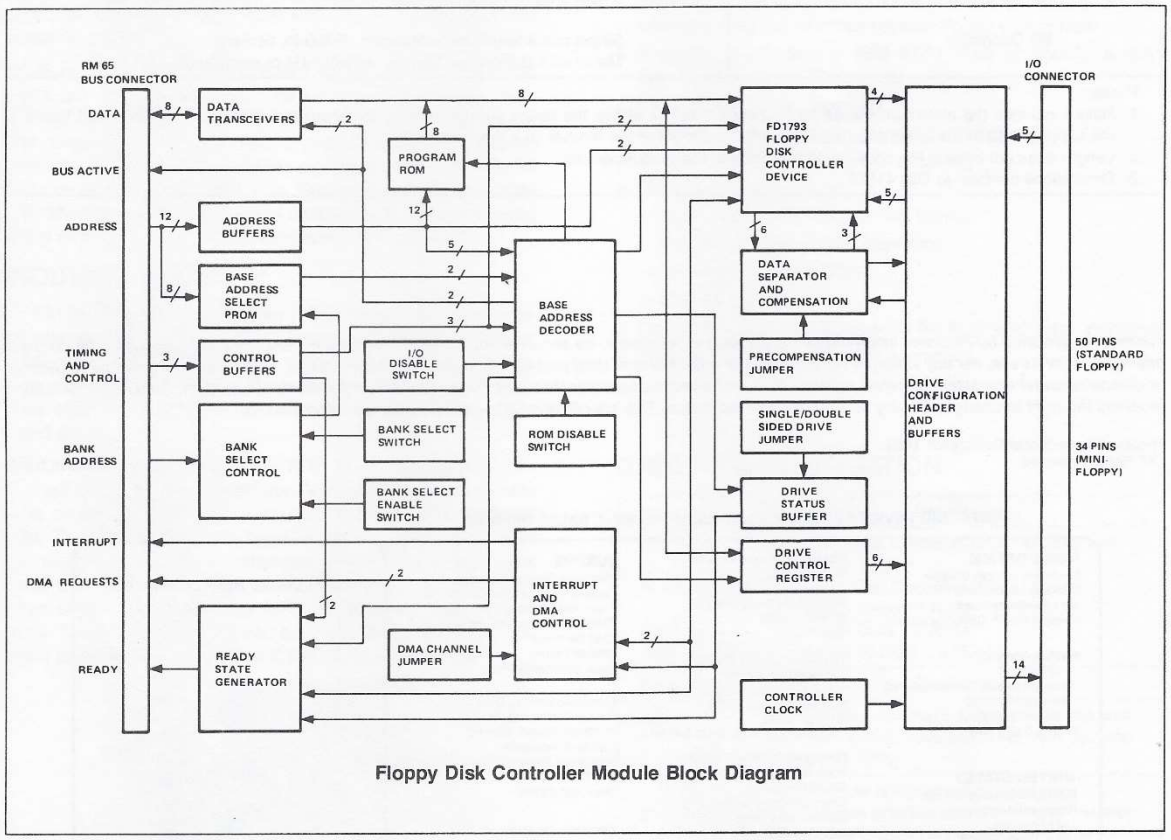
Format a Disk	Delete a File Name
List the Directory	Recover a File Name
List a File	Backup a Disk

Files are created automatically upon writing a file to disk. A file name (up to 10 characters in length) and the disk drive number (from 1 to 8) are operator entered in response to system prompts. (Double-sided drives are treated as two separate sides.)

The disk format function initializes a disk depending upon size, density and drive number. 5¼" and 8" disks are initialized to 35 and 77 tracks, respectively, however these values are user-alterable.

The contents of a file may be listed to another peripheral, including a file on another disk drive to allow copying of a file. All the active files on a disk may be copied to another disk using the backup function.

A file may be deleted (if active) to prevent it from being accessed or recovered (if deleted) to allow it to be accessed.



Floppy Disk Controller Module Block Diagram

RM 65 Bus Pin Assignments

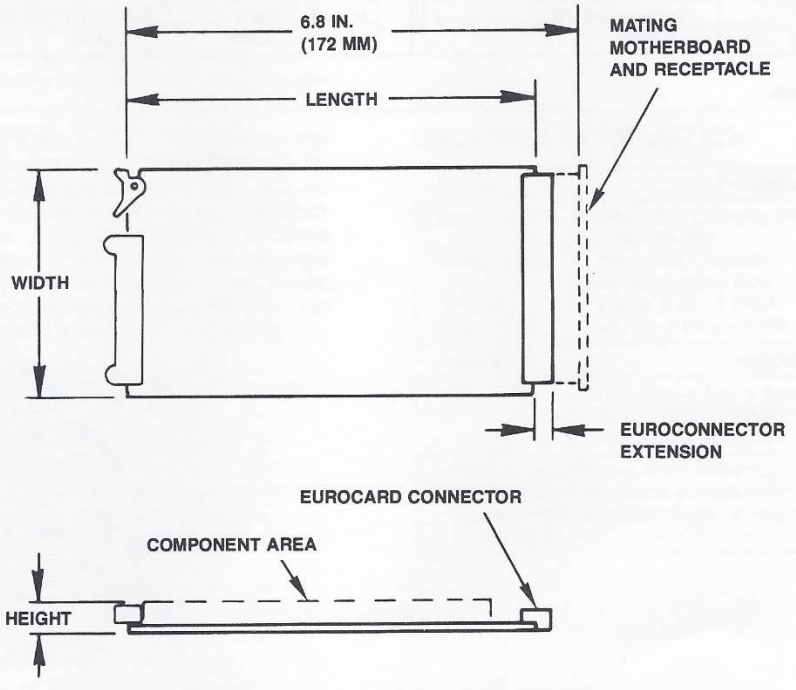
Bottom (Solder Side)			Top (Component Side)		
Pin	Signal Mnemonic	Signal Name	Pin	Signal Mnemonic	Signal Name
1a	GND	Ground	1c	+5V	+5 Vdc
2a	BADR/	Buffered Bank Address	2c	BA15/	Buffered Address Bit 15
3a	GND	Ground	3c	BA14/	Buffered Address Bit 14
4a	BA13/	Buffered Address Bit 13	4c	BA12/	Buffered Address Bit 12
5a	BA11/	Buffered Address Bit 11	5c	GND	Ground
6a	BA10/	Buffered Address Bit 10	6c	BA9/	Buffered Address Bit 9
7a	BA8/	Buffered Address Bit 8	7c	BA7/	Buffered Address Bit 7
8a	GND	Ground	8c	BA6/	Buffered Address Bit 6
9a	BA5/	Buffered Address Bit 5	9c	BA4/	Buffered Address Bit 4
10a	BA3/	Buffered Address Bit 3	10c	GND	Ground
11a	BA2/	Buffered Address Bit 2	11c	BA1/	Buffered Address Bit 1
12a	BA0/	Buffered Address Bit 0	12c	BØ1	*Buffered Phase 1 Clock
13a	GND	Ground	13c	BSYNC	*Buffered Sync
14a	BSO	*Buffered Set Overflow	14c	BDRQ1/	Buffered DMA Request 1
15a	BRDY	Buffered Ready	15c	GND	Ground
16a		*User Spare 1	16c	−12V/−V	*−12 Vdc/−V
17a	+12V/+V	+12 Vdc	17c		*User Spare 2
18a	GND	Ground Line	18c	BFLT/	*Buffered Bus Float
19a	BDMT/	*Buffered DMA Terminate	19c	BØ0	*Buffered External Phase 0 Clock
20a		*User Spare 3	20c	GND	Ground
21a	BR/$\overline{W}$/	Buffered Read/Write "Not"	21c	BDRQ2/	Buffered DMA Request 2
22a		*System Spare	22c	BR/$\overline{W}$	*Buffered Read/Write
23a	GND	Ground	23c	BACT/	Buffered Bus Active
24a	BIRQ/	Buffered Interrupt Request	24c	BNMI/	*Buffered Non-Maskable Interrupt
25a	BØ2/	Buffered Phase 2 "Not" Clock	25c	GND	Ground
26a	BØ2	*Buffered Phase 2 Clock	26c	BRES/	Buffered Reset
27a	BD7/	Buffered Data Bit 7	27c	BD6/	Buffered Data Bit 6
28a	GND	Ground	28c	BD5/	Buffered Data Bit 5
29a	BD4/	Buffered Data Bit 4	29c	BD3/	Buffered Data Bit 3
30a	BD2/	Buffered Data Bit 2	30c	GND	Ground
31a	BD1/	Buffered Data Bit 1	31c	BD0/	Buffered Data Bit 0
32a	+5V	+5 Vdc	32c	GND	Ground

Note:
*Not used on this module.

I/O Connector Pin Assignments

FDC Module I/O Connector Pin	Standard Floppy Disk Drive Interface Cable Connector		Mini-Floppy Disk Drive Interface Cable Connector (2)	
	Pin	Signal Name	Pin	Signal Name
2	2	Track > 43 (Remex & MFE or equivalents)		
4	4	N.C.		
6	6	N.C.		
8	8	Track > 43 (Caldisk or equivalents)		
10	10	N.C.		
12	12	N.C.		
14	14	2nd Side Select		
16	16	N.C.		
18	18	Head Load	2	N.C.
20	20	Index	4	N.C.
22	22	Drive Ready	6	Drive Select #4
24	24	N.C.	8	Index
26	26	Drive Select #1	10	Drive Select #1
28	28	Drive Select #2	12	Drive Select #2
30	30	Drive Select #3	14	Drive Select #3
32	32	Drive Select #4	16	Motor On
34	34	Direction In	18	Direction In
36	36	Step Pulse	20	Step Pulse
38	38	Write Data	22	Write Data
40	40	Write Gate	24	Write Gate
42	42	Track Zero	26	Track Zero
44	44	Write Protected	28	Write Protected
46	46	Read Data	30	Read Data
48	48	N.C.	32	2nd Side Select
50	50	N.C.	34	N.C.

Notes:
1. All odd numbered pins are GND.
2. Pin 1 of the 34-pin mini-floppy disk drive interface cable connector should be keyed to pin 17 of the FDC module I/O connector.



Floppy Disk Controller Module Dimensions

SPECIFICATIONS

Parameter	Value
Dimensions (1, 2, 3) Width Length Height	 3.9 in. (100 mm) 6.3 in. (160 mm) 0.56 in. (14 mm)
Weight	5.2 oz. (145 g)
Environment Operating Temperature Storage Temperature Relative Humidity	 0°C to 70°C −40°C to +85°C 0% to 85% (Without condensation)
Power Requirements	+5 Vdc ±5% @ 600 mA—Typical 900 mA—Maximum +12 Vdc ±5% @ 60 mA—Typical 100 mA—Maximum
Interfaces RM 65 Bus Interface I/O Connector	 64-pin plug (0.100 in. centers) per DIN 41612 (Row b not installed) 50-pin mass terminated connector (0.100 in. centers) Mates with I&B/Ansley Part No. 609-5001M or equivalent

Notes:
1. Height includes the maximum values for component height above the board surface (0.4 in. for populated modules), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.).
2. Length does not include the added extension due to the module ejector.
3. Dimensions conform to DIN 41612.

Printed in U.S.A.

ELECTRONIC DEVICES DIVISION REGIONAL ROCKWELL SALES OFFICES

HOME OFFICE
Electronic Devices Division
Rockwell International
4311 Jamboree Road
Newport Beach, California 92660

Mailing Address:
P.O. Box C
Newport Beach, California 92660
Mail Code 501-300
Tel: 714-833-4700
TWX: 910 591-1698

UNITED STATES
Electronic Devices Division
Rockwell International
1842 Reynolds
Irvine, California 92714
(714) 833-4655
ESL 62108710
TWX: 910 595-2518

Electronic Devices Division
Rockwell International
921 Bowser Road
Richardson, Texas 75080
(214) 996-6500
Telex: 73-307

Electronic Devices Division
Rockwell International
10700 West Higgins Rd., Suite 102
Rosemont, Illinois 60018
(312) 297-8862
TWX: 910 233-0179 (RI MED ROSM)

Electronic Devices Division
Rockwell International
5001B Greentree
Executive Campus, Rt. 73
Marlton, New Jersey 08053
(609) 596-0090
TWX: 710 940-1377

FAR EAST
Electronic Devices Division
Rockwell International Overseas Corp.
Itohpia Hirakawa-cho Bldg.
7-6, 2-chome, Hirakawa-cho
Chiyoda-ku, Tokyo 102, Japan
(03) 265-8806
Telex: J22198

EUROPE
Electronic Devices Division
Rockwell International GmbH
Fraunhoferstrasse 11
D-8033 Munchen-Martinsried
West Germany
(089) 857-6016
Telex: 0521/2650 rimd d

Electronic Devices Division
Rockwell International
Heathrow House, Bath Rd.
Cranford, Hounslow,
Middlesex, England
(01) 759-9911
Telex: 851-25463

Electronic Devices
Rockwell Collins
Via Boccaccio, 23
20123 Milano, Italy
498.74.79
Telex: 202/82

YOUR LOCAL REPRESENTATIVE

10/82