Rockwell

RM65-3132E
RM 65 32K DYNAMIC RAM MODULE

RM 65 MICROCOMPUTER MODULES

The RM65-3132E 32K Dynamic RAM Module is one of the hardware options available for the RM 65 Microcomputer Module Family.

RM 65 Microcomputer Module products are designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

RM 65 module products use a motherboard interconnect concept and accept any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A selection of card cages provides packaging flexibility. RM 65 products may also be used with Rockwell AIM 65 and AIM 65/40 Microcomputers for product development and for a broad variety of portable or desktop microcomputer applications.

PRODUCT OVERVIEW

The 32K Dynamic RAM module provides 32K bytes of read/write memory using 16 16K bit × 1 dynamic RAM (DRAM) devices. Two bank select switches allow the board to be dedicated to either one of two 65K Banks, or to be assigned common to both banks. A 24-pin DIP header allows each of the eight 4K sections to be independently mapped into any 4K block of the selected 65K bank. The independent addressing of blocks provide flexibility with system memory maps. An on-board switch allows the entire board to be write-protected.

All refreshing of the dynamic RAM chips is automatic and completely transparent to the RM 65 Bus, thus providing low power performance at no loss of bus speed.

FEATURES

- Compact size—about 4″ × 6¼″ (100 mm × 160 mm)
- Pin and socket bus connection
- RM 65 bus compatible
- Buffered data, address, and control lines
- Internal Refresh controller is completely transparent to the RM 65 bus
- On-board switch allows write protection
- Base Address Header allows each 4K memory section to be assigned to any 4K block as a selected bank
- Bank select switches allow the entire board to be mapped into either or both 65K banks
- On-board DC-DC converter for −5 volt power supply
- Requires +5 and +12 volt power from the RM 65 bus
- Fully assembled, tested, and warranted.

ORDERING INFORMATION

Part No.	Description
RM65-3132E	32K Dynamic RAM Module
RM65-3132NE	32K Dynamic RAM Module (without RAM devices installed)

Order No.	Description
808	32K Dynamic RAM Module User's Manual (included with RM65-3132E and RM65-3132NE)
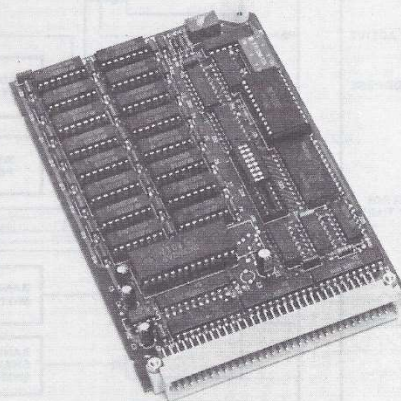
RM65-3132E 32K Dynamic RAM Module

FUNCTIONAL DESCRIPTION

The Data Transceivers invert and transfer 8-bit parallel data between the selected DRAMs to the RM 65 bus. During a read operation, data from the DRAMs are latched and driven by the transceivers onto the RM 65 bus. During a write operation, data from the RM 65 bus drives the DRAMs. The transceivers are disabled when the module is not addressed.

The Address Buffers invert and transfer 16-bit parallel address lines from the RM 65 bus into the DRAM Module.

The Bank Select Control circuit detects when the DRAM module's assigned memory bank is addressed by comparing the bank address signal from the RM 65 bus to the Bank Select and Bank Select Enable switches. The Bank Select Enable switch allows the board to reside in common memory (both Bank 0 and Bank 1) or only in the Bank set by the Bank Select switch (either Bank 0 or Bank 1).

The Control Buffers buffer the control and timing signals used from the RM 65 bus.

The DRAM devices require 3 voltages. Two of these (+5 and +12 volts) are available directly from the RM 65 bus. The third voltage (−5 volts) is generated on board with a DC/DC converter.

The Address Decoder uses the four MSB address lines to decode and enable one of 16 lines, each of which correspond to 4K blocks. The Base Address Selection Jumpers are placed in a 28 pin socket which consists of 16 lines from the Address Decoder, four lines from +5 volts, and 8 lines to the Base Address Encoder. The Base Address Selection is made by connecting each of the eight encoder inputs to any one of the 16 decoder outputs or to +5 volts. This allows each 4K block to be addressed anywhere in the selected 65K memory bank or dis-

abled. The Base Address Encoder produces a 3 bit code for the enabled line and an additional signal for any line active (Board Select). The 3 bit code from the encoder becomes the 3 MSB address bits for the Memory Address Multiplexer. The Board Select line and a valid Bank Select signal are used to enable the Memory Controller and Data Transceivers, as well as create a Data Bus Active Signal.

The Write Control logic uses the Write Protect switch and the Read/Write line to enable writing into the DRAMs. If the Write Protect switch is off, the Read/Write signal is transferred directly to the Memory Controller. If the Write Protect switch is on, the Memory Controller forces a read operation so that the contents of the DRAMs will not be altered.

The Timing Control generates all the clocks required by the Memory Controller, Memory Address Multiplexer, and the Refresh Clock. The Refresh Clock generates a refresh cycle for every seven RM 65 clock cycles.

The Memory Controller uses the clocks derived in the timing control to sequence the signals to the DRAM devices. During normal read or write cycles, the Memory Controller allows Row Address, then Column Address information to be applied to the addressed DRAMs and generates the read/write signal. When a refresh is required, the timing is controlled so that the refresh is transparent to the RM 65 bus.

The Memory Address Multiplexer and Refresh Counter multiplexes Row, Column, or Refresh Addresses onto the DRAM address lines in response to the Memory Controller. There is also a Refresh Counter which is incremented by the Refresh Clock.
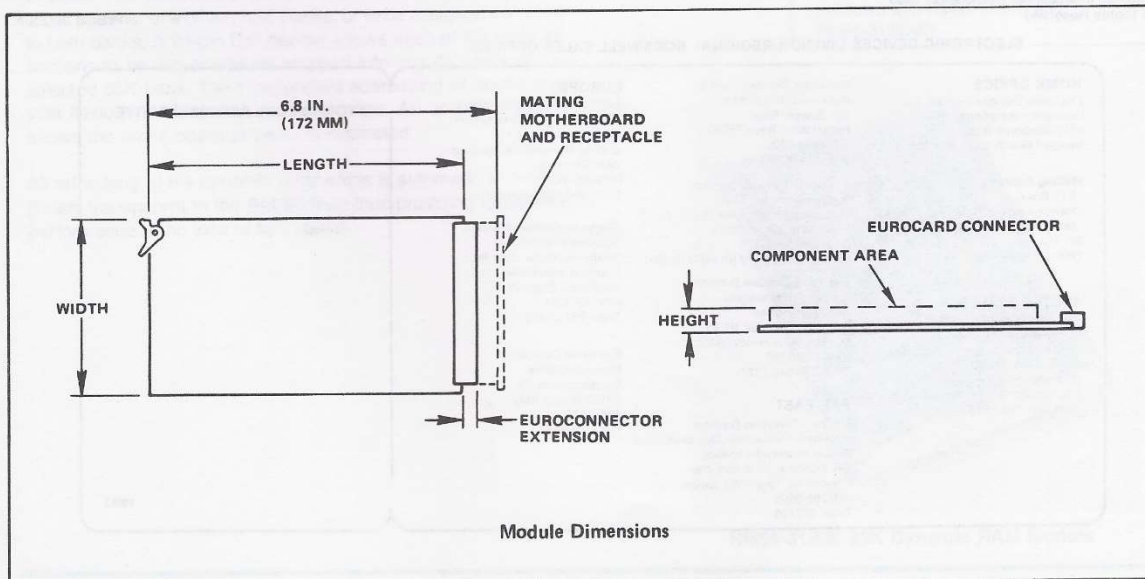

32K Dynamic RAM Module Block Diagram
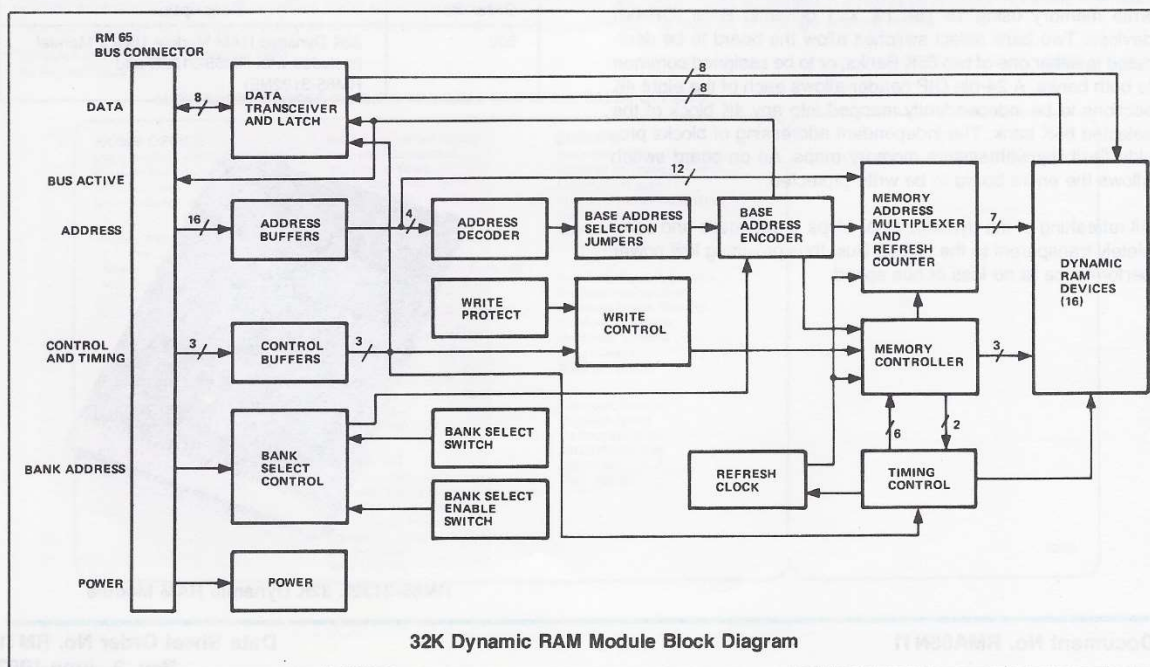
RM 65 Bus Pin Assignments

Bottom (Solder Side)			Top (Component Side)		
Pin	Signal Mnemonic	Signal Name	Pin	Signal Mnemonic	Signal Name
1a	GND	Ground	1c	+5V	+5 Vdc
2a	BADR/	Buffered Bank Address	2c	BA15/	Buffered Address Bit 15
3a	GND	Ground	3c	BA14/	Buffered Address Bit 14
4a	BA13/	Buffered Address Bit 13	4c	BA12/	Buffered Address Bit 12
5a	BA11/	Buffered Address Bit 11	5c	GND	Ground
6a	BA10/	Buffered Address Bit 10	6c	BA9/	Buffered Address Bit 9
7a	BA8/	Buffered Address Bit 8	7c	BA7/	Buffered Address Bit 7
8a	GND	Ground	8c	BA6/	Buffered Address Bit 6
9a	BA5/	Buffered Address Bit 5	9c	BA4/	Buffered Address Bit 4
10a	BA3/	Buffered Address Bit 3	10c	GND	Ground
11a	BA2/	Buffered Address Bit 2	11c	BA1/	Buffered Address Bit 1
12a	BA0/	Buffered Address Bit 0	12c	BØ1	*Buffered Phase 1 Clock
13a	GND	Ground	13c	BSYNC	*Buffered Sync
14a	BSO	*Buffered Set Overflow	14c	BDRQ1/	*Buffered DMA Request 1
15a	BRDY	*Buffered Ready	15c	GND	Ground
16a		*User Spare 1	16c	−12V/−V	*−12 Vdc/−V
17a	+12V/+V	+12 Vdc/+V	17c		*User Spare 2
18a	GND	Ground Line	18c	BFLT/	*Buffered Bus Float
19a	BDMT/	*Buffered DMA Terminate	19c	BØ0	*Buffered External Phase 0 Clock
20a		*User Spare 3	20c	GND	Ground
21a	BR/W̄/	Buffered Read/Write "Not"	21c	BDRQ2/	*Buffered DMA Request 2
22a		*System Spare	22c	BR/W̄	Buffered Read/Write
23a	GND	Ground	23c	BACT/	Buffered Bus Active
24a	BIRQ/	*Buffered Interrupt Request	24c	BNMI/	*Buffered Non-Maskable Interrupt
25a	BØ2/	Buffered Phase 2 "Not" Clock	25c	GND	Ground
26a	BØ2	*Buffered Phase 2 Clock	26c	BRES/	*Buffered Reset
27a	BD7/	Buffered Data Bit 7	27c	BD6/	Buffered Data Bit 6
28a	GND	Ground	28c	BD5/	Buffered Data Bit 5
29a	BD4/	Buffered Data Bit 4	29c	BD3/	Buffered Data Bit 3
30a	BD2/	Buffered Data Bit 2	30c	GND	Ground
31a	BD1/	Buffered Data Bit 1	31c	BD0/	Buffered Data Bit 0
32a	+5V	+5 Vdc	32c	GND	Ground

Note:
*Not used on this module.

Module Dimensions

6.8 IN. (172 MM)

LENGTH

MATING MOTHERBOARD AND RECEPTACLE

WIDTH

EUROCARD CONNECTOR

COMPONENT AREA

HEIGHT

EUROCONNECTOR EXTENSION

SPECIFICATIONS

Parameter	Value
Dimensions (1, 2, 3) Width Length Height	3.9 in. (100 mm) 6.3 in. (160 mm) 0.56 in. (14 mm)
Weight	4.5 oz. (140 g)
Environment Operating Temperature Storage Temperature Relative Humidity	0°C to 70°C −40°C to +85°C 0% to 85% (without condensation)
Power Requirements	+5 Vdc ±5% 1.4 A (7.0 W)—Maximum +12 Vdc ±5% 170 mA (2.1W)—Maximum
RM 65 Bus Interface	64-pin plug (0.100 in. centers) per DIN 41612 (Row b not installed)

Notes:
1. Height includes the maximum values for component height above the board surface (0.4 in. for populated modules), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.).
2. Length does not include extensions beyond the edge of the module due to connectors or the module ejector.
3. Dimensions conform to DIN 41612.

Information furnished by Rockwell International Corporation is believed to be accurate and reliable. However, no responsibility is assumed by Rockwell International for its use, nor any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Rockwell International other than for circuitry embodied in a Rockwell product. Rockwell International reserves the right to change circuitry at any time without notice. This specification is subject to change without notice.

Printed in U.S.A.

ELECTRONIC DEVICES DIVISION REGIONAL ROCKWELL SALES OFFICES