Rockwell

R6565
DOUBLE-DENSITY FLOPPY DISK CONTROLLER (DDFDC)

PRELIMINARY

DESCRIPTION

The R6565 Double-Density Floppy Disk Controller (DDFDC) interfaces up to four floppy disk drives to a 6500/6800 microprocessor-based system. The DDFDC simplifies the system design by minimizing both the number of external hardware components and software steps needed to implement the floppy disk drive (FDD) interface. Control signals supplied by the DDFDC reduce the number of components required in external phase locked loop and write precompensation circuitry. Memory-mapped registers containing commands, status and data simplify the software interface. Built-in functions reduce the software overhead needed to control the FDD interface. The DDFDC supports both the IBM 3740 Single-Density (FM) and IBM System 34 Double-Density (MFM) formats.

The DDFDC interfaces directly to the 6500/6800 synchronous microprocessor bus and operates with 8-bit byte length data transferred on the bus. The DDFDC will operate in either DMA or non-DMA mode. In DMA mode, the CPU need only load the command into the DDFDC and all data transfers occur under DMA control. The R6565 is directly compatible with the MC6844 Direct Memory Access Controller (DMAC). In non-DMA mode, the DDFDC generates an interrupt to the CPU indicating that a byte of data is available.

Controller commands, command or device status, and data are transferred between the DDFDC and the CPU via six internal registers. The Main Status Register (MSR) stores the DDFDC status information while four additional status registers provide result information to the CPU following each controller command. The Data Register (DR) stores actual disk data, parameters, controller commands and FDD status information for use by the CPU.

The R6565 executes 15 separate multi-byte commands:

Read Data	Specify
Write Data	Format a Track
Read Deleted Data	Scan Equal
Write Deleted Data	Scan High or Equal
Read a Track	Scan Low or Equal
Read ID	Sense Interrupt Status
Seek	Sense Drive Status
Recalibrate (Restore to Track 0)	

FEATURES

- Address mark detection circuitry
- Software control of
  —Track stepping rate
  —Head load time
  —Head unload time
- IBM compatible in both single- and double-density recording formats
- Programmable data record lengths: 128, 256, 512, 1024, 2048, 4096 or 8192 bytes/sector
- Multi-sector and multi-track transfer capability
- Controls up to four floppy disk drives
- Data scan capability—will scan a single sector or an entire track of data fields, comparing on a byte-by-byte basis data in the processor's memory with data read from the disk
- Data transfers in DMA or non-DMA mode
- Parallel seek operations on up to four drives
- Directly compatible with 6500 and 6800 synchronous microprocessor bus
- Single phase 8 MHz Clock
- Single +5 Volt Power Supply

ORDERING INFORMATION

Part Number	CLK Frequency	Temperature Range
R6565	8 MHz	0°C to 70°C

Package:
C = Ceramic
P = Plastic

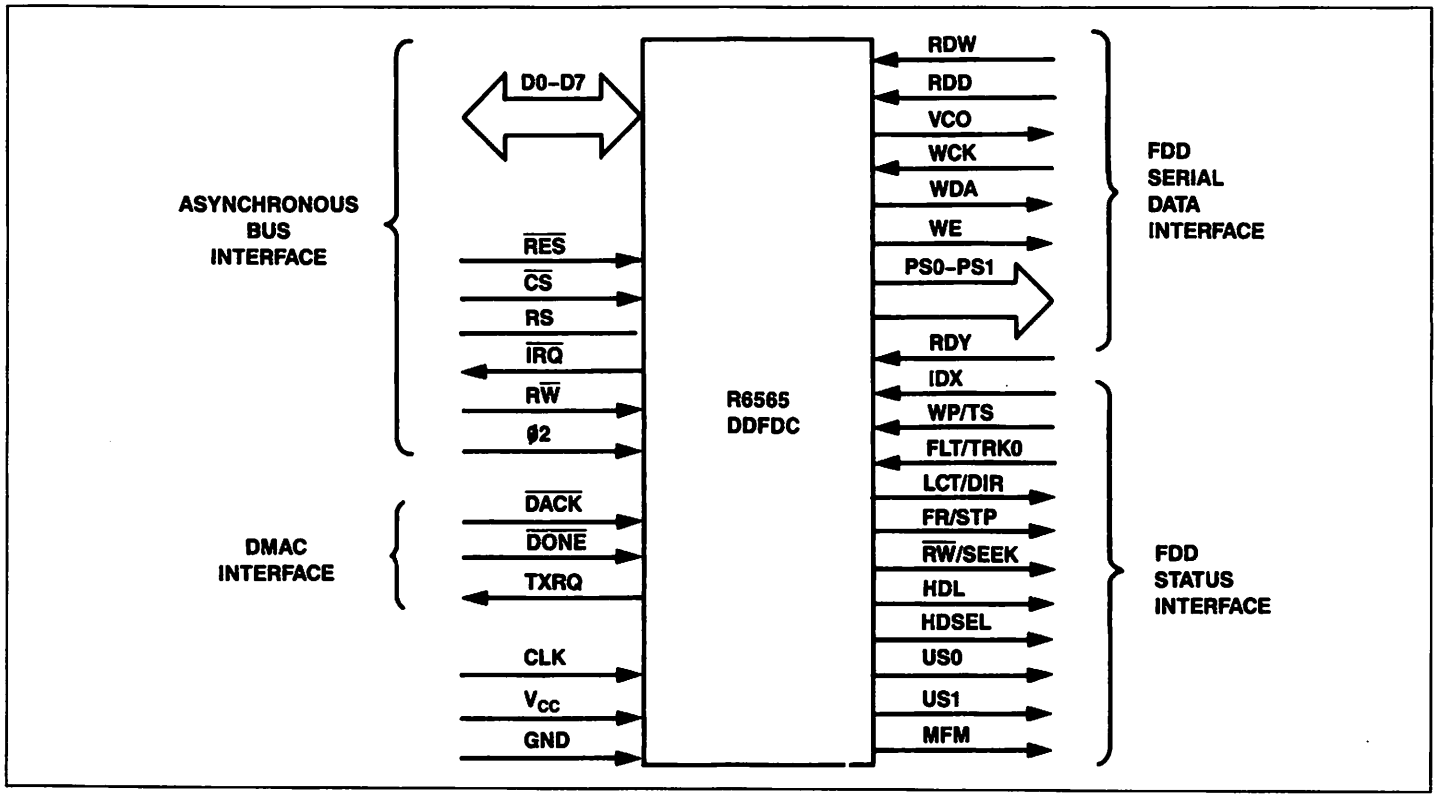


Figure 1. DDFDC Input and Output Signals

PIN DESCRIPTION

Throughout this document signals are presented using the terms active and inactive, or asserted and negated, independent of whether the signal is active in the high-voltage state or low-voltage state. (The active state of each logic pin is described below.) Active low signals are denoted by a superscript bar.

BUS INTERFACE

D0-D7—Data Lines. The bidirectional data lines transfer data between the DDFDC and the 8-bit data bus.

CLK—CLOCK. The clock is a TTL compatible 8 MHz square wave signal.

$\overline{RES}$—RESET. This active low input places the DDFDC in the idle state and resets the output lines to the floppy disk drive (FDD) to the low state.

$\overline{CS}$—Chip Select. The DDFDC is selected when the $\overline{CS}$ input is low.

RS—Data/Status Register Select. This input selects the Data or Status Register for reading from or writing to. When RS = high, the Data Register is selected and the state of R/$\overline{W}$ determines determines whether it is a read (R/$\overline{W}$ = high) or a write (R/$\overline{W}$ = low) operation. When RS = low, the Status Register is selected. This register may only be read (R/$\overline{W}$ = high); the state R/$\overline{W}$ = low is invalid when the Status Register is selected.

$\overline{IRQ}$—Interrupt Request. This active low output is the interrupt request generated by the DDFDC to the CPU.

R/$\overline{W}$—Read/Write. This input defines the data bus transfer as a read or write cycle. When high (read), the data transfer is from the DDFDC to the data bus. When low (write), the data transfer is from the data bus to the DDFDC.

Ø2—Enable. This input is the synchronous handshake line for the information transfer on the R6500 processor bus. This input signal is the standard enable signal commonly called Ø2 in R6500 peripheral devices or Enable in 6800 peripheral devices.

DIRECT MEMORY ACCESS CONTROLLER (DMAC) INTERFACE

$\overline{DACK}$—DMA Acknowledge. The DMA transfer acknowledge signal is a TTL compatible input generated by the DMA controller (DMAC) controlling the DDFDC. The DMA cycle is active when $\overline{DACK}$ is low and the DDFDC is performing a DMA transfer.

TXRQ—DMA Request. The transfer request signal is a TTL compatible output generated by the DDFDC to request a data transfer operation under control of the DMAC (in the DMA mode). The request is active when TXRQ = high. The signal is reset inactive when DMA Acknowledge ($\overline{DACK}$) is asserted (low).

$\overline{DONE}$—DMA Transfer Complete. This input signal is issued to the DDFDC when the DMA transfer for a channel is complete. The signal is active low concurrent with the $\overline{DACK}$ input when the DMA operation is complete as a result of that transfer.

FDD SERIAL DATA INTERFACE

RDD—Read Data. Read Data input from the floppy disk drive (FDD) containing clock and data bits.

RDW—Read Data Window. Data Window input generated by the Phase Locked Loop (PLL) and used to sample data from the FDD.

VCO—Variable Frequency Oscillator Sync. This output signal inhibits the VCO in the PLL circuit when low and enables the VCO in the PLL circuit when high. This inhibits RDD and RDW from being generated until valid data is detected from the FDD.

WCK—Write Clock. This input clock determines the Write Data rate to the FDD. The data rate is 500 KHz in the FM mode (MFM = low) and 1 MHz in the MFM mode (MFM = high). The pulse width is 250 ns (typical) in both modes.

WDA—Write Data. Serial write data output to the FDD containing both clock and data bits.

WE—Write Enable. This output signal enables the Write Data into the FDD when high.

PS0-PS1—Preshift. These outputs are encoded to convey write compensation status during the MFM mode to determine early, late or normal times as follows:

Write Precompensation Status	Preshift Outputs	
	PS0	PS1
Normal	0	0
Late	0	1
Early	1	0
Invalid	1	1
0 = Low, 1 = High		

FDD STATUS INTERFACE

RDY—Ready. An active high input signal indicates the FDD is ready to send data to, or receive data from, the DDFDC.

IDX—Index. An active high input signal from the FDD indicates the index hole is under the index sensor. Index is used to synchronize DDFDC timing.

$\overline{RW}$/SEEK—Read Write/Seek. Mode selection signal to the FDD which controls the multiplexer from the multiplexed signals. When $\overline{RW}$/SEEK is low, the Read/Write mode is commanded; when $\overline{RW}$/SEEK is high, the Seek mode is commanded.

$\overline{RW}$/SEEK	Mode	Active FDD Interface Signals
Low	Read/Write	WP, FLT, LCT, FR
High	Seek	TS, TRK0, DIR, STP

WP/TS—Write Protect/Two Side. An active high multiplexed input signal from the FDD. In the Read/Write mode, WP/TS high indicates the media is write-protected. In the Seek mode, WP/TS high indicates the media is two-sided.

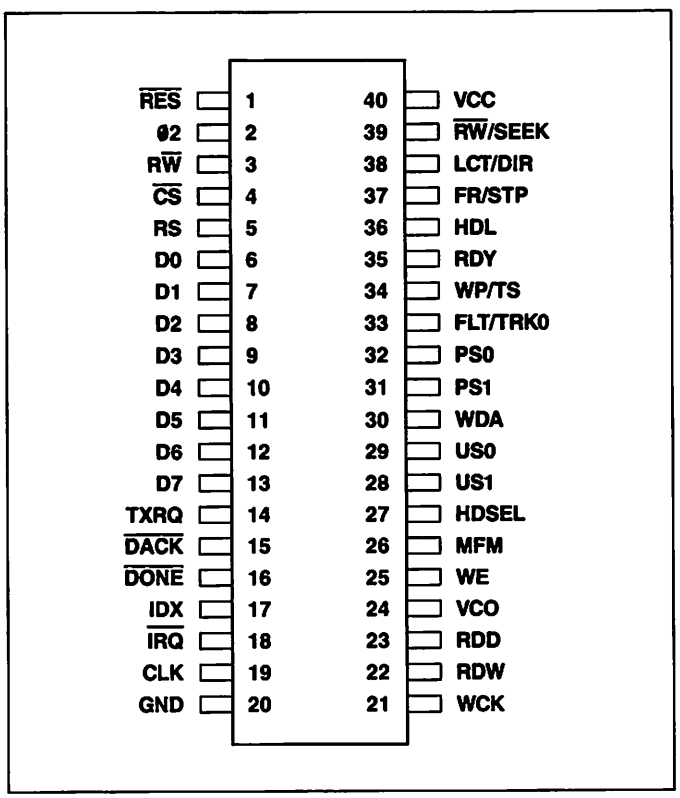
FLT/TRK0—Fault/Track Zero. An active high multiplexed input from the FDD. In the Read/Write mode ($\overline{RW}$/SEEK = low), FLT/TRK0 high indicates an FDD fault. In the Seek mode, FLT/TRK0 high indicates that the read/write head is positioned over track zero.

LCT/DIR—Low Current/Direction. A multiplexed output to the FDD. In the Read/Write mode, LCT/DIR is low when the read/write head is to be positioned over the inner tracks and the LCT/DIR is high when the head is to be positioned over the outer tracks. In the Seek mode, LCT/DIR controls the head direction. When LCT/DIR is high, the head steps to the outside of the disk; when LCT/DIR is low, the head steps to the inside of the disk.

FR/STP—Fault Reset/Step. A multiplexed output to the FDD. In the Read/Write mode, FR/STP high resets the fault indicator in the FDD. An FR pulse is issued at the beginning of each read or write command prior to issuing HDL. In the Seek mode, FR/STP provides the step pulses to move the read/write head to another track in the direction indicated by the LCT/DIR signal.

HDL—Head Load. An active high output to notify the FDD that the read/write head should be loaded (placed in contact with the media). A low level indicates the head should be unloaded.

HD—Head Select. An output to the FDD to select the proper read/write head. Head One is selected when HD = high and Head Zero is selected when HD = low.



R6565 DDFDC Pin Diagram

US0-US1—Unit Select. Output signals for floppy disk drive selection as follows:

Unit Select		Floppy Disk Drive Select
US0	US1	
0	0	0
0	1	1
1	0	2
1	1	3
0 = Low, 1 = High		

MFM—MFM Mode. Output signal to the FDD to indicate MFM or FM mode. Selects the MFM mode when MFM = high and the FM mode when MFM = low.

VCC—Power. +5V dc.

GND—Ground (V_{SS}).

DDFDC REGISTERS

The DDFDC contains six registers which may be accessed by the processor or DMA controller via the system (i.e., microprocessor) bus: a Main Status Register, a Data Register, and four Result Status Registers. The 8-bit Main Status Register (MSR) contains the status information of the DDFDC, and may be accessed at any time. The 8-bit Data Register, consisting of several registers in a stack with only one register presented to the data bus at a time, stores data, commands, parameters and FDD status information. Bytes of data are read out of, or written into, the Data Register in order to initiate a command or to obtain the results of a command execution.

The read-only Main Status Register facilitates the transfer of data between the system and the DDFDC. The other Status Registers (ST0, ST1, ST2 and ST3) are only available during the result phase, and may be read only after completing a command. The particular command which has been executed determines how many of the Status Registers will be read.

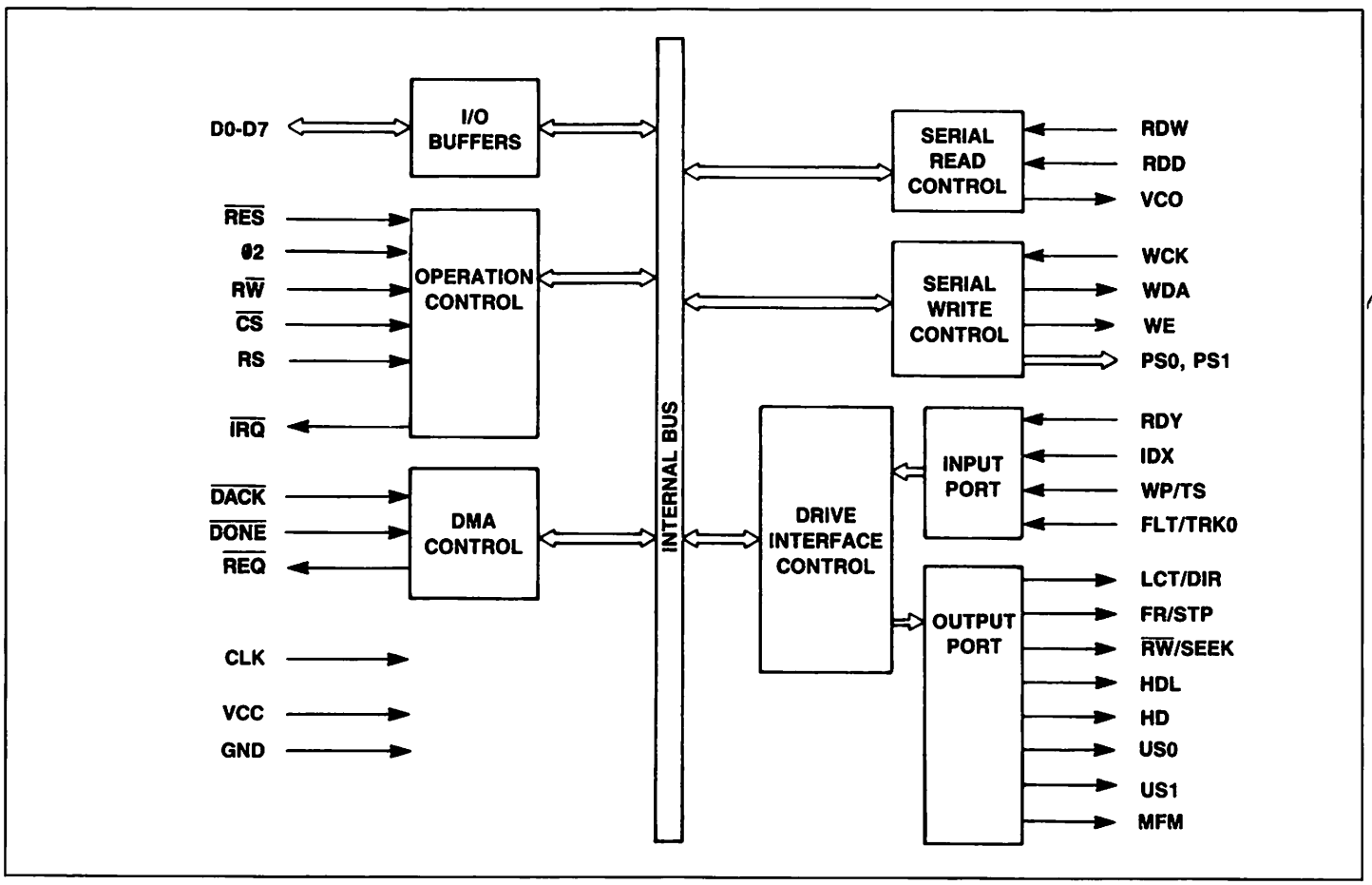


Figure 2. DDFDC Block Diagram

The relationship between the status/data registers and the R/$\overline{W}$ and RS signals is shown below.

RS	R/$\overline{W}$	Function
0	1	Read Main Status Register
0	0	Illegal
1	1	Read from Data Register
1	0	Write into Data Register
0 = Low, 1 = High		

Table 1 shows each of the status registers used by the DDFDC and each bit assignment within the individual registers. Table 2 defines the symbols used throughout the command definitions. Each register bit symbol is defined in the register descriptions that follow Table 2.

REGISTER DEFINITIONS

Main Status Register (MSR)

7	6	5	4	3	2	1	0
RQM	DIO	EXM	CB	D3B	D2B	D1B	D0B

The Main Status Register (MSR) contains the status information of the DDFDC, and must be read by the processor before each byte is written to, or read from, the Data Register during the command or result phase. MSR reads are not required during the execution phase. The Data Input/Output (DIO) and Request for Master (RQM) bits in the MSR indicate when data is ready and in which direction data will be transferred on the data bus. The maximum time between the last R/$\overline{W}$ during command or result phases and the DIO and RQM getting set or reset is 12 μs. For this reason, every time the MSR is read the processor should wait 12 μs. The maximum time from the end of the last read in the result phase to when bit 4 (DDFDC Busy) goes low is also 12 μs.

The DIO and RQM timing chart is shown in Figure 3.

MSR
7 RQM —Request for Master.
0 Data Register is not ready.
1 Data Register is ready.

MSR
6 DIO —Data Input/Output.
0 Data transfer is from system to the Data Register.
1 Data transfer is from Data Register to the system.

MSR
5 EXM —Execution Mode. (Non-DMA mode only).
0 Execution phase ended, result phase begun.
1 Execution phase started.

MSR
4 CB —Controller (DDFDC) Busy.
0 DDFDC is not busy, will accept a command.
1 DDFDC is busy, will not accept a command.

MSR
3 D3B —Floppy Disk Drive (FDD) 3 Busy.
0 FDD 3 is not busy, DDFDC will accept read or write command.
1 FDD 3 is busy, DDFDC will not accept read or write command.

MSR
2 D2B —FDD 2 Busy.
0 FDD 2 is not busy, DDFDC will accept read or write command.
1 FDD 2 is busy, DDFDC will not accept read or write command.

MSR
1 D1B —FDD 1 Busy.
0 FDD 1 is not busy, DDFDC will accept read or write command.
1 FDD 1 is busy, DDFDC will not accept read or write command.

MSR
0 D0B —FDD 0 Busy.
0 FDD 0 is not busy, DDFDC will accept read or write command.
1 FDD 0 is busy, DDFDC will not accept read or write command.

Status Register 0 (ST0)

7	6	5	4	3	2	1	0
IC		SE	EC	NR	HD	US	
						US1	US0

The Status Register 0 (ST0) as well as the other status registers (ST1-ST3), are available only during the result phase, and may be read only after completing a command. The particular command executed determines which status registers are used and may be read.

ST0
7 6 IC —Interrupt Code.
0 0 Normal Termination (NT). Command was properly executed and completed.
0 1 Abnormal Termination (AT). Command execution was started, but was not successfully completed.
1 0 Invalid Command (IC). Received command was invalid.
1 1 Abnormal Termination (AT). The Ready (RDY) signal from the FDD changed state during command execution.

ST0
5 SE —Seek End.
0 Seek command is not completed.
1 Seek command completed by DDFDC.

ST0
4 EC —Equipment Check.
0 No error.
1 Either a fault signal is received from the FDD or the track 0 signal failed to occur after 256 step pulses (Recalibrate Command).

Table 1. DDFDC Status Register Bit Assignments

	Bit Number							
	7	6	5	4	3	2	1	0
Main Status Register (MSR)	RQM	DIO	EXM	CB	D3B	D2B	D1B	D0B
Status Register 0 (ST0)	IC		SE	EC	NR	HD	US	
							US1	US0
Status Register 1 (ST1)	EN	0	DE	OR	0	ND	NW	MA
Status Register 2 (ST2)	0	CM	DD	WT	SH	SN	BT	MD
Status Register 3 (ST3)	FLT	WP	RDY	TRK0	TS	HD	US1	US0

Table 2. Command Symbol Description

Symbol	Name	Description
D	Data	The data pattern which is going to be written into a sector.
D0-D7	Data Bus	8-bit data bus, where D0 is the least significant data line and D7 is the most significant data line.
DTL	Data Length	When N is defined as 00, DTL is the number of data bytes to read from or write into the sector.
EOT	End of Track	The final sector number on a track. During read or write operation, the DDFDC stops data transfer after reading from or writing to the sector equal to EOT.
GPL	Gap Length	The length of Gap 3. During read/write commands this value determines the number of bytes that the VCO will stay low after two CRC bytes. During the Format a Track command it determines the size of Gap 3.
H	Head Address	Head number 0 or 1, as specified in ID field.
HD (H)	Head	A selected head number 0 or 1 which controls the polarity of pin 27. (H = HD in all command words).
HLT	Head Load Time	The head load time in the FDD (2 to 254 ms in 2 ms increments).
HUT	Head Unload Time	The head unload time after a read or write operation has occurred (16 to 240 ms in 16 ms increments).
MF	FM or MFM Mode	When MF = 0, FM mode is selected; and when MF = 1, MFM mode is selected.
MT	Multi-Track	When MT = 1, a multi-track operation is to be performed. After finishing a read/write operation on side 0, the DDFDC will automatically start searching for sector 1 on side 1.
N	Bytes/Sector	The number of data bytes written in a sector.
ND	Non-DMA Mode	When ND = 1, operation is in the Non-DMA mode; when ND = 0, operation is in the DMA mode.
NTN	New Track Number	A new track number, which will be reached as a result of the Seek command. Desired head position.
PTN	Present Track Number	The track number at the completion of Sense Interrupt Status command. Present head position.
R	Record (Sector)	The sector number to be read or written.
RS	Register Select	Controls selection of Main Status Register (RS = low) or Data Register (RS = high).
R/W	Read/Write	Either read (R) or write (W) signal.
ST	Sectors/Track	The number of sectors per track.
SK	Skip	Skip Deleted Data Address Mark.
SRT	Step Rate Time	The stepping rate for the FDD (1 to 16 ms in 1 ms increments). Stepping rate applies to all drives (F = 1 ms, E = 2 ms, etc.)
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	Four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the Main Status Register (selected by RS = low). ST0-ST3 may be read only after a command has been executed and contain information relevant to that particular command.
STP	Sector Test Process	During a Scan command, if STP = 01, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA controller); and if STP = 02, then alternate sectors are read and compared.
T	Track Number	The current/selected track number of the medium (0–255).
US0,US1	Unit Select	A selected drive number (0-3).

ST0
3 NR —Not Ready.
0 FDD is ready.
1 FDD is not ready at issue of read or write command. If a read or write command is issued to side 1 of a single-sided drive, this bit is also set.

ST0
2 HD —Head Address. (At Interrupt).
0 Head Select 0.
1 Head Select 1.

ST0
1 0 US —Unit Select. (At Interrupt).
0 0 FDD 0 selected.
0 1 FDD 1 selected.
1 0 FDD 2 selected.
1 1 FDD 3 selected.

Status Register 1 (ST1)

7	6	5	4	3	2	1	0
EN	0	DE	OR	0	ND	NW	MA

ST1
7 EN —End of Track.
0 No error.
1 DDFDC attempted to access a sector beyond the last sector of a track.

ST1
6 —Not Used. Always Zero.

ST1
5 DE —Data Error.
0 No error.
1 DDFDC detected a CRC error in ID field or the Data field.

ST1
4 OR —Over Run.
0 No error.
1 DDFDC was not serviced by the system during data transfers, within a predetermined time interval.

ST1
3 —Not Used. Always Zero.

ST1
2 ND —No Data.
0 No error.
1 3 possible errors.

1. DDFDC cannot find sector specified in ID Register during execution of Read Data, Write Deleted Data or Scan commands.
2. DDFDC cannot read ID field without an error during Read ID command.
3. DDFDC cannot find starting sector during execution of Read a Track command.

ST1
1 NW —Not Writable.
0 No error.
1 DDFDC detected a write protect signal from FDD during execution of Write Data, Write Deleted Data or Format a Track commands.

ST1
0 MA —Missing Address Mark.
0 No error.
1 2 possible errors.

1. DDFDC cannot detect the ID Address Mark after encountering the index hole twice.
2. DDFDC cannot detect the Data Address Mark or Deleted Data Address Mark. The MD (Missing Address Mark in Data field) of Status Register 2 is also set.

Status Register 2 (ST2)

7	6	5	4	3	2	1	0
0	CM	DD	WT	SH	SN	BT	MD

ST2
7 —Not Used. Always Zero.

ST2
6 CM —Control Mark.
0 No error.
1 DDFDC encountered a sector which contained a Deleted Data Address Mark during execution of a Read Data, Read a Track, or Scan command, or which contained a Data Address Mark during execution of a Read Deleted Data command.

ST2
5 DD —Data Error in Data Field.
0 No error.
1 DDFDC detected a CRC error in the Data field.

ST2
4 WT —Wrong Track.
0 No error.
1 Contents of T on the disk is different from that stored in IDR. Bit is related to ND (Bit 2) of Status Register 1.

ST2
3 SH —Scan Equal Hit.
0 No "equal" condition during a scan command.
1 "Equal" condition satisfied during a scan command.

ST2
2 SN —Scan Not Satisfied.
0 No error.
1 DDFDC cannot find a sector on the track which meets the scan command condition.

ST2
1 BT —Bad Track.
0 No error.
1 Contents of T on the disk is different from that stored in the IDR and T = FF. Bit is related to ND (Bit 2) of Status Register 1.

ST2
0 MD —Missing Address Mark in Data Field.
0 No error.
1 DDFDC cannot find a Data Address Mark or Deleted Data Address Mark during a data read from the disk.

Status Register 3 (ST3)

7	6	5	4	3	2	1	0
FLT	WP	RDY	TRK0	TS	HD	US1	US0

Status Register 3 (ST3) holds the results of the Sense Drive Status command.

ST3
7 FLT —Fault.
0 Fault (FLT) signal from the FDD is low.
1 Fault (FLT) signal from the FDD is high.

ST3
6 WP —Write Protect.
0 Write Protect (WP) signal from the FDD is low.
1 Write Protect (WP) signal from the FDD is high.

ST3
5 RDY —Ready.
0 Ready (RDY) signal from the RDD is low.
1 Ready (RDY) signal from the FDD is high.

ST3
4 TRK0 —Track 0.
0 Track 0 (TRK0) signal from the FDD is low.
1 Track 0 (TRK0) signal is from the FDD is high.

ST3
3 TS —Two Side.
0 Two Side (TS) signal from the FDD is low.
1 Two Side (TS) signal from the FDD is high.

ST3
2 HD —Head Select.
0 Head Select (HD) signal to the FDD is low.
1 Head Select (HD) signal to the FDD is high.

ST3
1 US1 —Unit Select 1.
0 Unit Select 1 (US1) signal to the FDD is low.
1 Unit Select 1 (US1) signal to the FDD is high.

ST3
0 US0 —Unit Select 0.
0 Unit Select 0 (US0) signal to the FDD is low.
1 Unit Select 0 (US1) signal to the FDD is high.

COMMAND SEQUENCE

The DDFDC is capable of performing 15 different commands. Each command is initiated by a multi-byte transfer of data from the system. After command execution, the result of the command may be a multi-byte transfer of data back to the system. Because of this multi-byte transfer of information between the DDFDC and the system, each command consists of three phases:

Command Phase—The DDFDC receives all information required to perform a particular operation from the system.

Execution Phase—The DDFDC performs the instructed operation.

Result Phase—After completion of the operation, status and other housekeeping information are made available to the system.

The bytes of data sent to the DDFDC to form a command, and read out of the DDFDC in the result phase, must occur in the order shown for each command sequence. That is, the command code byte must be sent first followed by the other bytes in the specified sequence. All command bytes must be written and all result bytes must be read in each phase. After the last byte of data in the command phase is received by the DDFDC, the execution phase starts. Similarly, when the last byte of data is read out in the result phase, the command is ended and the DDFDC is ready to accept a new command. A command can be terminated by asserting the $\overline{\text{DONE}}$ signal to the DDFDC. This ensures that the processor can always get the DDFDC's attention even if the command in process hangs up in an abnormal manner.

COMMAND DESCRIPTION

READ DATA

A command set of nine bytes places the DDFDC into the Read Data mode. After the Read Data command has been received the DDFDC loads the head (if it is unloaded), waits the specified Head Settling Time (defined in the Specify command), then begins reading ID Address Marks and ID fields from the disk. When the current sector number (R) stored in the ID Register (IDR) matches the sector number read from the disk, the DDFDC transfers data from the disk Data field to the data bus.

After completion of the read operation from the current sector, the DDFDC increments the Sector Number (R) by one, and the data from the next sector is read and output to the data bus. This continuous read function is called a "Multi-Sector Read Operation." The Read command terminates after reading the last data byte from sector R when R = EOT. ST0 bits 7 and 6 are set to 0 and 1, respectively, and ST1 bit 7 (EN) is set to a 1.

The Read Data command can also be terminated by a low $\overline{\text{DONE}}$ signal. $\overline{\text{DONE}}$ should be issued at the same time that the $\overline{\text{DACK}}$ for the last byte of data is sent. Upon receipt of $\overline{\text{DONE}}$, the DDFDC stops outputting data to the data bus, but continues to read data from the current sector, checks CRC (Cyclic Redundancy Count) bytes, and then at the end of that sector terminates the Read Data command and sets bits 7 and 6 in ST0 to 0. The amount of data

which can be handled with a single command to the DDFDC depends upon MT (Multi-Track), MF (MFM/FM), and N (Number of Bytes/Sector) values. Table 3 shows the transfer capacity.

The multi-track function (MT) allows the DDFDC to read data from both sides of the disk. For a particular track, data is transferred starting at sector 1, side 0 and completed at sector L, side 1 (sector L = last sector on the side). This function pertains to only one track (the same track) on each side of the disk.

When N = 0 in command byte 6 (FM mode), the Data Length (DTL) in command byte 9 defines the data length that the DDFDC must treat as a sector. If DTL is smaller than the actual data length in a sector, the data beyond the DTL is not sent to the data bus. The DDFDC reads (internally) the complete sector, performs the CRC check, and depending upon the manner of command termination, may perform a multi-sector Read operation. When N is non-zero (MFM mode), DTL has no meaning and should be set to FF.

At the completion of the Read Data command, the head is not unloaded until the Head Unload Time (HUT) interval defined in the Specify command has elapsed. The head settling time may be avoided between subsequent reads if the processor issues another command before the head unloads. This time savings is considerable when disk contents are copied from one drive to another.

If the DDFDC detects the Index Hole twice in succession without finding the right sector (indicated in R), then the DDFDC sets the No Data (ND) flag in Status Register 1 (ST1) to a 1, sets Status Register 0 (ST0) bits 7 and 6 to 0 and 1, respectively, and terminates the Read Data command.

After reading the ID and Data fields in each sector, the DDFDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the DDFDC sets the Data Error (DE) flag in ST1 to a 1, sets the Data Error in Data Field (DD) flag in ST2 to a 1 if a CRC error occurs in the Data field, sets bits 7 and 6 in ST0 to 0 and 1, respectively, and terminates the command.

If the DDFDC reads a **Deleted Data Address Mark** from the disk, and the Skip Deleted Data Address Mark bit in the first command byte is not set (SK = 0), then the DDFDC reads all the data in the sector, sets the Control Mark (CM) flag in ST2 to a 1, and terminates the command. If SK = 1, the DDFDC skips the sector with the **Deleted Data Address Mark** and reads the next sector. The CRC bits in the deleted data field are not checked when SK = 1.

During disk data transfers from the DDFDC to the system, the DDFDC must be serviced by the system within 27 μs in the FM mode, and within 13 μs in the MFM mode, otherwise the DDFDC sets the Over Run (OR) flag in ST1 to a 1, sets bits 7 and 6 in ST0 to 0 and 1, respectively, and terminates the command.

If the processor terminates a read (or write) operation in the DDFDC, then the ID information in the result phase is dependent upon the state of the MT bit in the first command byte and the End of Track (EOT) byte. Table 4 shows the values for Track Number (T), Head Number (H), Sector Number (R), and Number of Data Bytes/Sector (N), when the processor terminates the command.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	0	0	1	1	0
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Table 3. DDFDC Transfer Capacity

Multi-Track (MT)	MFM/FM (MF)	Bytes/Sector (N)	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Disk
0	0	00	(128) (26) = 3,328	26 at Side 0
0	1	01	(256) (26) = 6,656	or 26 at Side 1
1	0	00	(128) (52) = 6,656	26 at Side 1
1	1	01	(256) (52) = 13,312	
0	0	01	(256) (15) = 3,840	15 at Side 0
0	1	02	(512) (15) = 7,680	or 15 at Side 1
1	0	01	(256) (30) = 7,680	15 at Side 1
1	1	02	(512) (30) = 15,360	
0	0	02	(512) (8) = 4,096	8 at Side 0
0	1	03	(1024) (8) = 8,192	or 8 at Side 1
1	0	02	(512) (16) = 8,192	8 at Side 1
1	1	03	(1024) (16) = 16,384	

Table 4. DDFDC Command Termination Values

Command Phase ID		Final Sector Transferred to/from Data Bus	Result Phase ID			
Multi-Track (MT)	Head Number (HD)		Track Number (T)	Head Number (H)	Sector Number (R)	No. of Data Bytes (N)
0	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	T + 1	NC	01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	T + 1	NC	01	NC
1	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	NC	LSB	01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	T + 1	LSB	01	NC

Notes:
1. NC (No Change): The same value as the one at the beginning of command execution.
2. LSB (Least Significant Bit): The least significant bit of H is complemented.

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

WRITE DATA

A command set of nine bytes places the DDFDC in the Write Data mode. After the Write Data command has been received the DDFDC loads the head (if it is unloaded), waits the specified Head Settling Time (defined in the Specify command), then begins reading ID fields from the disk. When the four bytes (T, H, R, N) loaded during the command match the four bytes of the ID field from the disk, the DDFDC transfers data from the data bus to the disk Data field.

After writing data into the current sector, the DDFDC increments the sector number (R) by one, and writes into the Data field in the next sector. The DDFDC continues this multi-sector write operation until the last byte is written to sector R when R = EOT. ST0 bits 7 and 6 are set to 0 and 1, respectively, and ST1 bit 7 (EN) is set to a 1.

The command can also be terminated by a low on $\overline{\text{DONE}}$. If $\overline{\text{DONE}}$ is sent to the DDFDC while writing into the current sector, then the remainder of the Data field is filled with 00 (zeros). In this case, ST0 bits 7 and 6 are set to 0 and the command is terminated.

The DDFDC reads the ID field of each sector and checks the CRC bytes. If the DDFDC detects a read error (incorrect CRC) in one of the ID fields, it terminates the Write Data command, sets the DE flag in ST1 to a 1, and sets bits 7 and 6 in ST0 to 0 and 1, respectively.

The Write Data command operates in much the same manner as the Read Data command. Refer to the Read Data command for the handling of the following items:

- Transfer Capacity
- End of Track (EN) flag
- No Data (ND) flag
- Head Unload Time (HUT) interval
- ID information when the processor terminates command (see Table 4)
- Definition of Data Length (DTL) when N = 0 and when N ≠ 0

In the Write Data mode, data transfers from the data bus to the DDFDC must occur within 27 μs in the FM mode, and within 13 μs in the MFM mode. If the time interval between data transfers is longer than this, then the DDFDC terminates the Write Data command, sets the Over Run (OR) flag in ST1 to a 1, and sets bits 7 and 6 in ST0 to 0 and 1, respectively.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	0	0	0	1	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

WRITE DELETED DATA

The Write Deleted Data command is the same as the Write Data command except a Deleted Data Address Mark is written at the beginning of the Data field instead of the normal Data Address Mark.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	0	0	1	0	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector(N)

READ DELETED DATA

The Read Deleted Data command is the same as the Read Data command except that if SK = 0 when the DDFDC detects a **Data Address Mark** at the beginning of a Data field, it reads all the data in the sector and sets the CM flag in ST2 to a 1, and then terminates the command. If SK = 1, then the DDFDC skips the sector with the **Data Address Mark** and reads the next sector.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	0	1	1	0	0
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

READ A TRACK

The Read a Track command is similar to the Read Data command except that this is a continuous read operation where all Data fields from each of the sectors on a track are read and transferred to the data bus. Immediately after encountering the Index Hole, the DDFDC starts reading the Data fields as continuous blocks of data. This command terminates when the number of sectors read is equal to EOT. Multi-track operations are not allowed with this command.

If the DDFDC finds an error in the ID or Data CRC check bytes, it continues to read data from the track. The DDFDC compares the ID information read from each sector with the value stored in the IDR, and sets the ND flag in ST1 to a 1 if there is no match.

If the DDFDC does not find an ID Address Mark on the disk after it encounters the Index Hole for the second time it terminates the command, sets the Missing Address Mark (MA) flag in ST1 to a 1, and sets bits 7 and 6 of ST0 to 0 and 1, respectively.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	MF	SK	0	0	0	1	0
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

READ ID

The two-byte Read ID command returns the present position of the read/write head. The DDFDC obtains the value from the first ID field it is able to read, sets bits 7 and 6 in ST0 to 0 and terminates the command.

If no proper ID Address Mark is found on the disk before the Index Hole is encountered for the second time then the Missing Address Mark (MA) flag in ST1 is set to a 1, and if no data is found then the ND flag in ST1 is also set to a 1. Bits 7 and 6 in ST0 are set to 0 and 1, respectively and the command is terminated.

During this command there is no data transfer between DDFDC and the data bus except during the result phase.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	MF	0	0	1	0	1	0
	2	X	X	X	X	X	HD	US1	US0

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

FORMAT A TRACK

The six-byte Format a Track command formats an entire track. After the Index Hole is detected, data is written on the disk: Gaps, Address Marks, ID fields and Data fields; all are recorded in either the double-density IBM System 34 format (MF = 1) or the single-density IBM 3740 format (MF = 0). The particular format written is also controlled by the values of Number of Bytes/Sector (N), Sectors/Track (ST), Gap Length (GPL) and Data Pattern (D) which are supplied by the processor during the command phase. The Data field is filled with the data pattern stored in D.

The ID field for each sector is supplied by the processor in response to four data requests per sector issued by the DDFDC. The type of data request depends upon the Non-DMA flag (ND) in the Specify command. In the DMA mode (ND = 0), the DDFDC asserts the DMA Request (TXRQ) output four times per sector. In the Non-DMA mode (ND = 1), the DDFDC asserts Interrupt Request ($\overline{IRQ}$) output four times per sector.

The processor must write one data byte in response to each request, sending (in the consecutive order) the Track Number (T), Head Number (H), Sector Number (R) and Number of Bytes/Sector (N). This allows the disk to be formatted with non-sequential sector numbers, if desired.

The processor must send new values for T, H, R, and N to the DDFDC for each sector on the track. For sequential formatting R is incremented by one after each sector is formatted, thus, R contains the total numbers of sectors formatted when it is read during the result phase. This incrementing and formatting continues for the whole track until the DDFDC, upon encountering the Index Hole for the second time, terminates the command and sets bits 7 and 6 in ST0 to 0.

If the Fault (FLT) signal is high from the FDD at the end of a write operation, the DDFDC sets the Equipment Check (EC) flag in ST0 to a 1, sets bits 7 and 6 of ST0 to 0 and 1, respectively, and terminates the command. Also, a low (RDY) signal at the beginning of a command execution phase causes bits 7 and 6 of ST0 to be set to 0 and 1, respectively.

Table 5 shows the relationship between N, ST, and GPL for various disk and sector sizes.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	MF	0	0	1	1	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Number of Bytes per Sector (N)							
	4	Sectors per Track (ST)							
	5	Gap Length (GPL)							
	6	Data Pattern (D)							

Table 5. Standard Floppy Disk Sector Size Relationship

Disk Size	Mode	Sector Size Bytes/Sector	No. of Data Bytes/Sector (N)	No. of Sectors/Tracks (ST)	Gap Length (GPL)[4]		Remarks
					Read/Write Command[1]	Format Command[2]	
8"	FM	128	00	1A	07	1B	IBM Disk 1
		256	01	0F	0E	2A	IBM Disk 2
		512	02	08	1B	3A	
		1024	03	04	47	8A	
		2048	04	02	C8	FF-	
		4096	05	01	C8	FF	
	MFM[3]	256	01	1A	0E	36	IBM Disk 2D
		512	02	0F	1B	54	
		1024	03	08	35	74	IBM Disk 2D
		2048	04	04	99	FF	
		4096	05	02	C8	FF	
		8192	06	01	C8	FF	
5¼"	FM	128	00	12	07	09	
		128	00	10	10	19	
		256	01	08	18	30	
		512	02	04	46	87	
		1024	03	02	C8	FF	
		2048	04	01	C8	FF	
	MFM[3]	256	01	12	0A	0C	
		256	01	10	20	32	
		512	02	08	2A	50	
		1024	03	04	80	F0	
		2048	04	02	C8	FF	
		4096	05	01	C8	FF	

Notes:
1. Suggested values of GPL in Read or Write Commands to avoid overlapping between Data field and ID field of contiguous sections.
2. Suggested values of GPL in Format a Track command.
3. In MFM mode the DDFDC cannot perform a read/write/format operation with 128 bytes/sector (N = 00).
4. Values of ST and GPL are in hexadecimal.

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)*
	5	Head Number (H)*
	6	Sector Number (R)*
	7	Number of Data Bytes per Sector (N)*

* The ID information has no meaning in this command.

SCAN COMMANDS

The scan commands compare data read from the disk to data supplied from the data bus. The DDFDC compares the data, and looks for a sector of data which meets the conditions of $D_{FDD} = D_{BUS}$, $D_{FDD} \leq D_{BUS}$, or $D_{FDD} \geq D_{BUS}$ (D = the data pattern in hexadecimal). A magnitude comparison is performed (FF = largest number, 00 = smallest number). The hexadecimal byte of FF either from the bus or from FDD can be used as a mask byte because it always meets the condition of the compare. After a whole sector of data is compared, if the conditions are not met, the sector number is incremented (R + STP → R), and the scan operation is continued. The scan operation continues until one of the following events occur: the conditions for scan are met (equal, low or equal, or high or equal), the last sector on the track is reached (EOT), or $\overline{DONE}$ is received.

If conditions for scan are met, the DDFDC sets the Scan Hit (SH) flag in ST2 to a 1, and terminates the command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the track (EOT), then the DDFDC sets the Scan Not Satisfied (SN) flag in ST2 to a 1, and terminates the command. The receipt of $\overline{DONE}$ from the processor or DMA controller during the scan operation will cause the DDFDC to complete the comparison of the particular byte which is in process, and then to terminate the command. Table 6 shows the status of bits SH and SN under various conditions of scan.

If SK = 0 and the DDFDC encounters a Deleted Data Address Mark on one of the sectors, it regards that sector as the last sector of the track, sets the Control Mark (CM) bit in ST2 to a 1 and terminates the command. If SK = 1, the DDFDC skips the sector with the Deleted Data Address Mark, sets the CM flag to a 1 in order to show that a Deleted Sector has been encountered, and reads the next sector.

Table 6. Scan Status Codes

Command	Status Register 2		Comments
	Bit 2 = SN	Bit 3 = SH	
Scan Equal	0	1	$D_{FDD} = D_{BUS}$
	1	0	$D_{FDD} \neq D_{BUS}$
Scan Low or Equal	0	1	$D_{FDD} = D_{BUS}$
	0	0	$D_{FDD} < D_{BUS}$
	1	0	$D_{FDD} > D_{BUS}$
Scan High or Equal	0	1	$D_{FDD} = D_{BUS}$
	0	0	$D_{FDD} > D_{BUS}$
	1	0	$D_{FDD} < D_{BUS}$

When either the STP sectors are read (contiguous sectors = 01, or alternate sectors = 02) or MT (Multi-Track) is set, **the last sector on the track must be read.** For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26, and the scan command starts reading at sector 21. Sectors 21, 23, and 25 are read, then the next sector (26) is skipped and the Index Hole is encountered before the EOT value of 26 can be read. This results in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the scan command would be completed in a normal manner.

During a scan command data is supplied from the data bus for comparison against the data read from the disk. In order to avoid having the Over Run (OR) flag set in ST1, data must be available from the data bus in less than 27 μs (FM mode) or 13 μs (MFM mode). If an OR occurs, the DDFDC terminates the command and sets bits 7 and 6 of ST0 to 0 and 1, respectively.

The following tables specify the command bytes and describe the result bytes for the three scan commands.

SCAN EQUAL

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	1	0	0	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Sector Test Process (STP)							

Result Phase:

R		
	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

SCAN LOW OR EQUAL

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	1	1	0	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Sector Test Process (STP)							

Result Phase:

R		
	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

SCAN HIGH OR EQUAL

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	1	1	1	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Sector Test Process (STP)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

SEEK

The three-byte Seek command steps the FDD read/write head from track to track. The DDFDC has two independent Present Track Registers for each drive. They are cleared only by the Recalibrate command. The DDFDC compares the Present Track Number (PTN) which is the current head position with the New Track Number (NTN), and if there is a difference, performs the following operation:

If PTN < NTN: Sets the direction output (LCT/DIR) high and issues step pulses (FR/STP) to the FDD to cause the read/write head to step in.

If PTN > NTN: Sets the direction output (LCT/DIR) low and issues step pulses to the FDD to cause the read/write head to step out.

The rate at which step pulses are issued is controlled by the Step Rate Time (SRT) in the Specify command. After each step pulse is issued, NTN is compared against PTN. When NTN = PTN, then the Seek End (SE) flag in ST0 is set to a 1, bits 7 and 6 in ST0 are set to 0, and the command is terminated. At this point DDFDC asserts IRQ.

The FDD Busy flag (bit 0-3) in the Main Status Register (MSR) corresponding to the FDD performing the Seek operation is set to a 1.

After command termination, all FDD Busy bits set are cleared by the Sense Interrupt Status command.

During the command phase of the Seek operation the DDFDC sets the Controller Busy (CB) flag in the MSR to 1; but during the execution phase the CB flag is set to 0 to indicate DDFDC non-busy. While the DDFDC is in the non-busy state, another Seek command may be issued, and in this manner parallel seek operations may be performed on all drives at once.

No command other than Seek will be accepted while the DDFDC is sending step pulses to any FDD. If a different command type is attempted, the DDFDC will set bits 7 and 6 in ST0 to a 1 and 0, respectively, to indicate an invalid command.

If the FDD is in a not ready state at the beginning of the command execution phase or during the seek operation, then the DDFDC sets the Not Ready (NR) flag in ST0 to a 1, sets ST0 bits 7 and 6 to 0 and 1, respectively, and terminates the command.

If the time to write the three bytes of the Seek command exceeds 150 μs, the time between the first two step pulses may be shorter than the Step Rate Time (SRT) defined by the Specify command by as much as 1 ms.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	1	1	1	1
	2	X	X	X	X	X	0	US1	US0
	3	New Track Number (NTN)							

Result Phase: None.

RECALIBRATE

This two-byte command retracts the FDD read/write head to the Track 0 position. The DDFDC clears the contents of the PTN counters, and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal (TRK0) is low, the direction signal (LCT/DIR) output remains low and step pulses are issued on FR/STP. When TRK0 goes high the DDFDC sets the Seek End (SE) flag in ST0 to a 1 and terminates the command. If the TRK0 is still low after 256 step pulses have been issued, the DDFDC sets Seek End (SE) and Equipment Check (EC) flags in ST0 to 1s, sets bits 7 and 6 of ST0 to 0 and 1, respectively, and terminates the command.

The ability to do overlap Recalibrate commands to multiple FDDs and the loss of the RDY signal, as described in the Seek command, also applies to the Recalibrate command.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	0	1	1	1
	2	X	X	X	X	X	0	US1	US0

Result Phase: None.

SENSE INTERRUPT STATUS

Interrupt Request ($\overline{IRQ}$) is asserted by the DDFDC when any of the following conditions occur:

1. Upon entering the result phase of:
   a. Read Data command
   b. Read a Track command
   c. Read ID command
   d. Read Deleted Data command
   e. Write Data command
   f. Format a Track command
   g. Write Deleted Data command
   h. Scan commands
2. Ready (RDY) line from the FDD changes state
3. Seek or Recalibrate command termination
4. During execution phase in the Non-DMA mode

$\overline{IRQ}$ caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. During an execution phase in Non-DMA mode, bit 5 in the MSR is set to 1. Upon entering result phase this bit is set to 0. Reasons 1 and 4 do not require the Sense Interrupt Status command. The interrupt is cleared by reading or writing data to DDFDC. Interrupts caused by reasons 2 and 3 are identified with the aid of the Sense Interrupt Status command. This command resets $\overline{IRQ}$ and sets/resets bits 5, 6, and 7 of ST0 to identify the cause of the interrupt. Table 7 defines the seek and interrupt codes.

Neither the Seek or Recalibrate command has a result phase. Therefore, it is mandatory to use the Sense Interrupt Status command after these commands to effectively terminate them and to verify where the head is positioned by checking the Present Track Number (PTN).

Issuing a Sense Interrupt Status command without an interrupt pending is treated as an invalid command.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	1	0	0	0

Result Phase:

R	1	Status Register 0 (ST0)
	2	Present Track Number (PTN)

SPECIFY

The three-byte Specify command sets the initial values for each of the three internal timers. The Head Unload Time (HUT) defines the time from the end of the execution phase of one of the read/write commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (1 = 16 ms, 2 = 32 ms,. . . F = 240 ms).

The Step Rate Time (SRT) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms,. . .0 = 16 ms.

The Head Load Time (HLT) defines the time between the Head Load (HDL) signal going high and the start of the read/write operation. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms,. . .7F = 254 ms).

The time intervals are a direct function of the clock (CLK on pin 19). Times indicated above are for an 8 MHz clock. If the clock is reduced to 4 MHz (mini-floppy application) then all time intervals are increased by a factor of two.

The choice of DMA or Non-DMA operation is made by the Non-DMA mode (ND) bit. When this bit = 1 the Non-DMA mode is selected, and when ND = 0 the DMA mode is selected.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	0	0	1	1
	2	SRT				HUT			
	3	HLT							ND

SRT — Step Rate Time
HUT— Head Unload Time
HLT — Head Load Time
ND — Non-DMA mode

Result Phase: None.

Table 7. ST0 Seek and Interrupt Code Definition for Sense Interrupt Status

Status Register 0 (ST0) Bits			
Interrupt Code (IC)		Seek End (SE)	Cause
7	6	5	
1	1	0	RDY line changed state, either polarity
0	0	1	Normal termination of Seek or Recalibrate command
0	1	1	Abnormal termination of Seek or Recalibrate command

SENSE DRIVE STATUS

This two-byte command obtains and reports the status of the FDDs. Status Register 3 (ST3) is returned in the result phase and contains the drive status.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	0	1	0	0
	2	X	X	X	X	X	HD	US1	US0

Result Phase:

R	1	Status Register 3 (ST3)

INVALID COMMAND

If an invalid command (i.e., a command not previously defined) is received by the DDFDC, then the DDFDC terminates the command after setting bits 7 and 6 of ST0 to 1 and 0, respectively. The DDFDC does not generate an interrupt during this condition. Bits 6 and 7 (DIO and RQM) in the MSR are both set to a 1 indicating to the processor that the DDFDC is in the result phase and that ST0 must be read. A hex 80 in ST0 indicates that an invalid command was received.

A Sense Interrupt Status command must be sent after a Seek or Recalibrate interrupt, otherwise the DDFDC considers the next command to be an invalid command.

In some applications the user may wish to use this command as a No-Op command, to place the DDFDC in a standby or no operation state.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	Invalid Codes							

Result Phase:

R	1	Status Register 0 (ST0) = 80

PROCESSOR INTERFACE

During the command or result phases, the Main Status Register (MSR) must be read by the processor before each byte of information is transferred to, or from, the DDFDC Data Register. After each byte of data is written to, or read from, the Data Register, the processor should wait 12 μs before reading the MSR. Bits 6 and 7 in the MSR must be a 0 and 1, respectively, before each command byte can be written to the DDFDC. During the result phase, bits 6 and 7 of the MSR must both be 1s prior to reading each byte from the Data Register onto the data bus. Note that this status reading of bits 6 and 7 of the MSR before each byte transfer to and from the DDFDC is required in only the command and result phases and not during the execution phase.

During the result phase all bytes shown in the result phase must be read by the processor. The Read Data command, for example, has seven bytes of data in the result phase. All seven bytes must be read to successfully complete the Read Data command. The DDFDC will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the result phase.

INTERRUPT REQUEST MODE

During the execution phase, the MSR need not be read. The receipt of each data byte from the FDD is indicated by $\overline{IRQ}$ low on pin 18. When the DDFDC is in Non-DMA mode, $\overline{IRQ}$ is asserted during the execution phase. When the DDFDC is in the DMA mode, the $\overline{IRQ}$ is asserted at the result phase. The $\overline{IRQ}$ signal is reset by a read (R/$\overline{W}$ high) or write (R/$\overline{W}$ low) of data to the DDFDC. A further explanation of the $\overline{IRQ}$ signal is described in the Sense Interrupt Status command on page 16. If the system cannot handle interrupts fast enough (within 13 μs for MFM mode or 27 μs for FM mode), it should poll bit 7 (RQM) in the MSR. In this case, RQM in the MSR functions as an Interrupt Request ($\overline{IRQ}$). If the RQM bit is not set, the Over Run (OR) flag in ST1 will be set to a 1 and bits 7 and 6 of ST0 will be set to a 0 and 1, respectively.

DMA MODE

When the DDFDC is in the DMA mode (ND = 0 in the third command byte of the Specify command), TXRQ (DMA Request) is asserted during the execution phase (rather than $\overline{IRQ}$) to request the transfer of a data byte between the data bus and the DDFDC.

During a read command, the DDFDC asserts TXRQ as each byte of data is available to be read. The DMA controller responds to this request with $\overline{DACK}$ low (DMA Acknowledge) and R/$\overline{W}$ high (read). When $\overline{DACK}$ goes low the DMA Request is reset (TXRQ low). After the execution phase has been completed ($\overline{DONE}$ low or the EOT sector is read), $\overline{IRQ}$ is asserted to indicate the start of the result phase. When the first byte of data is read during the result phase, $\overline{IRQ}$ is reset high.

During a write command, the DDFDC asserts TXRQ as each byte of data is required. The DMA controller responds to this request with $\overline{DACK}$ low (DMA Acknowledge) and R/$\overline{W}$ low (write). When $\overline{DACK}$ goes low the DMA Request is reset (TXRQ low). After the execution phase has been completed ($\overline{DONE}$ low or the EOT sector is written), $\overline{IRQ}$ is asserted. This signals the beginning of the result phase. When the first byte of data is read during the result phase, the $\overline{IRQ}$ is reset high.

FDD POLLING

After the Specify command has been received by the DDFDC, the Unit Select lines (US0 and US1) begin the polling mode. Between commands (and between step pulses in the Seek Command) the DDFDC polls all the FDD's looking for a change in the RDY line from any of the drives. If the RDY line changes state (usually due to the door opening or closing) then the DDFDC asserts $\overline{IRQ}$. When Status Register 0 (ST0) is read (after Sense Interrupt Status command is issued), Not Ready (NR = 1) will be indicated. The polling of the RDY line by the DDFDC occurs continuously between commands, thus notifying the processor which drives are on- or off-line. Each drive is polled every 1.024 ms except during read/write commands.

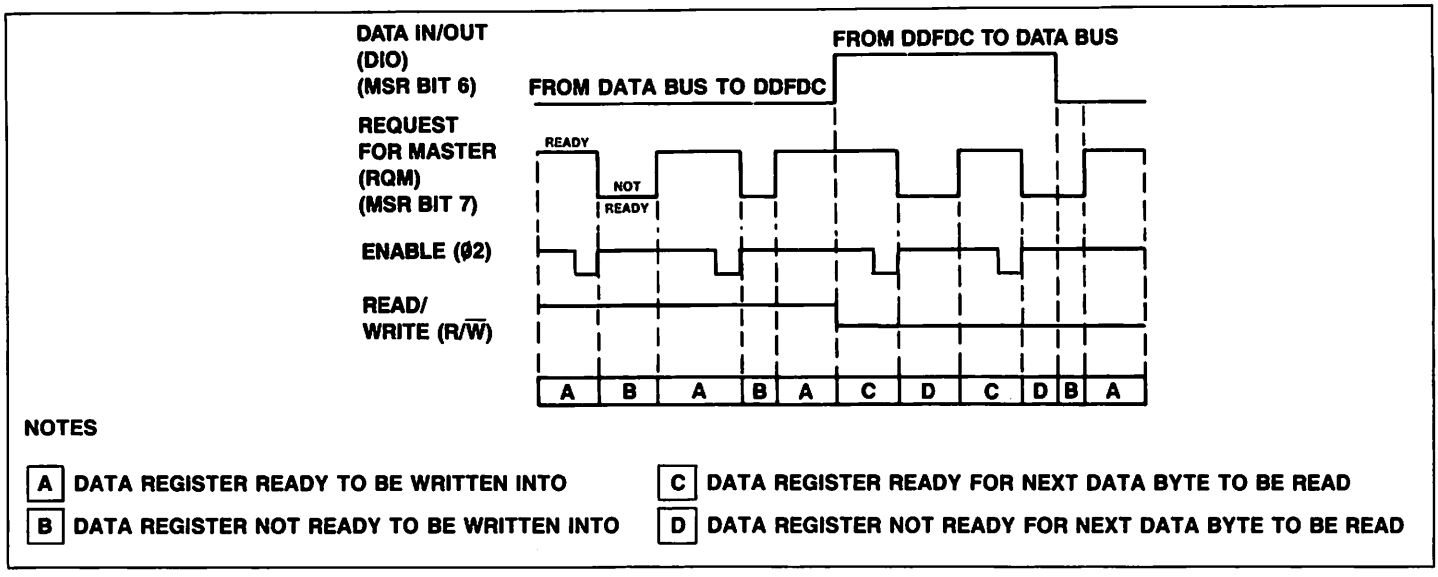


Figure 3. DDFDC and System Data Transfer Timing

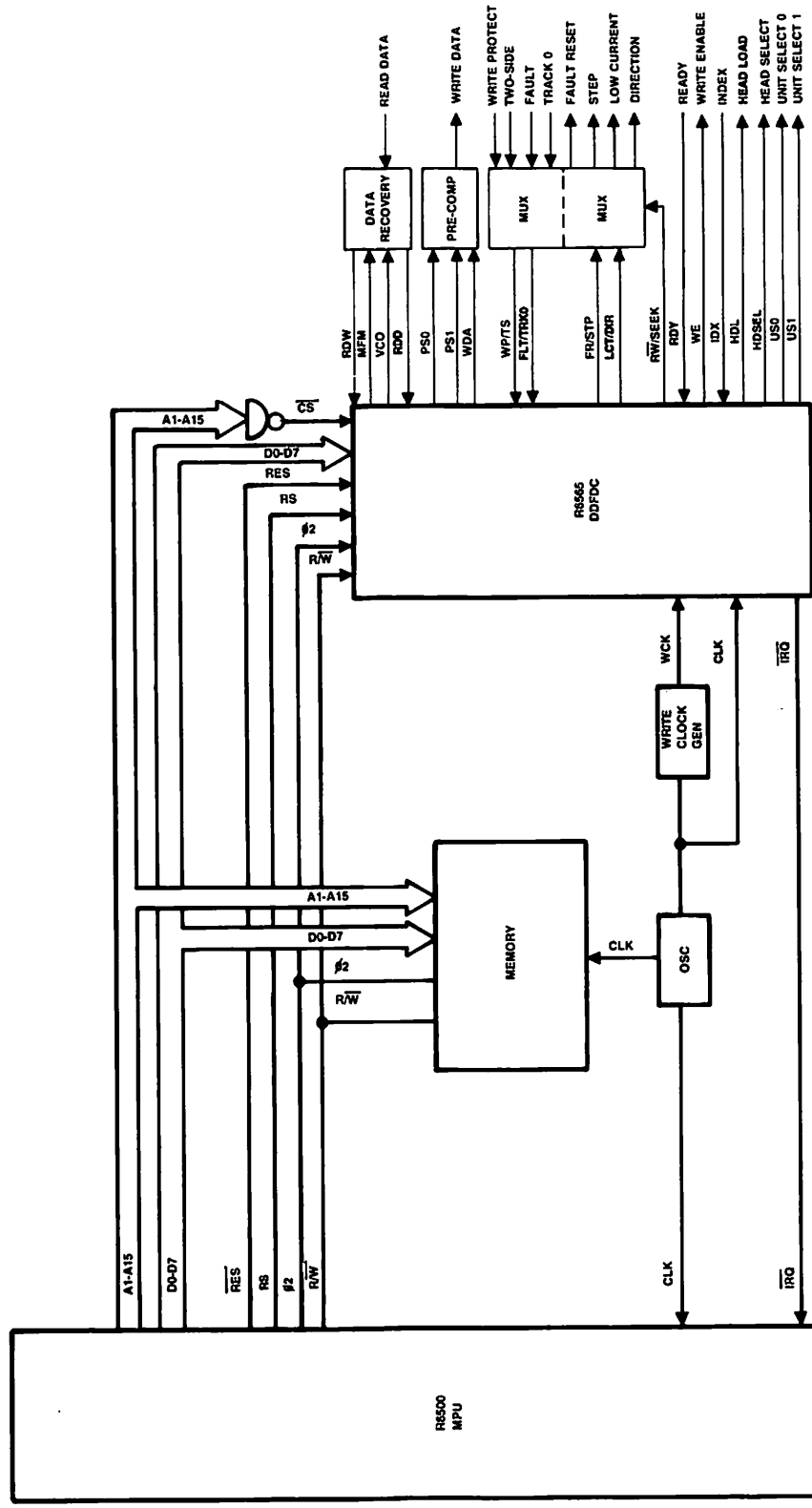


Figure 4. R6565 DDFDC Interface to R6500

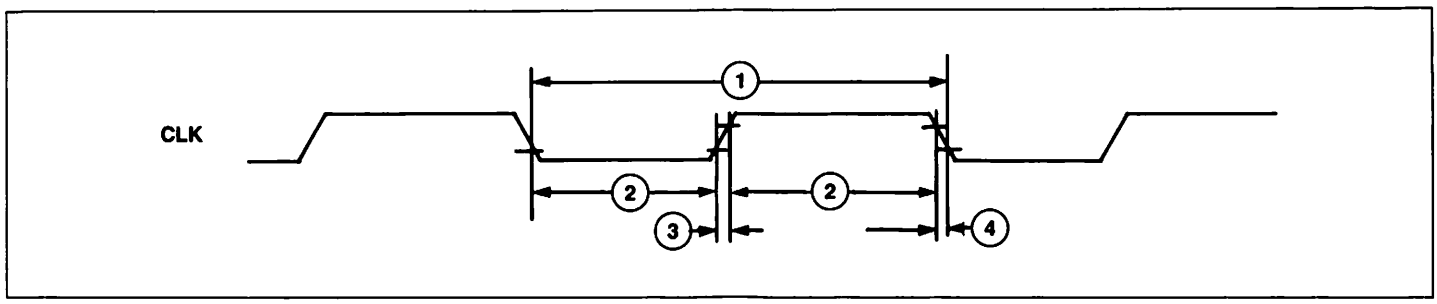


Figure 5. Clock Timing

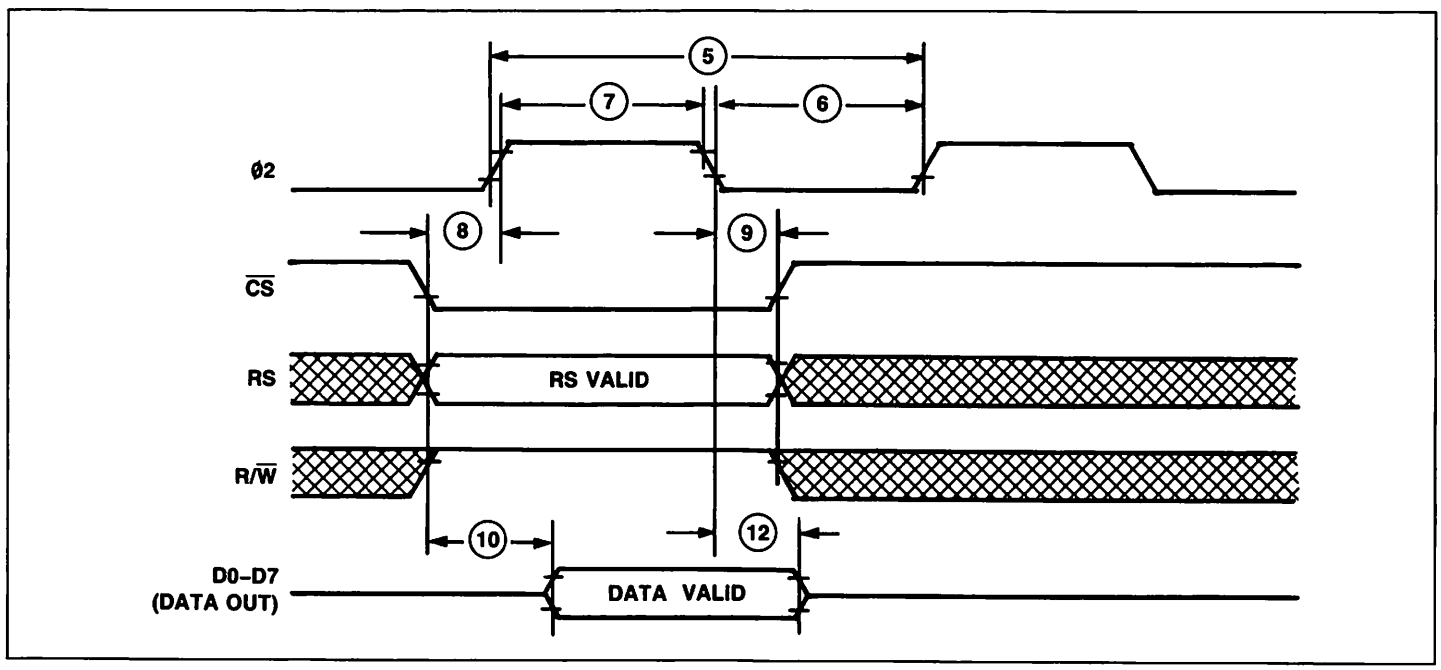


Figure 6. Read Cycle Timing

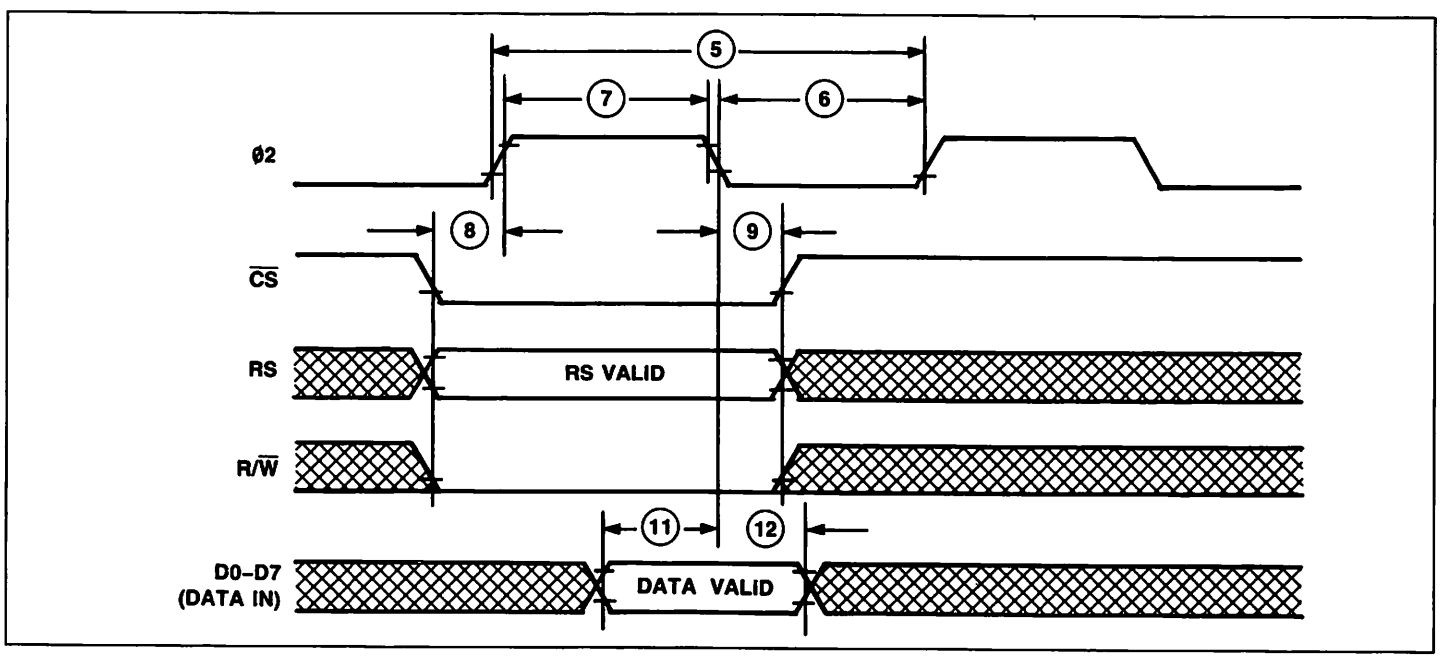


Figure 7. Write Cycle Timing

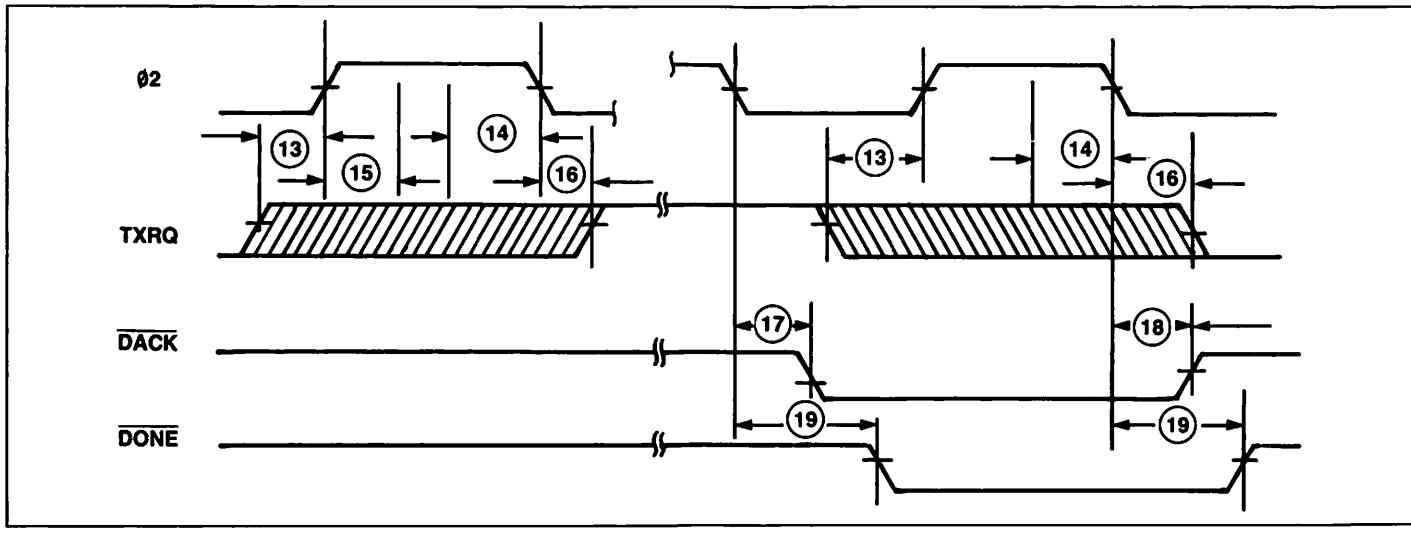


Figure 8. DMA Operation Timing

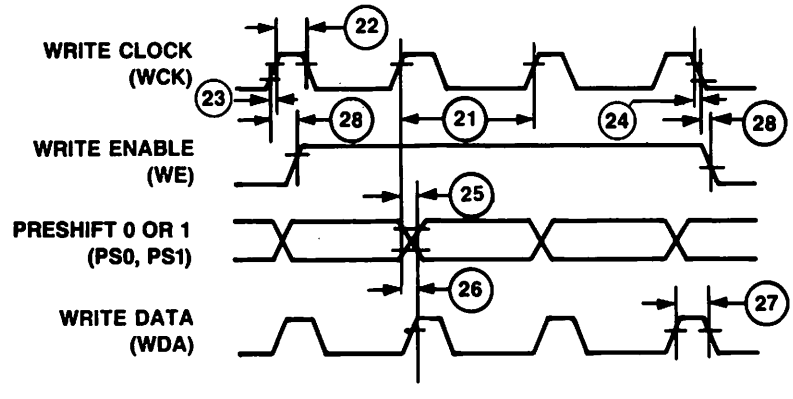
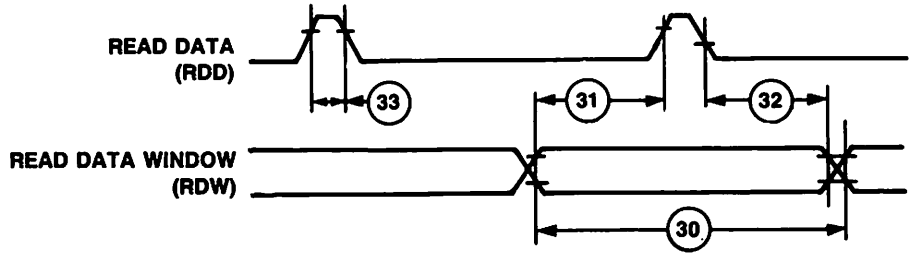


Figure 9. FDD Write Operation Timing



NOTE:
EITHER POLARITY DATA WINDOW IS VALID

Figure 10. FDD Read Operation Timing

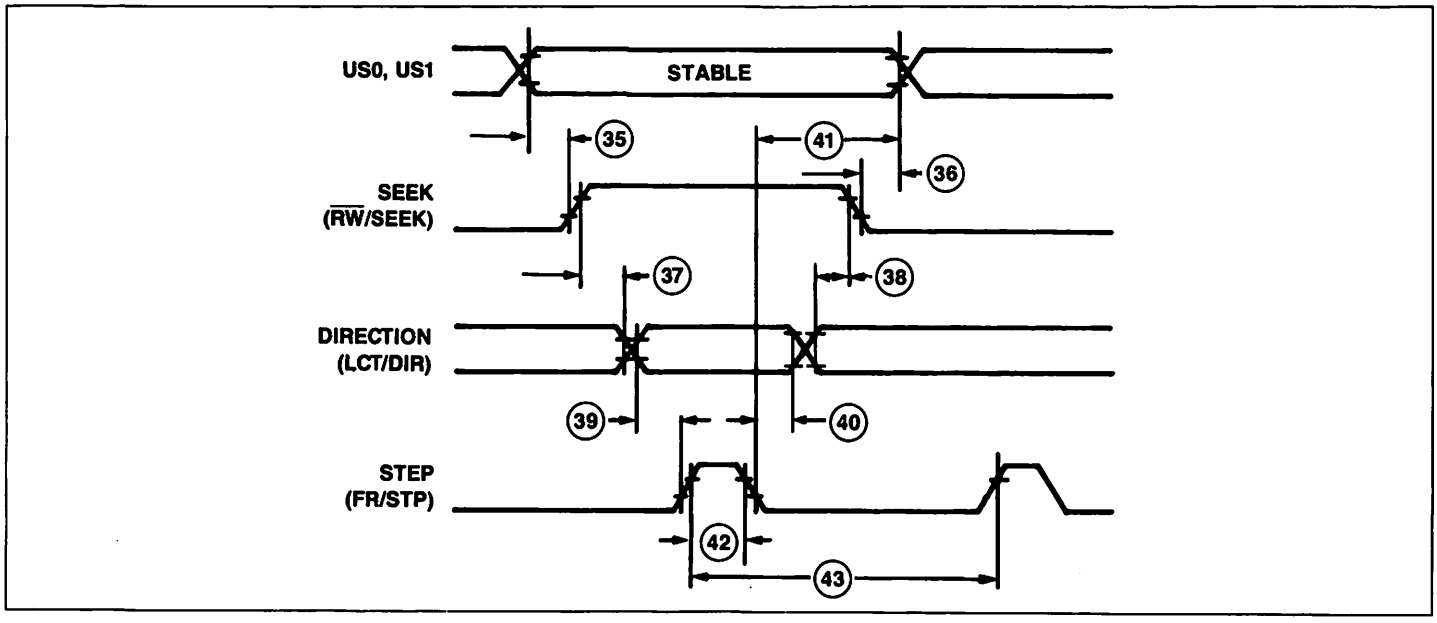


Figure 11. Seek Operation Timing

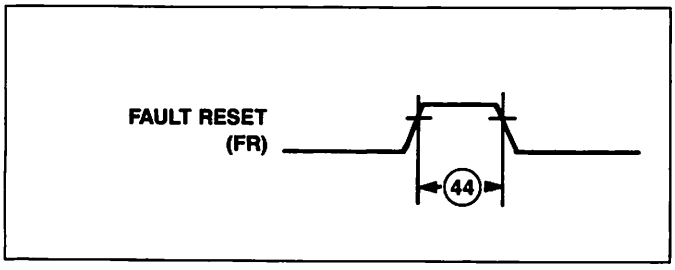


Figure 12. Fault Reset Timing

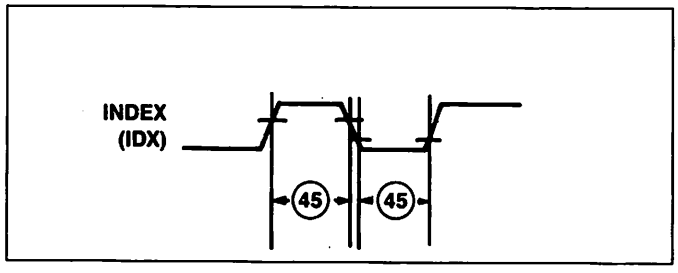


Figure 13. Index Timing

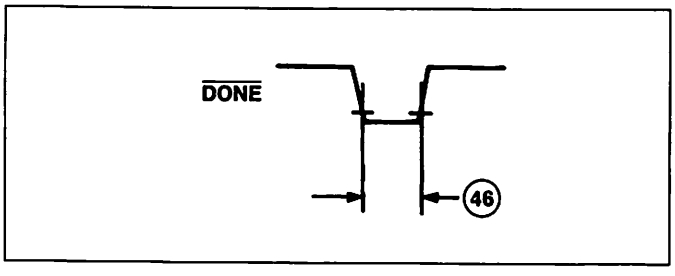


Figure 14. $\overline{\text{DONE}}$ Timing

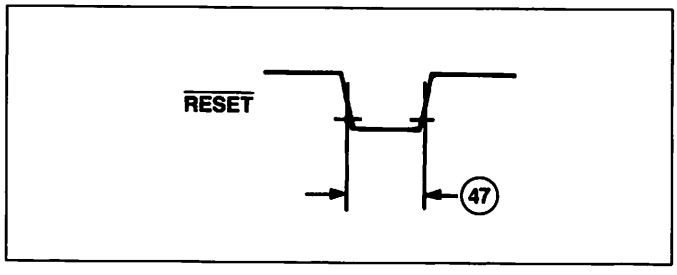
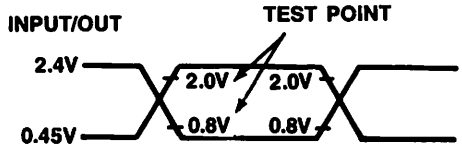
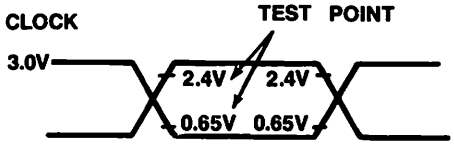


Figure 15. $\overline{\text{RESET}}$ Timing



INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45 V FOR A LOGIC "0." TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0."

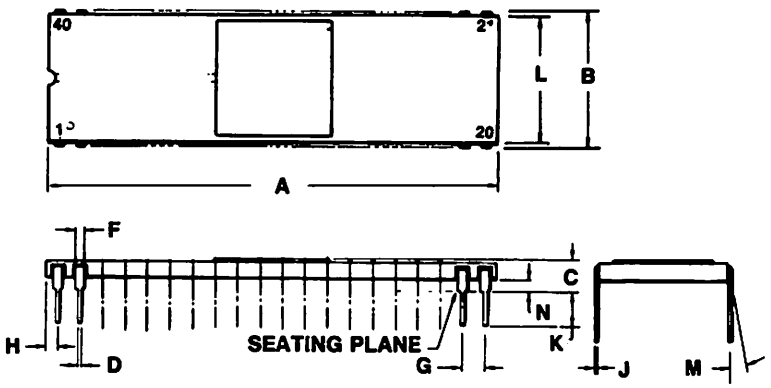


CLOCKS ARE DRIVEN AT 3.0V FOR A LOGIC "1" AND 0.3V FOR A LOGIC "0." TIMING MEASUREMENTS ARE MADE AT 2.4V FOR A LOGIC "1" AND 0.65V FOR A LOGIC "0."

Figure 16. AC Timing Measurement Conditions

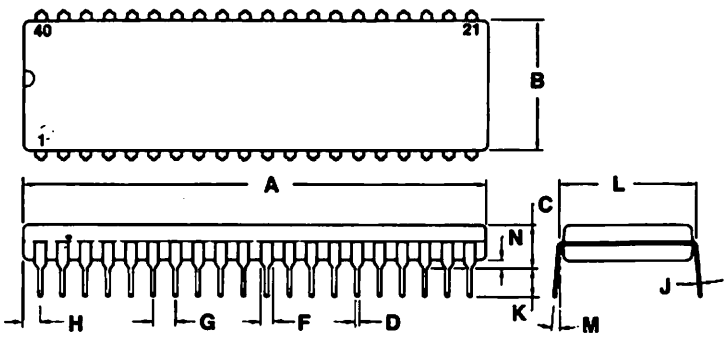
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50.29	51.31	1.980	2.020
B	14.86	15.62	0.585	0.615
C	2.54	4.19	0.100	0.165
D	0.38	– 0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.60	15.37	0.575	0.605
M	0°	10°	0°	10°
N	0.51	1.52	0.020	0.060

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.28	52.32	2.040	2.060
B	13.72	14.22	0.540	0.560
C	3.55	5.08	0.140	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{IN}	−0.3 to +7.0	V
Output Voltage	V_{OUT}	−0.3 to +7.0	V
Operating Temperature Range	T_A	0 to +70	C°
Storage Temperature Range	T_{STG}	−55 to +150	C°

***NOTE:** Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Range
V_{CC} Power Supply	5.0V ±5%
Operating Temperature	0°C to 70°C

DC CHARACTERISTICS

(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc, T_A = 0°C to 70°C, unless otherwise noted)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input Low Voltage Logic CLK and WCK	V_{IL}	 −0.5 −0.5	 0.8 0.65	V	
Input High Voltage Logic CLK and WCK	V_{IH}	 2.0 2.4	 V_{CC} + 0.5 V_{CC} + 0.5	V	
Output Low Voltage	V_{OL}		0.45	V	V_{CC} = 4.75V, I_{OL} = 2.0 mA
Output High Voltage	V_{OH}	2.4	V_{CC}	V	V_{CC} = 4.75V, I_{OH} = −200 µA
V_{CC} Supply Current	I_{CC}		150	mA	V_{CC} = 4.75V
Input Load Current All Inputs	I_{IL}		10	µA	V_{IN} = V_{CC}
			−10	µA	V_{IN} = 0V
High Level Output Leakage Current	I_{LOH}		10	µA	V_{CC} = 0V to 5.25V, V_{SS} = 0V V_{OUT} = V_{CC}
Low Level Output Leakage Current	I_{LOL}		−10	µA	V_{CC} = 0V to 5.25V, V_{SS} = 0V V_{OUT} = +0.45V
Internal Power Dissipation	P_{INT}	—	1.0	W	T_A = 25°C

CAPACITANCE

(T_A = 25°C; f_c = 1 MHz; V_{CC} = 0V)

Parameter	Symbol	Max Limit	Unit
Clock Input	$C_{IN(0)}$	20	pF
Input	C_{IN}	10	pF
Output	C_{OUT}	20	pF
Note: All pins except pin under test tied to ground.			

AC CHARACTERISTICS

(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc, T_A = 0°C to 70°C)

Ref. Fig.	No.	Characteristic	Symbol	Alt. Sym.	Min.	Typ.	Max.	Unit	Test Conditions
5	1	Clock Period	t_{CY}	ϕ_{CY}	120	125	500	ns	CLK = 8 MHz
	2	Clock High, Low Width	t_{CA}	ϕ_0	80	125	—	ns	
	3	Clock Rise Time	t_{CLCH}	ϕ_r	—	—	—	ns	
	4	Clock Fall Time	t_{CHCL}	ϕ_f	—	—	—	ns	
6 & 7	5	Ø2 Clock Cycle Time	t_{CCY}	t_{2CY}	500	—	—	ns	C_L = 100 pF
	6	Ø2 Clock Low	t_{CL}	t_{2CL}	210	—	—	ns	
	7	Ø2 Clock High	t_{CH}	t_{2CH}	220	—	—	ns	
	8	Address Setup Time	t_{AVCH}	t_{AS}	70	—	—	ns	
	9	Address Hold Time	t_{CLAX}	t_{AH}	10	—	—	ns	
	10	Data Access Time	t_{AVDV}	t_{ACC}	—	—	250	ns	
	11	Data Setup Time	t_{DVCL}	t_{DS}	60	—	—	ns	
12	12	Data Hold	t_{AXDX}	t_{DH}	10	—	—	ns	
8	13	TXRQ Setup to Ø2 High	t_{TVCH}	t_{TSH}	120	—	—	ns	CLK = 8 MHz
	14	TXRQ Setup to Ø2 Low	t_{TVCL}	t_{TSL}	210	—	—	ns	
	15	TXRQ Hold from Ø2 High	t_{CHTX}	t_{THH}	10	—	—	ns	
	16	TXRQ Hold from Ø2 Low	t_{CLTX}	t_{THL}	10	—	—	ns	
	17	$\overline{DACK}$ Delay Time	t_{CLAL}	t_{AD}	—	—	150	ns	
	18	$\overline{DACK}$ Hold Time	t_{CLAH}	t_{AH}	30	—	—	µs	
	19	$\overline{DONE}$ Delay Time	t_{CLDL}	t_{DD}	—	—	210	µs	
9	21	WCK Cycle Time	t_{KCY}	t_{CY}	—	note 1	—	µs	
	22	WCK High Width	t_{KHKL}	t_0	80	250	350	ns	
	23	WCK Rise Time	t_{KLKH}	t_r	—	—	20	ns	
	24	WCK Fall Time	t_{KHKL}	t_f	—	—	20	ns	
	25	WCK High to PS0, PS1 Valid (Delay)	t_{KHPV}	t_{CP}	20	—	100	ns	
	26	PS0, PS1 Valid to WDA High (Delay)	t_{PVDH}	t_{CD}	20	—	100	ns	
	27	WDA High Width	t_{DHDL}	t_{WDD}	t_{WCH} −50	—	—	ns	
	28	WE High to WCK High or WE Low to WCK Low	t_{EHKH}	t_{WE}	20	—	100	ns	
10	30	RDW Cycle Time	t_{WCY}	t_{WCY}	—	note 2	—	µs	
	31	RDW Valid to RDD High (Setup)	t_{WVRH}	t_{WRD}	15	—	—	ns	
	32	RDD Low to RDW Invalid (Hold)	t_{RLWI}	t_{RDW}	15	—	—	ns	
	33	RDD High Width	t_{RHRL}	t_{RDD}	40	—	—	ns	
11	35	US0, US1 Valid to SEEK High (Setup)	t_{UVSH}	t_{US}	12	—	—	µs	CLK = 8 MHz
	36	SEEK Low to US0, US1 Invalid (Hold)	t_{SLUI}	t_{SU}	15	—	—	µs	
	37	SEEK High to DIR Valid (Setup)	t_{SHDV}	t_{SD}	7	—	—	µs	
	38	DIR Invalid to SEEK Low (Hold)	t_{DXSL}	t_{DS}	30	—	—	µs	
	39	DIR Valid to STP High (Setup)	t_{DVTH}	t_{DST}	1	—	—	µs	
	40	STP Low to DIR Invalid (Hold)	t_{TLDX}	t_{STD}	24	—	—	µs	
	41	STP Low to US0, US1 Invalid (Hold)	t_{TLUX}	t_{STU}	5	—	—	µs	
	42	STP High Width	t_{THTL}	t_{STP}	6	7	—	µs	
	43	STP Cycle Time	t_{TCY}	t_{SC}	33[3]	—	note 3	µs	
12	44	FR High Width	t_{FHFL}	t_{FR}	8	—	10	µs	
13	45	IDX High Width	t_{IHIL}	t_{IDX}	10	—	—	t_{CY}	
14	46	$\overline{DONE}$ Low Width	t_{THTL}	t_{TC}	1	—	—	t_{CY}	
15	47	$\overline{RES}$ Low Width	t_{RHRL}	t_{RST}	14	—	—	t_{CY}	

Notes:

1.

MFM	Mini	Standard
0	4 µs	2 µs
1	2 µs	1 µs

2. For MFM = 0: Typ. = 2 µs
   For MFM = 1: Typ. = 1 µs
3. t_{SC} = 33 µs min. is for different drive units. In the case of the same unit, t_{SC} can range from 1 ms to 16 ms with 8 MHz clock period, and 2 ms to 32 ms with 4 MHz clock, under software control.

Printed in U.S.A.

SEMICONDUCTOR PRODUCTS DIVISION REGIONAL ROCKWELL SALES OFFICES

HOME OFFICE
Semiconductor Products Division
Rockwell International
4311 Jamboree Road
P.O Box C, MS 501-300
Newport Beach, California
92658-8902
(714) 833-4700
TWX: 910 591-1698

UNITED STATES
Semiconductor Products Division
Rockwell International
1842 Reynolds
Irvine, California 92714
(714) 833-4655
TWX: 910 595-2518

Semiconductor Products Division
Rockwell International
3375 Scott Blvd., Suite 410
Santa Clara, California 95051
(408) 980-1900

Semiconductor Products Division
Rockwell International
921 Bowser Road
Richardson, Texas 75080
(214) 996-6500
TLX: 73-307

Semiconductor Products Division
Rockwell International
10700 West Higgins Rd., Suite 102
Rosemont, Illinois 60018
(312) 297-8862
TWX: 910 233-0179 (RI MED ROSM)

Semiconductor Products Division
Rockwell International
5001B Greentree
Executive Campus, Rt. 73
Marlton, New Jersey 08053
(609) 596-0090
TWX: 710 940-1377

FAR EAST
Semiconductor Products Division
Rockwell International Overseas Corp.
Itohpia Hirakawa-cho Bldg.
7-6, 2-chome, Hirakawa-cho
Chiyoda-ku, Tokyo 102, Japan
(03) 265-6806
TLX: J22198

Rockwell Collins International
Tai Sang Commercial Bldg., 11th Floor
24-34 Hennessy Rd.
Hong Kong
(5) 274-321
TLX: 74071 HK

EUROPE
Semiconductor Products Division
Rockwell International GmbH
Fraunhoferstrasse 11
D-8033 Munchen-Martinsried
West Germany
(089) 857-6016
TLX: 0521/2650 rimd d

Semiconductor Products Division
Rockwell International
Heathrow House, Bath Rd.
Cranford, Hounslow,
Middlesex, England
(01) 759-9911
TLX: 851-25463

Semiconductor Products
Rockwell Collins Italiana S.P.A.
Via Boccaccio, 23
20123 Milano, Italy
(02) 498.74.79
TLX: 316562 RCIMIL 1

YOUR LOCAL REPRESENTATIVE

1/84