

FEBRUARY 1975

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 82S23 (Open Collector Outputs) and the 82S123 (Tri-State Outputs) are Bipolar 256-Bit Read Only Memories, organized as 32 words by 8 bits per word. They are Field-Programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S23 and 82S123 devices are supplied with all outputs at logical "0". Outputs are programmed to a logic "1" level at any specified address by fusing a Ni-Cr link matrix.

The 82S23 and 82S123 are fully TTL compatible, and include on-chip decoding and one chip enable input for ease of memory expansion. They feature either Open Collector or Tri-State outputs for optimization of word expansion in bussed organizations.

Both 82S23 and 82S123 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S23/123, B or F. For the military temperature range (-55°C to +125°C) specify S82S23/123, F only.

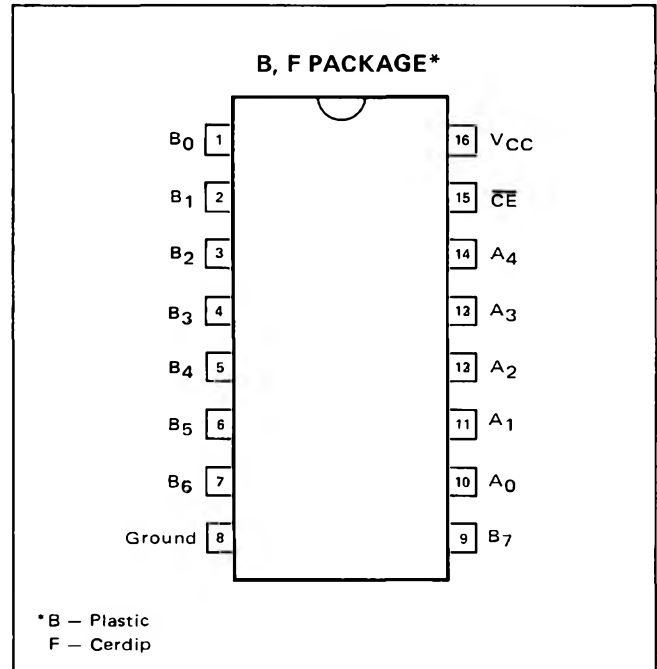
FEATURES

- ORGANIZATION – 32 X 8
- ADDRESS ACCESS TIME:
S82S23/S82S123 – 65ns, MAXIMUM
N82S23/N82S123 – 50ns, MAXIMUM
- POWER DISSIPATION – 1.3mW/BIT TYPICAL
- INPUT LOADING:
S82S23/123 – (-150µA) MAXIMUM
N82S23/123 – (-100µA) MAXIMUM
- ON-CHIP ADDRESS DECODING
- OUTPUT OPTION:
OPEN COLLECTOR – 82S23
TRI-STATE – 82S123
- NO SEPARATE "FUSING" PINS
- UNPROGRAMMED OUTPUTS ARE "0" LEVEL
- 16-PIN CERAMIC DIP

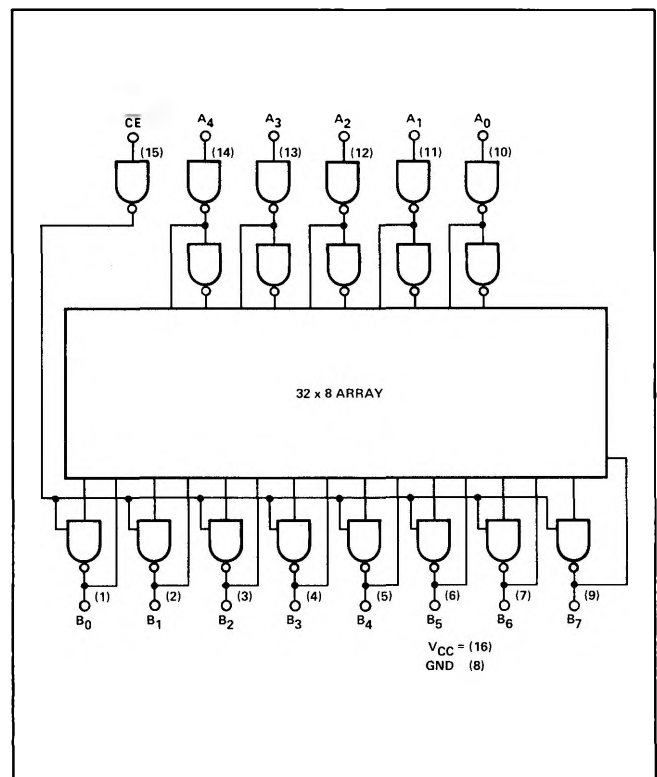
APPLICATIONS

PROTOTYPING/VOLUME PRODUCTION
SEQUENTIAL CONTROLLERS
FORMAT CONVERSION
HARDWIRED ALGORITHMS
RANDOM LOGIC
CODE CONVERSION

PIN CONFIGURATION



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V _{CC}	Power Supply Voltage	+7	Vdc
V _{IN}	Input Voltage	+5.5	Vdc
V _{OH}	High Level Output Voltage (82S23)	+5.5	Vdc
V _O	Off-State Output Voltage (82S123)	+5.5	Vdc
T _A	Operating Temperature Range	0° to +75°	°C
	(N82S23/123)	-55° to +125°	°C
	(S82S23/123)		
T _{stg}	Storage Temperature Range	-65° to +150°	°C

ELECTRICAL CHARACTERISTICS S82S23/S82S123 -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V
 N82S23/N82S123 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS ¹	S82S23/S82S123			N82S23/N82S123			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V _{OL}	"0" Output Voltage			0.5			0.45	V
I _{OLK}	Output Leakage Current (82S23)			50			40	μA
I _{O(OFF)}	Hi-Z State Output Current (82S123)			50			40	μA
				-50			-40	μA
V _{OH}	"1" Output Voltage (82S123)	2.4			2.4			V
C _{IN}	Input Capacitance		5			5		pF
C _{OUT}	Output Capacitance		8			8		pF
I _{IL}	"0" Input Current			-150			-100	μA
I _{IH}	"1" Input Current			50			50	μA
V _{IL}	"0" Level Input Voltage			0.8			0.85	V
V _{IH}	"1" Level Input Voltage	2.0			2.0			V
I _{CC}	V _{CC} Supply Current		65	85		65	77	mA
V _{IC}	Input Clamp Voltage		-0.8	-1.2		-0.8	-1.2	V
I _{OS}	Output Short Circuit Current (82S123)	-20		-100	-20		-90	mA

SWITCHING CHARACTERISTICS S82S23/S82S123 -55°C ≤ T_A ≤ +125°C, 4.5 ≤ V_{CC} ≤ 5.5V
 N82S23/N82S123 0°C ≤ T_A ≤ +75°C, 4.75 ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS ¹	S82S23/S82S123			N82S23/N82S123			UNIT
		MIN	TYP ²	MAX	MIN	TYP ²	MAX	
Propagation Delay								
T _{AA}	Address to Output		35	65		35	50	ns
T _{CD}	Chip Disable to Output		25	40		25	35	ns
T _{CE}	Chip Enable to Output		25	40		25	35	ns

NOTES:
 1. Positive current is defined as into the terminal referenced.
 2. Typical values are at V_{CC} = 5.0V, T_A = +25°C.

PROGRAMMING SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT		
		MIN	TYP	MAX			
Power Supply Voltage							
V_{CCP}^1	To Program	$I_{CCP} = 250 \pm 50\text{mA}$ (Transient or steady state)		9.5	10.0	10.5	V
V_{CCH}	Upper Verify Limit			5.3	5.5	5.7	V
V_{CCL}	Lower Verify Limit			4.3	4.5	4.7	V
V_S^3	Verify Threshold			0.9	1.0	1.1	V
I_{CCP}	Programming Supply Current	$V_{CCP} = +10.0 \pm 0.5\text{V}$		200	250	300	mA
Input Voltage							
V_{IH}	Logical "1"			2.4		5.5	V
V_{IL}	Logical "0"			0	0.4	0.8	V
Input Current							
I_{IH}	Logical "1"	$V_{IH} = +5.5\text{V}$				50	μA
I_{IL}	Logical "0"	$V_{IL} = +0.4\text{V}$				-500	μA
V_{OUT}^2	Output Programming Voltage	$I_{OUT} = 65 \pm 3\text{mA}$ (Transient or steady state)		15.0	15.5	16.0	V
I_{OUT}	Output Programming Current	$V_{OUT} = +15.5 \pm 0.5\text{V}$		62	65	68	mA
T_R	Output Pulse Rise Time			10		50	μs
t_p	\overline{CE} Programming Pulse Width			1		2	ms
t_V	Verify Delay			50			μs
t_D	Pulse Sequence Delay			10			μs
T_{PR}	Programming Time	$V_{CC} = V_{CCP}$				2.5	sec
T_{PS}	Programming Pause	$V_{CC} = 0\text{V}$		5			sec
$\frac{T_{PR}^4}{T_{PR}+T_{PS}}$	Programming Duty Cycle					33	%

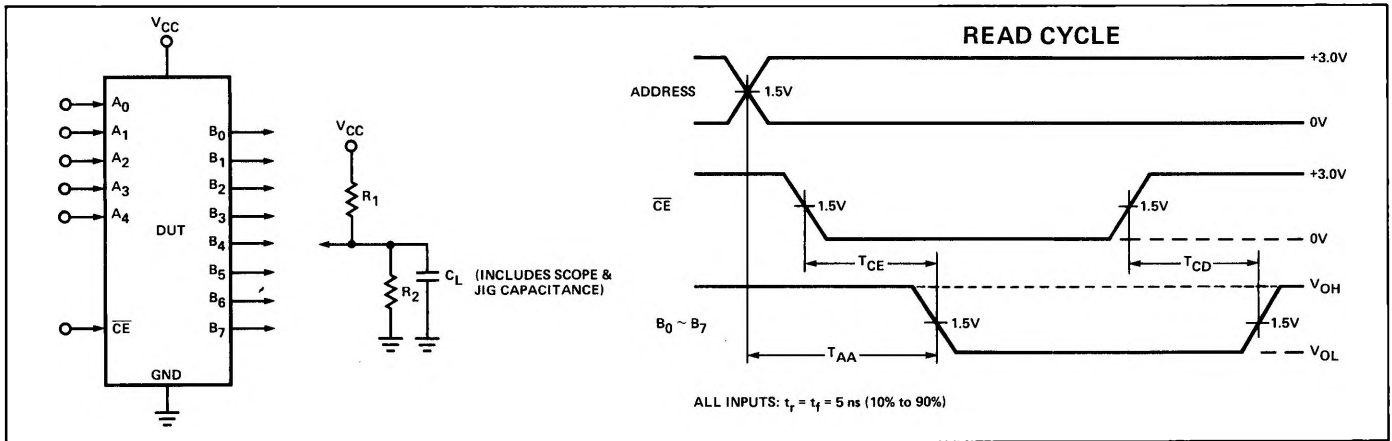
PROGRAMMING PROCEDURE

1. Terminate all device outputs with a $10\text{K}\Omega$ resistor to V_{CC} .
2. Select the Address to be programmed, and raise V_{CC} to $V_{CCP} = +10 \pm 0.5\text{V}$.
3. After $10\mu\text{s}$ delay, apply $I_{OUT} = 65 \pm 3\text{mA}$ to the output to be programmed. Program one output at a time.
4. After $10\mu\text{s}$ delay, pulse the \overline{CE} input to logic "0" for 1 to 2 ms.
5. After $10\mu\text{s}$ delay, remove I_{OUT} from the programmed output.
6. After $10\mu\text{s}$ delay, return V_{CC} to 0V.
7. To verify programming, after $50\mu\text{s}$ delay, raise V_{CC} to $V_{CCH} = +5.5 \pm .2\text{V}$, and apply a logic "0" level to the \overline{CE} input. The programmed output should remain in the "1" state. Again, lower V_{CC} to $V_{CCL} = +4.5 \pm .2\text{V}$, and verify that the programmed output remains in the "1" state.
8. Raise V_{CC} to $V_{CCP} = +10 \pm 0.5\text{V}$ and repeat steps 3 through 7 to program other bits at the same address.
9. After $10\mu\text{s}$ delay, repeat steps 2 through 8 to program all other address locations.

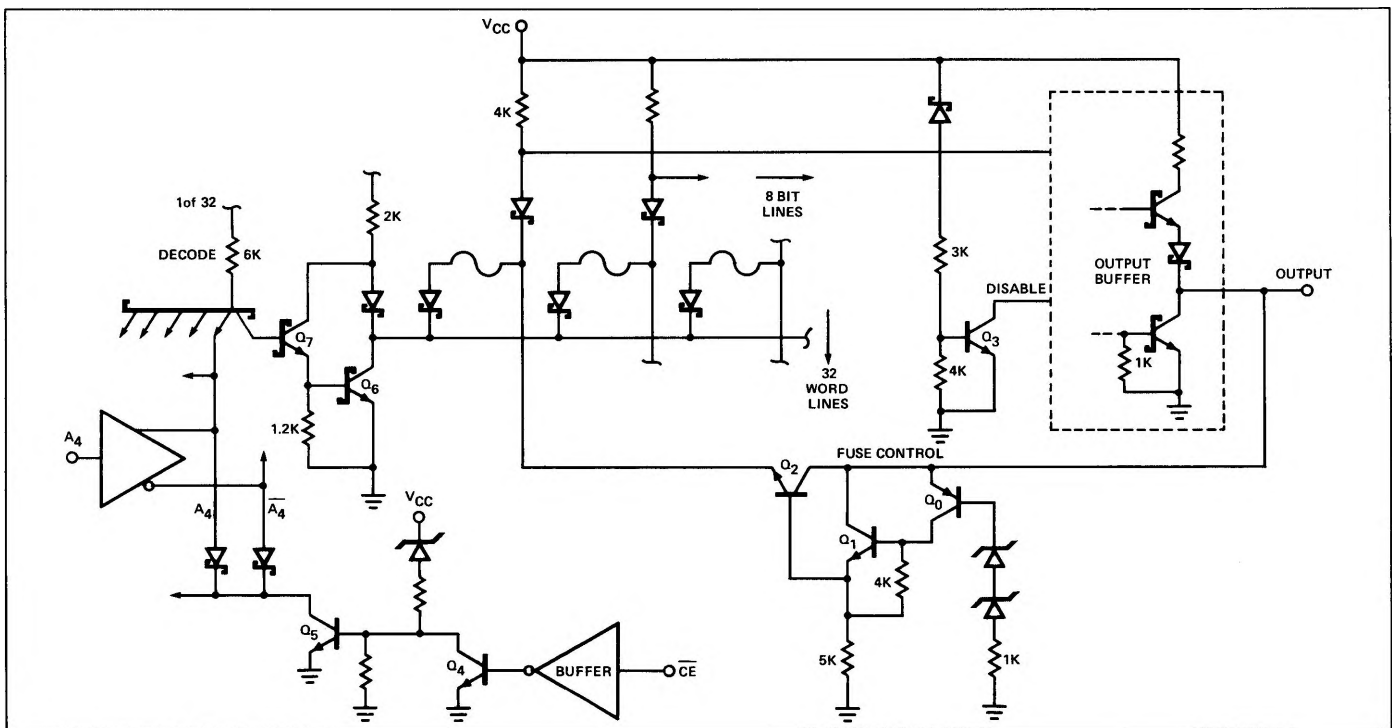
NOTES:

1. Bypass V_{CC} to GND with a $0.01\mu\text{F}$ capacitor to reduce voltage spikes.
2. Care should be taken to insure that $+15.5 \pm 0.5\text{V}$ output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
3. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
4. Continuous fusing for an unlimited time is also allowed, provided that a 33% duty cycle is maintained. This may be accomplished by following each Program-Verify cycle with a Rest period ($V_{CC} = 0\text{V}$) of 4ms.

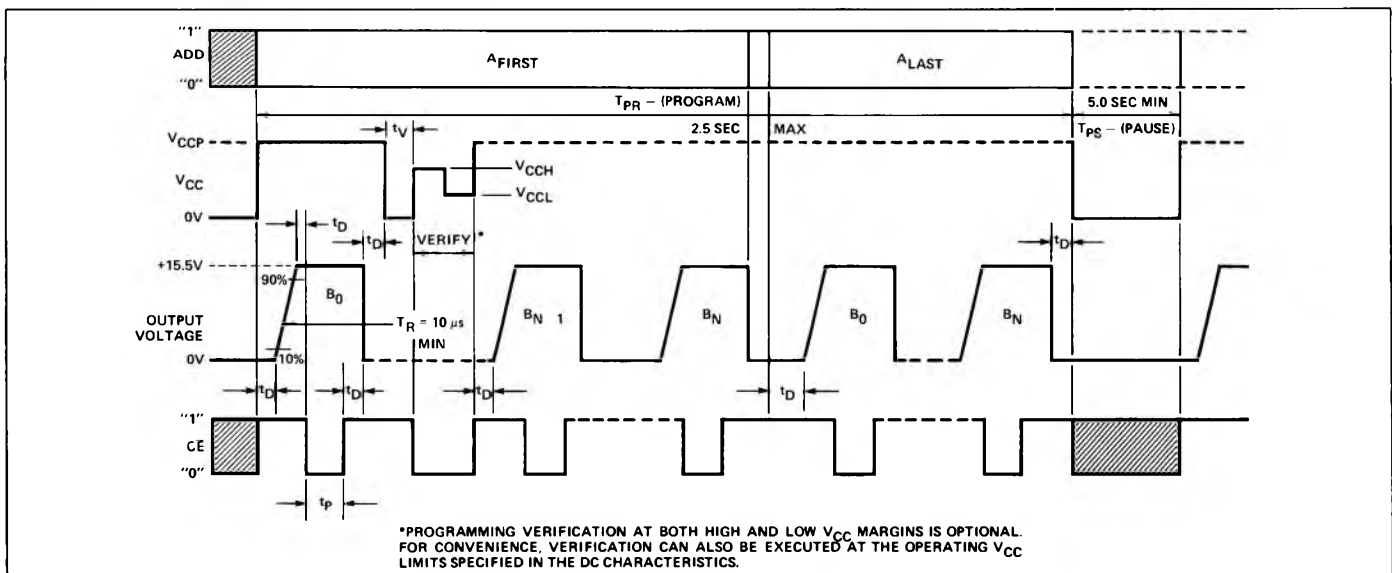
AC TEST FIGURE AND WAVEFORM



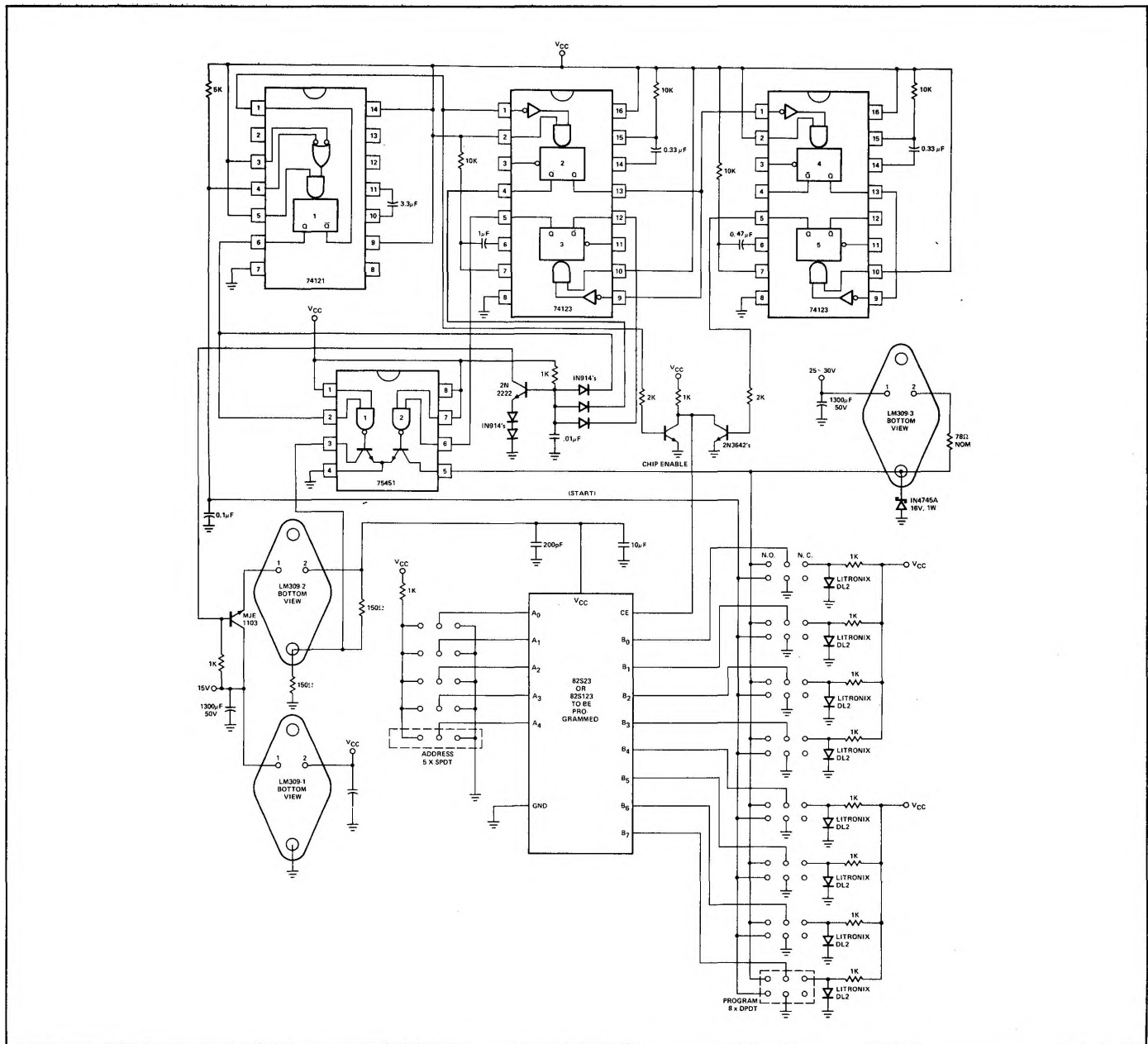
TYPICAL FUSING PATH



TYPICAL PROGRAMMING SEQUENCE



MANUAL PROGRAMMER



TIMING SEQUENCE

