

MCS6501 - MCS6505 MICROPROCESSORS

## The MCS650X Microprocessor Family Concept ----

The MCS6501 - MCS6505 represent the first five members of the MCS650X microprocessor family. This family of products includes a range of software compatible microprocessors which provide a selection of address-able memory range, interrupt input options and on-chip clock oscillators and drivers. The family includes the 40 pin MCS6501 for clock compatibility with the MC6800 microprocessor, the 40 pin MCS6502 with the same features as the MCS6501 but including an on-chip clock, and the 28 pin MCS6503, 4 and 5 providing in addition to the on-chip clock a set of options allowing the user to tailor his microprocessor to suit the particular need. All of the microprocessors in the MCS6501 - MCS6505 group are software compatible within the group and are bus compatible with the M6800 product offering.

## Features of the MCS6501 - MCS6505

- . Single five volt supply
- . N channel, silicon gate, depletion load technology
- . Eight bit parallel processing
- . 55 Instructions
- . Decimal and binary arithmetic
- . Thirteen addressing modes
- . True indexing capability
- . Programmable stack pointer
- . Variable length stack
- . Interrupt capability
- . Non-maskable interrupt
- . Use with any type or speed memory
- . Bi-directional Data Bus

#### Members of the Family

MCS6501 - 40 pin package

- \* Compatible with MC6800
- \* 65K addressable bytes of memory
- MCS6502 40 pin package
  - \* 65K addressable bytes of memory
  - \* On-the-chip clock
  - ✓ External single phase input
  - RC time base input
  - Crystal time base input

- . Instruction decoding and control
- . Addressable memory range of up to 65K bytes
- . "Ready" input
- . Direct memory access capability
- . Bus compatible with MC6800
- . On-the-chip clock options
  - \* External single clock input
  - \* RC time base input
  - \* Crystal time base input
  - . 40 and 28 pin package versions
  - . Pipeline architecture

#### MCS6503 - 28 pin package

\* On-the-chip clock

- \* 4K addressable bytes
- \* Two interrupts

MCS6504 - 28 pin package

- \* On-the-chip clock
- \* 8K addressable bytes
- \* One interrupt

MCS6505 - 28 pin package

- \* On-the-chip clock
- \* 4K addressable bytes
- \* One interrupt, RDY signal

#### **Comments on the Data Sheet**

This data sheet describes the first five members of the MCS650X microprocessor family. The data sheet is constructed to review first the basic "Common Characteristics" - those features which, unless specifically stated otherwise, are common to all of the MCS6501 - MCS6505 microprocessors. Subsequent to a review of the family characteristics will be sections devoted to each member of the group with specific features of each.



## COMMON CHARACTERISTICS

#### MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT	This device contains
SUPPLY VOLTAGE	Vcc	-0.3 to +7.0	Vdc	put protection agains damage due to high st
INPUT VOLTAGE	Vin	-0.3 to +7.0	Vdc	voltages or electric
OPERATING TEMPERATURE	TA	0 to +70	°C	be taken to avoid app
STORAGE TEMPERATURE	TSTG	-55 to +150	°C	than the maximum ration

int atic fields; should lica-er ng.

## ELECTRICAL CHARACTERISTICS (Vec = 5.0V $\pm$ 5%, Vss = 0, T\_A = 25° C)

 $\emptyset_1$ ,  $\emptyset_2$  applies to MCS6501,  $\emptyset_{o(in)}$  applies to MCS6502, 3, 4 and 5.

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input High Voltage $\begin{array}{c} \text{Logic}, \emptyset_{\circ}(\text{in}) \\ \emptyset_{1}, \emptyset_{2} \end{array}$	VIH	Vss + 2.4 Vcc - 0.2	1	Vcc Vcc + 0.25	Vdc
Input Low Voltage $\begin{array}{c} \text{Logic}, \emptyset_{\circ} \text{ (in)} \\ \emptyset_1, \emptyset_2 \end{array}$	V <sub>IL</sub>	Vss - 0.3 Vss - 0.3	2	Vss + 0.4 Vss + 0.2	Vdc
Input High Threshold Voltage RES, NMI, RDY, IRQ, Data, S.O. (6502, 3, 4, 5)	VIHT	Vss + 2.0	•	-	Vdc
Input Low Threshold Voltage RES, NMI, RDY, JRQ, Data, S.O. (6502, 3, 4, 5)	V <sub>ILT</sub>		-	Vss + 0.8	Vdc
Input Leakage Current $(V_{in} = 0 \text{ to } 5.25V, Vcc = 0)$ Logic (Excl.RDY, S.0.) $\theta_1, \theta_2$ $\theta_0(in)$	Iin			2.5 100 10.0	μΑ μμ Αμ
Three-State (Off State) Input Current (V <sub>in</sub> = 0.4 to 2.4V, Vcc = 5.25V) Data Lines	I <sub>TSI</sub>	121	- ,	10	μA
Output High Voltage ( $I_{LOAD} = -100\mu Adc$ , Vcc = 4.75V) BA,Data,AO-A15,R/W	V <sub>OH</sub>	Vss + 2.4	-	-	Vdc
Output Low Voltage (I <sub>LOAD</sub> = 1.6mAdc, Vcc = 4.75V) BA,Data,AO-A15, R/W	VOL	-	-	Vss + 0.4	Vdc
Power Dissipation	PD	-	. 25	.70	W
Capacitance $(v_{in} = 0, T_A = 25^{\circ}C, f = 1MHz)$	C				pF
Logic	Cin	0.700	-	10	
A0-A15, R/W, SYNC, B.A.	Cout	1	2	15	
Ø <sub>o(in)</sub>	Co	-	1	15	
Ø1	C <sub>Ø1</sub>		30	50	
Ø2	Cø2	-	50	80	

Note: IRQ and NMI require 3K pull-up resistors.

CHARACTER COLO	CIDEOL	WTN	TVD	MAY	INTT
CHARACIERISTIC	SIMBOL	MIN.	mr.	MAX.	UNII
Cycle Time	TCYC	1.0 µs			psec
Clock Pulse Width Ø1 (Measured at Vcc -#0.2v) Ø2	PWH Ø1 PWH Ø2	430 470			nsec
Fall Time (Measured from 0.2v to Vcc - 0.2v)	T <sub>F</sub>			25	nsec
Delay Time between Clocks (Measured at 0.2v)	TD	0		-	nsec
ad /Write Timing					
CHARACTERISTIC ,	SYMBOL	MIN.	TYP.	MAX.	UNIT
Read/Write Setup Time from MCS650X	TRWS		100	300	ns
Address Setup Time from MCS650X	TADS		200	300	ns
Memory Read Access Time T <sub>R</sub> T <sub>CYC</sub> - (T <sub>ADS</sub> - T <sub>DSU</sub> - tr)	TACC			575	ns
Data Stability Time Period	T <sub>DSU</sub>	100			ns
Data Hold Time	т <sub>н</sub>	10	30		ns
Enable High Time for DBE Input	TEH	470			ns
Data Setup Time from MCS650X	TMDS		150	200	ns
RDY Setup Time	TRDY	100			ns
Bus Available Setup Time from MCS650X	TBA			470	ns
SYNC Setup Time from MCS650X	TSYNC			350	ns



## COMMON CHARACTERISTICS

#### Clocks $(\emptyset_1, \emptyset_2)$

The MCS6501 requires a two phase non-overlapping clock that runs at the Vcc voltage level.

The MCS6502, 3, 4 and 5 clocks are supplied with an internal clock generator. The frequency of these clocks is externally controlled. Details of this feature are discussed in the MCS6502 portion of this data sheet.

Address Bus  $(A_0-A_{1.5})$  (See sections on MCS6503, 4 and 5 for respective address lines on those devices.)

These outputs are TTL compatible, capable of driving one standard TTL load and 130pf.

#### Data Bus (D<sub>0</sub>-D<sub>7</sub>)

Eight pins are used for the data bus. This is a bi-directional bus, transferring data to and from the device and peripherals. The outputs are tri-state buffers capable of driving one standard TTL load and 130pf.

#### Data Bus Enable (DBE) (MCS6501 only)

This TTL compatible input allows external control of the tri-state data output buffers and will enable the microprocessor bus driver when in the high state. In normal operation DBE would be driven by the phase two  $(\emptyset_2)$  clock, thus allowing data output from microprocessor only during  $\emptyset_2$ . During the read cycle, the data bus drivers are internally disabled, becoming essentially an open circuit. To disable data bus drivers externally. DBE should be held low.

#### Ready (RDY) (MCS6501, MCS6502, MCS6505 only)

This input signal allows the user to single cycle the microprocessor on all cycles except write cycles. A negative transition to the low state during or coincident with phase one  $(\emptyset_1)$  will halt the microprocessor with the output address lines reflecting the current address being fetched. This condition will remain through a subsequent phase two  $(\emptyset_2)$  in which the Ready signal is high. This feature allows microprocessor interfacing with low speed PROMS as well as fast (max. 2 cycle) Direct Memory Access (DMA). If Ready is low during a write cycle, it is ignored until the following read operation.

#### Bus Available (BA) (MCS6501 only)

During normal operation the Bus Available signal will be in the low state, when in the high state it indicates that the microprocessor has stopped and that all buses are available. This situation will occur if the RDY signal is low and the microprocessor is not in a Write state.

#### Interrupt Request (IRQ)

This TTL level input requests that an interrupt sequence begin within the microprocessor. The microprocessor will complete the current instruction being executed before recognizing the request. At that time, the interrupt mask bit in the Status Code Register will be examined. If the interrupt mask flag is not set, the microprocessor will begin an interrupt sequence. The Program Counter and Processor Status Register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further interrupts may occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, therefore transferring program control to the memory vector located at these addresses. The RDY signal must be in the high state for any interrupt to be recognized. A  $3K\Omega$  external resistor should be used for proper wire-OR operation.

Non-Maskable Interrupt (NMI) (MCS6501, MCS6502, MCS6503 only)

A negative going edge on this input requests that a non-maskable interrupt sequence be generated within the microprocessor.

 $\overline{\rm NMI}$  is an unconditional interrupt. Following completion of the current instruction, the sequence of operations defined for IRQ will be performed, regardless of the state interrupt mask flag. The vector address loaded into the program counter, low and high, are locations FFFA and FFFB respectively. The instructions loaded at these locations causes the microprocessor to branch to a non-maskable interrupt routine in memory.

NMI also requires an external 3KΩ register to Vcc for proper wire-OR operations.

Inputs  $\overline{IRQ}$  and  $\overline{NMI}$  are hardware interrupts lines that are sampled during  $\emptyset_2$  (phase 2) and will begin the appropriate interrupt routine on the  $\emptyset_1$  (phase 1) following the completion of the current instruction.

#### Set Overflow Flag (S.O.) (MCS6502 only)

This TTL level input signal allows external control of the overflow bit in the Status Code Register.

SYNC (MCS6502 only)

This output line is provided to identify those cycles in which the microprocessor is doing an OP CODE fetch. The SYNC line goes high during  $\emptyset_1$  of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the  $\emptyset_1$  clock pulse in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.

#### Reset

This input is used to reset or start the microprocessor from a power down condition. During the time that this line is held low, writing to or from the microprocessor is inhibited. When a positive edge is detected on the input, the microprocessor will immediately begin the reset sequence.

After a system initialization time of six clock cycles, the mask interrupt flag will be set and the microprocessor will load the program counter from the memory vector locations FFFC and FFFD. This is the start location for program control.

After Vcc reaches 4.75 volts in a power up routine, reset must be held low for at least two clock cycles. At this time the R/W and (BA or SYNC) signal will become valid.

When the reset signal goes high following these two clock cycles, the microprocessor will proceed with the normal reset procedure detailed above.

**COMMON CHARACTERISTICS** 

## INSTRUCTION SET – ALPHABETIC SEQUENCE

ADC Add Memory to Accumulator with Carry AND "AND" Memory with Accumulator DEC Decrement Memory by One Decrement Index X by One DEX Shift left One Bit (Memory or Accumulator) Decrement Index Y by One ASL DEY Branch on Carry Clear Branch on Carry Set EOR "Exclusive-or" Memory with Accumulator BCC BCS Branch on Result Zero INC Increment Memory by One BEO Test Bits in Memory with Accumulator BIT INX Increment Index X by One Branch on Result Minus INY Increment Index Y by One BMI BNE Branch on Result not Zero Branch on Result Plus JMP Jump to New Location JSR Jump to New Location Saving Return Address BPL BRK Force Break Branch on Overflow Clear BVC LDA Load Accumulator with Memory BVS Branch on Overflow Set LDX Load Index X with Memory LDY Load Index Y with Memory Clear Carry Flag Clear Decimal Mode CLC CLD LSR Shift One Bit Right (Memory or Accumulator) Clear Interrupt Disable Bit Clear Overflow Flag CLI CLV NOP No Operation Compare Memory and Accumulator Compare Memory and Index X CMP

CPX

CPY

Compare Memory and Index Y

ORA "OR Memory with Accumulator

PHA Push Accumulator on Stack

- Push Processor Status on Stack PHP
- PLA Pull Accumulator from Stack PLP Pull Processor Status from Stack
- ROL Rotate One Bit Left (Memory or Accumulator) Return from Interrupt RTT
- RTS Return from Subroutine
- SBC Subtract Memory from Accumulator with Borrow
- SEC Set Carry Flag Set Decimal Mode SED
- SEI
- Set Interrupt Disable Status Store Accumulator in Memory STA
- STX Store Index X in Memory STY Store Index Y in Memory
- TAX Transfer Accumulator to Index X
- TAY Transfer Accumulator to Index 1
- TSX Transfer Stack Pointer to Index X
- Transfer Index X to Accumulator Transfer Index X to Stack Pointer TXA TXS
- Transfer Index Y to Accumulator

#### ADDRESSING MODES

- ACCUMULATOR ADDRESSING This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.
- IMMEDIATE ADDRESSING In immediate addressing, the operand is contained in the second byte of the instruction, with no further memory addressing required.

ABSOLUTE ADDRESSING - In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Thus, the absolute addressing mode allows access to the entire 65K bytes of addressable memory.

- ZERO PAGE ADDRESSING The zero page instructions allow for shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code efficiency.
- INDEXED ZERO PAGE ADDRESSING (X, Y indexing) This form of addressing is used in conjunction with the index register and is referred to as "Zero Page, X" or "Zero Page, Y". The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally due to the "Zero Page" addressing nature of this mode, no carry is added to the high order 8 bits of memory and crossing of page boundaries does not occur.
- INDEXED ABSOLUTE ADDRESSING (X, Y indexing) This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X", and "Absolute, Y". The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.
- IMPLIED ADDRESSING In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.
- RELATIVE ADDRESSING Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is -128 to +127 bytes from the next instruction.

- INDEXED INDIRECT ADDRESSING In indexed indirect addressing (referred to as (Indirect,X)), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents is the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.
- INDIRECT INDEXED ADDRESSING In indirect indexed addressing (referred to as (Indirect),Y), the second byte of the instruction points to a memory location in page zero. The contents of this memory location is added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.
- ABSOLUTE INDIRECT The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location is contained in the third byte of the instruction. The contents of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter.



AND	AAM+A (1)	29	2	2	2D	4	3	25	3	2							21	6	2 3	1	5 2	3	5 4	2	30	4	3	39	9 4	3											1	1	-	-	-		1
ASL	C+(7)+0				ØE	6	3	86	5	2	ØA	2	1									16	6	2	16	E 7	3														1	1	1	-	-	-	
BCC	BRANCH ON C=@ (2)																														90	2	2	L							-	-	-	-	-	-	
BCS	BRANCH ON C=1 (2)								<u>)</u>					L		_	-		1												B	2	2	L							-	-	-	-	-	-	
BEQ	BRANCH ON Z=1 (2)	_																							1	1					F	2	2								-	-	-	-	-	-	
BIT	AAM .				2C	4	3	24	3	2																															м,	1	-	2	-	Me	
BMI	BRANCH ON N=1 (2)																														30	2	2								-	-	-	-	-	-	
BNE	BRANCH ON Z=0 (2)																				1					1					D	8 2	2								-	-	-	-	-	-	
BPL	BRANCH ON N=0 (2)					_								_		_		_	-	-	-	+		-	+	-	-	+	-	-	10	2	2	⊢	1	4	+	+	-	_	-	-	-	-	-	-	4
BRK	(See Fig. 1)													00	7	1												1									Т				-	-	-	'	-	-	Т
BVC	BRANCH ON V=0 (2)																														50	2	2								-	-	-	-	-	-	
BVS	BRANCH ON V=1 (2)																														76	2	2								-	-		-	-	-	
CLC	0+0													18	2	1																									-	-		-		-	
CLD	0+0	-				-	-	-						DB	2	1	-	+	+	+	+	+	-	+	+	+	+	+	+	-	+	+	+	╋	+	+	+	+	+	-	-	-	-			-	+
CLV	0													20	2																Г										-	-	-		-		
CMP	A_M	C0	2	2	CD		2	C6	2	2				50	-	1	C1		2 0				5 4	2	0		1	0		3											5		,	2			
CPX	X-M	Ea	2		EC	1	3	EA	2	2								°	1	"	1			1	1	1	1	1	1	1											Ľ,	,	;	0			
CPY	Y-M	CO	2	2	cc	4	3	CA	3	2																															Ľ	;	,	2	_	_	
DEC	M-1 + M	F	-		CE	6	3	C6	5	2		-						+	+	+	+	D	6 6	2	D	E 7	3		+	+	t	+	+	1-	+	+	+	1		-	1	1	-	-	-	-	1
DEX	X-1 + X					24	1		-					CA												1															1	,	-	-	-	-	
DEY	Y-1 + Y													88																											1	1	-	-	-	-	
EOR	A + M + A (1)	49	2	2	4D	4	3	45	3	2							41	6	2 5	1	5 3	5	5 4	2	50	0 4	3	59	4	3											1	1	-	-	-	-	
INC	M+1 + M				EE	6	3	E6	5	2												F	6 6	2	F	E 7	3										., 				V	1	-	-	-	-	
INX	X+1 + X													E8	2	1	0.55											T			T			Т	Т	Τ	Т					1	-	-	-	-	
INY	Y+1+Y													C8	2	1																									1	1	-	-	-	-	
JMP	JUMP TO NEW LOC.				4C	3	3																											60	5	1	3				-	-	-	-	-	-	
JSR	(See Fig. 2)JUMP SUB				20	6	3																																		-	-	-	-	-	-	
LDA	M + A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2 8	1	5	8	5 4	2	B	D 4	3	89	9 4	3										_	1	1	-	-	-	-	
		-			_																					_																					
	1	IM	AEDI	ATE	AB	SOLL	TE	SEI	ROP	AGE	1	CCI	JM.	IN	PLIE	D	()	ND,	0	(1)	(D), Y	1	PAG	SE, X		ABS	, X		ABS	Y.		RELA	TIVE	1	NDI	REC	T	2,9	AGE	<b>Y</b>		CON	DIT	ION	COD	DES	5
And an and the second second					OP	N	1 #	OP	N	#	OF	N	#	OP	N	#	OD	R.I	# 4	OP	N	t In	DP N	1 #		ND N	#	lo	PN	#	0	PN	N #	0	PN	4	ŧ.	OP	N	#	I N	2	C		D	• •	1
MNEMONIC	OPERATION	OP	N		0,			-			-	-	1	-			UP		77	-	-	-	-		-	1	1"	-				-			-		-	-			- "						-
MNEMONIC LDX	OPERATION M + X (1	A	2	2	AE	4	3	A6	3	2							UP		-								1	B	E	3				Τ			E	<b>B6</b>	4	2					-		-
MNEMONIC L D X L D Y	OPERATION           M + X         (1)           M + Y         (1)	OP A3 A0	N 2 2	2 2	AE	4	3	A6 A4	3	2 2							UP		<u> </u>			8	14 4	2	BI	c 4	3	B	E	3							E	B6	4	2		*			1 1		1
L D X L D Y L S R	OPERATION           M + X         (1)           M + Y         (1)           Q+(1)         (1)           Q+(2)         (1)           DOC         (1)	OP A3	N 2 2	2 2	AE AC 4E	4 4 6	3 3 3	A6 A4 46	3 3 5	2 2 2	4A	2	1				UP		#- 1			8	14 4 6 6	2	8	C 4	3	B	E	3							E	86	4	2					(11		
MNEMONIC LDX LDY LSR NOP	OPERATION           M + X         (1)           M + Y         (1)           Q+(2)         (3)           OPERATION         (1)           AV M + A         (1)	A	N 2 2 2	2 2 2	AE AC 4E	4 4 6	333	A6 A4 46	3 3 5	2 2 2 2	4A	2	1	EA	2	1						8	6 6	2	8	C 4	3	BI	E	3							E	86	4	2					1 1 1 1		
MNEMONIC LDX LDY LSR NOP ORA	OPERATION           M + X         (1)           M + Y         (1)           Q+(1)         (	0P A3 A0	N 2 2 2	2 2 2 2	AE AC 4E	4 4 6 4	3 3 3 3	A6 A4 46 Ø5	3 3 5 3	2 2 2 2	4A	2	1	EA	2	1	01	6	2 1	11	5	8	4 4 6 6 5 4	2 2	BI 51	C 4 E 7 D 4	3	8	e 4	3							E	86	4	2					1111	-	
MNEMONIC LDX LDY LSR NOP ORA PHA PHP	OPERATION           M + X         (1)           M + Y         (1)           Q+(1	0P A3 A9	N 2 2 2	2 2 2	AE AC 4E	4 4 6 4	3 3 3 3	A6 A4 46 Ø 5	3 3 5 3	2 2 2 2 2	4.4	2	1	EA 48 0 8	2	1	01	6	2 1	11	5	8	4 4 6 6 5 4	2 2 2	BI 51	C 4 E 7 D 4	3	81	e 4	3							E	86	4	2							
MNEMONIC LDX LDY LSR NOP ORA PHA PHP PLA	$\begin{array}{c} \hline \textbf{OPERATION} \\ \hline \textbf{M} + \textbf{X} & (1) \\ \hline \textbf{M} + \textbf{Y} & (1) \\ \hline \textbf{q} + [\overrightarrow{1} \ \overrightarrow{1}] + \textbf{C} \\ \hline \textbf{NO} \ \textbf{OPERATION} \\ \hline \textbf{AV M} + \textbf{A} \\ \hline \textbf{A} - \textbf{M}_{S} \ \textbf{S} - 1 \rightarrow \textbf{S} \\ \hline \textbf{P} - \textbf{M}_{S} \ \textbf{S} - 1 \rightarrow \textbf{S} \\ \hline \textbf{S} + 1 \rightarrow \textbf{S}  \textbf{M} \rightarrow \textbf{A} \end{array}$	0P A3 A0	N 2 2 2	2 2 2	AE AC 4E	4 4 6 4	3333	A6 A4 46 Ø5	3 3 5 3	2 2 2 2 2	4.4	2	1	EA 48 0 8 68	2 3 3 4	1 1 1	01	6	2 1	11	5	8	14 4 6 6 5 4	2	BI 51	C 4 E 7 D 4	3	8	e 4	3							E	86	4	2							
MNEMONIC LDX LDY LSR NOP ORA PHA PHP PLA PLP	OPERATION           M + X         (1)           M + Y         (1)           get         SP-C           NO OPERATION         AV M + A           A - Ms         S-1-+S           S^1-+S         Mi-+A           S^1-+S         Mi-+A	0P A3 A0	N 2 2 2	2222	AE AC 4E	4 4 6 4	3 3 3 3	A6 A4 46 Ø 5	335	2 2 2 2 2	4A	2	1	EA 48 0 8 68 28	2 3 3 4 4	1 1 1 1	01	6	2 1	n	5	B 5	14 4 6 6 5 4	2 2	9 BI	C 4 E 7 D 4	3	81	E 4	3	1000 Diale						E	86	4	2			/	-	- - - - ED)		
I D X L D X L D Y L S R N O P O R A P H A P H P P L A P L P R O L	$\begin{array}{c} \hline \textbf{OPERATION} \\ M \rightarrow X & (1) \\ M \rightarrow Y & (1) \\ q \leftarrow S \rightarrow C \\ NO OPERATION \\ A \lor M + A \\ A \leftarrow M_{5}  S - 1 \rightarrow S \\ S \rightarrow 1 \rightarrow S  M_{5} \rightarrow P \\ S \rightarrow 1 \rightarrow S  M_{5} \rightarrow P \\ S \rightarrow 1 \rightarrow S  M_{5} \rightarrow P \\ \hline \end{tabular}$	0P A3 A0	N 2 2 2	222	AE AC 4E Ø D	4 4 6 4 6 6	3 3 3 3 3	A6 A4 46 05	33533	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	4A 2A	2	1	EA 48 08 68 28	2 3 3 4 4	1 1 1 1 1	01	6	2 1	n	5	B 5 2 1	14 4 6 6 5 4	2 2 2 2	2 31	C 4 E 7 D 4	3	8	E 4	3	100 m						E	B6	4	2	· · · · · · · · · · · · · · · · · · ·			TOP			
MNEMONIC LDX LDY LSR NOP ORA PHA PHP PLA PLP ROL RTI	$\begin{array}{c} 0 \text{ DFRATION} \\ M + X & (1) \\ M + Y & (1) \\ 0 \text{ C} & \text{Sec} \\ NO OFERATION \\ AV M + A \\ A \rightarrow Ms & S-1 \rightarrow S \\ S^{+}1 \rightarrow S & Ms \rightarrow P \\ S^{+}1 \rightarrow S & Ms \rightarrow P \\ S^{+}1 \rightarrow S & Ms \rightarrow P \\ S^{-} \text{ C} & \text{ C} \text{ C} \text{ C} \text{ C} \text{ C} \\ S^{-} \text{ C} $	0P A1 A0	N 2 2 2	2 2 2 2	AE AC 4E Ø D	4 4 6 4 6	3 3 3 3 3 3	A6 A4 46 05	3 3 5 3 3	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	4A 2A	2	1	EA 48 68 28	2 3 3 4 4 6	1 1 1 1 1 1	01	6	2	11	5	B 5 2 1	4 4 6 6 5 4 6 6	2 2 2	2 31	C 4 E 7 D 4	3	8	E 4	3							E	B6	4	2	· · · · · · · · · · · · · · · · · · ·	· · · · · · · · · · · · · · · · · · ·	RES V	TOP			
MNEMONIC LDX LDY LSR NOP ORA PHA PHP PLA PLP ROL RTI RTS	$\begin{array}{c} \hline \textbf{DPERATION} \\ \hline \textbf{M} + \textbf{X} & (1) \\ \hline \textbf{M} + \textbf{Y} & (1) \\ \hline \textbf{g} + \boxed{\begin{array}{c} \hline \textbf{g} + \textbf{C} \\ \hline \textbf{NO} \mbox{ OPERATION} \\ \hline \textbf{AV M} + \textbf{A} \\ \hline \textbf{A} - \textbf{M}_{S} \mbox{ S} - 1 \rightarrow \textbf{S} \\ \hline \textbf{S} + 1 \rightarrow \textbf{S} \mbox{ M}_{S} \mbox{ S} - 1 \rightarrow \textbf{S} \\ \hline \textbf{S} + 1 \rightarrow \textbf{S} \mbox{ M}_{S} \rightarrow \textbf{P} \\ \hline \textbf{g} + \boxed{\begin{array}{c} \hline \textbf{G} = \textbf{F}_{B} \mbox{ (I)} \\ \hline \textbf{S} = \textbf{F}_{B} \mbox{ (I)} \mbox{ NIT} \\ \hline \textbf{S} = \textbf{F}_{B} \mbox{ (I)} \mbox{ RT NJI} \\ \hline \textbf{S} = \textbf{F}_{B} \mbox{ (I)} \mbox{ RT NJI} \\ \hline \textbf{S} = \textbf{F}_{B} \mbox{ (I)} \mbox{ RT NJI} \\ \hline \textbf{S} = \textbf{F}_{B} \mbox{ (I)} \mbox{ RT NJI} \\ \hline \textbf{S} = \textbf{F}_{B} \mbox{ (I)} \mbox{ RT NJI} \\ \hline \textbf{S} = \textbf{F}_{B} \mbox{ (I)} \mbox{ RT NJI} \\ \hline \textbf{S} = \textbf{F}_{B} \mbox{ (I)} \mbox{ RT NJI} \\ \hline \textbf{S} = \textbf{F}_{B} \mbox{ (I)} \mbox{ RT NJI} \\ \hline \textbf{S} = \textbf{F}_{B} \mbox{ (I)} \mbox{ RT NJI} \\ \hline \textbf{S} = \textbf{F}_{B} \mbox{ (I)} \mbox{ RT NJI} \\ \hline \textbf{S} = \textbf{F}_{B} \mbox{ (I)} \mbox{ RT NJI} \\ \hline \textbf{S} = \textbf{F}_{B} \mbox{ (I)} \mbox{ RT NJI} \\ \hline \textbf{S} = \textbf{F}_{B} \mbox{ (I)} \mbox{ RT NJI} \\ \hline \textbf{S} = \textbf{F}_{B} \mbox{ (I)} \mbox{ RT NJI} \\ \hline \textbf{S} = \textbf{F}_{B} \mbox{ (I)} \mbox{ RT NJI} \\ \hline \textbf{S} = \textbf{F}_{B} \mbox{ (I)} \mbox{ RT NJI} \\ \hline \textbf{S} = \textbf{F}_{B} \mbox{ (I)} \mbox{ RT NJI} \\ \hline \textbf{S} = \textbf{F}_{B} \mbox{ (I)} \mbox{ RT NJI} \\ \hline \textbf{S} = \textbf{F}_{B} \mbox{ (I)} \mbox{ RT NJI} \\ \hline \textbf{S} = \textbf{F}_{B} \mbox{ (I)} \mbox{ RT NJI} \\ \hline \textbf{S} = \textbf{F}_{B} \mbox{ (I)} \mbox{ RT NJI} \\ \hline \textbf{S} = \textbf{F}_{B} \mbox{ (I)} \mbox{ RT NJI} \\ \hline \textbf{S} = \textbf{F}_{B} \mbox{ (I)} $	0P A3 09	N 2 2 2	2 2 2 2	4E 80 D 2E	4 4 6 4	3 3 3 3 3	A6 A4 46 05 26	33533	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	4A 2A	2	1	48 0 8 68 28 40 60	2 3 3 4 4 6 6	1 1 1 1 1 1 1 1 1	01	6	2	11	5	B 5 2 1	14 4 6 6 5 4 6 6	2 2 2	2 31	C 4 E 7 D 4	3	8	E 4	3							E	86	4	2	· · · · · · · · · · · · · · · · · · ·	· · · · · · · · · · · · · · · · · · ·	RES V	TOF			
INNEMONIC LDX LDY LSR NOP ORA PHA PHP PLA PLP ROL RTI RTS SBC	OPERATION           M + X         (1)           M + Y         (1) $M + X$ (1)           M + Q         (1) $M + X$ (1)           NO OPERATION         AV $AV M + A$ A $A + M + S - 1 \rightarrow S$ S - 1 $\rightarrow S$ $S + 1 \rightarrow S$ $M_1 \rightarrow A$ $A - M - C$ $A$ $A - M - C$ $A$	0P A3 09 09	N 2 2 2 2 2	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	4E 4E 2E ED	4 6 6 4	3 3 3 3 3 3	A6 A4 46 05 26 E5	3 3 5 3 5 5	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	4A 2A	2	1	48 08 68 28 40 60	2 3 3 4 4 6 6	1 1 1 1 1 1	01 E1	6	2	11 F1	5	8 5 2 1 3	14 4 6 6 5 4 6 6	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	2 31	C 4 E 7 D 4 E 7	3	8 19 8 19	e 4 9 4	1 3	3						E	86	4	2	· · · · · · · · · · · · · · · · · · ·	· · · · · · · · · · · · · · · · · · ·	/	TOR	= = = = = = = = = = = = = = = = = = =		
INNEMONIC LDX LDY LSR NOP ORA PHA PHP PLA PLP RTI RTS SBC SEC	$\begin{array}{c} \hline \textbf{OPERATION} \\ \textbf{M} + \textbf{X} & (1) \\ \textbf{M} + \textbf{Y} & (1) \\ \hline \textbf{g} + \boxed{}  \textbf{S} + \textbf{C} \\ \hline \textbf{NO OPERATION} \\ \textbf{AV M} + \textbf{A} \\ \textbf{A} - \textbf{M} & \textbf{S} - 1 \rightarrow \textbf{S} \\ \hline \textbf{S} + 1 \rightarrow \textbf{S} & \textbf{M}_1 \rightarrow \textbf{A} \\ \hline \textbf{S} + 1 \rightarrow \textbf{S} & \textbf{M}_1 \rightarrow \textbf{A} \\ \hline \textbf{S} + 1 \rightarrow \textbf{S} & \textbf{M}_1 \rightarrow \textbf{A} \\ \hline \textbf{S} + 1 \rightarrow \textbf{S} & \textbf{M}_2 \rightarrow \textbf{P} \\ \hline \textbf{Gee Fig. 2) RTRN SUB} \\ \textbf{A} - \textbf{M} - \textbf{C} & \textbf{A} & (1) \\ \textbf{I} + \textbf{C} \end{array}$	0P A3 09 09	N 2 2 2 2 2 2	2 2 2 2 2 2	4E 9 D 2E	4 4 6 4 6	3 3 3 3 3 3	A6 A4 46 05 26 E5	3 3 5 3 5 3	2 2 2 2 2 2 2 2 2	4A 2A	2	1	EA 48 68 28 40 60 38	2 3 3 4 4 6 6 6 2	1 1 1 1 1 1 1 1 1 1	01 E1	6	2	F1	5	8 5 2 1 3 2 F	14 4 6 6 5 4 6 6	2 2 2 2	2 31	C 4 E 7 D 4	3 3 3 3	8 19 8 19	e 4	1 3	3						E	86	4	2	· · · · · · · · · · · · · · · · · · ·	· · · · · · · · · · · · · · · · · · ·	/	TOP	= = = = = = = = = = = = = = = = = = =		
UNNEMONIC LDX LDY LSR NOPA PHA PHP PLA PLP ROL RTI RTS SBC SEC SED	$\begin{array}{c} 0 \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ $	0P A1 09 09	N 2 2 2 2 2	2 2 2 2 2 2	4E 4C 4E 2E	4 4 6 4	3 3 3 3 3 3	A6 A4 46 05 26 E5	3 3 5 3 5	2 2 2 2 2 2 2 2 2	4A 2A	2	1	EA 48 68 28 40 60 38 F8	2 3 3 4 4 6 6 2 2	1 1 1 1 1 1 1 1 1	01 E1	6	2	11 F1	5	8 5 2 1 3 3	14 4 6 6 5 4 6 6	2 2 2 2	2 31	C 4 E 7 D 4	3	8 19 19 19 19 19 19 19 19 19 19 19 19 19	e 4	1 3	3						E	86	4	2	· · · · · · · · · · · · · · · · · · ·	· · · · · · · · · · · · · · · · · · ·		TOP			
INNEMONIC LDX LDY LSR NOP ORA PHA PHP PLA PLP ROL RTI RTS SBC SEC SED SEI	OPERATION           M + X         (1)           M + Y         11           g+C         Six           NO OPERATION         AV           AV M + A         A           A-Mix         S-1-+S           Six+S         Mi-→A           Si++S         Mi-→A           Si++S         Mi-→A           Six++S         Mi-→A           A-M-C         A           Six+++S         Mi++A           Six++++S	0P A1 0 0 9 0 9	N 2 2 2 2 2	2 2 2 2 2 2	4E 4C 4E 2E ED	4 4 6 4 6	3 3 3 3 3 3	A6 A4 46 05 26 E5	3 3 5 3 5	2 2 2 2 2 2 2 2	4A 2A	2	1	EA 48 08 68 28 40 60 38 F8 78	2 3 3 4 4 6 6 6 2 2 2 2	1 1 1 1 1 1 1 1 1	01 E1	6	2	F1	5	2 1 3 2 F	4 4 6 6 6 6 6 6	2 2 2	2 31	C 4 E 7 D 4	3	8 19 8 19	E 4	i 3 i 3	3						E	86	4	2	· · · · · · · · · · · · · · · · · · ·	· · · · · · · · · · · · · · · · · · ·	/	TOP	= = = = = = = = = = = = = = = = = = =		
UNREMONIC LDX LDY LSY NOP ORA PHA PHP PLA ROL RTI RTS SBC SEC SEC SEI SEI STA	OPERATION           M + X         (1)           M + Y         (1)           Q+C         Sec           NO OPERATION         AV M + A           A - Mis         S-1-+S           S*1-+S         Mis-+A           S*1+S         Mis-+A           S*1+S         Mis-+A           S*1+S         Mis-+A           S*6         Fig. 21)         RTRN. NUL           Gee Fig. 21)         RTRN SUB         A-M-C         A           A - M-C         A         (1)         1 + C           1 + D         1 + 1         A + M         (1)	0P A1 A0 09	N 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	2 2 2 2 2 2	4E 4C 4E 2E ED	4 4 6 4 6	3 3 3 3 3 3 3	A6 A4 46 05 26 E5	3 3 5 3 5 3 3	2 2 2 2 2 2 2 2 2 2 2 2 2 2	4A 2A	2	1	EA 48 68 28 40 60 38 F8 78	2 3 3 4 4 6 6 6 2 2 2 2	1 1 1 1 1 1 1 1 1 1	©1 E1	6	2	F1	5	2 1 3 2 5 3 3 2 7	14 4 6 6 5 4 6 6 6 6 6 6 7 7 8 7 8 7 8 7 8 7 8	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	2 31 2 F	C 4 E 7 D 4 E 7	3	6 19 6 19 6 19 7 19	94	i 3 i 3	3						E	86	4	2	· · · · · · · · · · · · · · · · · · ·	· · · · · · · · · · · · · · · · · · ·	RES' V RES' 1 1	TOP	= - - - ED) - - 1		
UNREMONIC LDX LDY LSR PHA PHP PLA PLP LA PLP LA RTI RTS SBC SEC SEC SEC SEI STA STX	$\begin{array}{c} \hline \textbf{DPERATION} \\ \textbf{M} + \textbf{X} & (1) \\ \textbf{M} + \textbf{Y} & (1) \\ \hline \textbf{q} + \boxed{\begin{matrix} \textbf{D} \\ \textbf{P} \end{matrix}} \\ \textbf{NO OPERATION} \\ \textbf{AV M} + \textbf{A} \\ \textbf{A} \rightarrow \textbf{M}_{S} & \textbf{S} - \textbf{I} \rightarrow \textbf{S} \\ \textbf{S} + \textbf{I} \rightarrow \textbf{S} & \textbf{M}_{S} \rightarrow \textbf{A} \\ \textbf{S} + \textbf{I} \rightarrow \textbf{S} & \textbf{M}_{S} \rightarrow \textbf{A} \\ \textbf{S} + \textbf{I} \rightarrow \textbf{S} & \textbf{M}_{S} \rightarrow \textbf{A} \\ \textbf{S} + \textbf{I} \rightarrow \textbf{S} & \textbf{M}_{S} \rightarrow \textbf{A} \\ \textbf{S} + \textbf{I} \rightarrow \textbf{S} & \textbf{M}_{S} \rightarrow \textbf{A} \\ \textbf{S} + \textbf{I} \Rightarrow \textbf{S} & \textbf{M}_{S} \rightarrow \textbf{A} \\ \textbf{S} + \textbf{I} \Rightarrow \textbf{S} & \textbf{M}_{S} \rightarrow \textbf{A} \\ \textbf{S} + \textbf{I} \Rightarrow \textbf{S} & \textbf{M}_{S} \rightarrow \textbf{A} \\ \textbf{S} + \textbf{I} \Rightarrow \textbf{S} & \textbf{I} \textbf{N} \textbf{T} \\ \textbf{S} \text{ er Fig. 2) RTRN INT \\ \textbf{S} \text{ er Fig. 2) RTRN U \\ \textbf{A} - \textbf{M} = \textbf{C} & \textbf{I} \\ \textbf{I} + \textbf{C} \\ \textbf{I} + \textbf{D} \\ \textbf{I} + \textbf{I} \\ \textbf{A} + \textbf{M} \\ \textbf{X} + \textbf{M} \end{array}$	0P A1 A0 09	N 2 2 2 2 2 2	2 2 2 2 2 2	4E 4C 4E 8D 8D 8E	4 4 6 4 6 4 4	3 3 3 3 3 3 3 3 3 3	A6 A4 46 05 26 E5 85 86	3 3 5 3 5 3 3 3 3	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	4A 2A	2	1	48 08 68 28 40 60 38 F8 78	2 3 3 4 4 6 6 2 2 2 2	1 1 1 1 1 1 1	©1 E1	6 6	2	F1	5	8 5 2 1 3 3 2 F	6 6 5 4 6 4	2 2 2 5 5 1 4 2	2 31 2 F	E 7 E 7 E 7	3 3 1 3 1 3	8 19 8 19 8 5 91	9 4 9 4	i 3 i 3	3						5	996	4	2	· · · · · · · · · · · · · · · · · · ·		/	TOP	= = = = = = = = = = = = = = = = = = =		
UNREMONIC LDX LDX LSR NOP ORA PHA PHA PLP ROL RTI RTS SBC SEC SEC SEC SEC SEI STX STX	$\begin{array}{c} \hline \textbf{DPERATION} \\ \textbf{M} + \textbf{X} & (1) \\ \textbf{M} + \textbf{Y} & (1) \\ \textbf{g} + \boxed{\begin{array}{c} \hline \end{array}} \\ \textbf{NO} OPERATION \\ \textbf{AV M} + \textbf{A} \\ \hline \textbf{AV M} + \textbf{A} \\ \textbf{AV M} + \textbf{A} \\ \textbf{AV M} + \textbf{A} \\ \textbf{S} + 1 \rightarrow \textbf{S} \\ \textbf{M} + \textbf{S} \\ \textbf{S} + 1 \rightarrow \textbf{S} \\ \textbf{M} + \textbf{S} \\ \textbf{S} + 1 \rightarrow \textbf{S} \\ \textbf{M} + \textbf{M} \\ \textbf{S} + \textbf{M} \\ \textbf{M} \\$	0P A3 09 09	N 2 2 2 2 2 2 2	2 2 2 2 2 2	4E 4E 22E ED 8D 8E 8C	4 4 6 4 6 4 4 4 4	3 3 3 3 3 3 3 3 3 3 3	A6 A4 46 05 26 E5 85 86 84	3 3 5 3 5 3 3 3 3 3 3	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	4A 2A	2	,	48 08 68 28 40 60 38 F8 78	2 3 3 4 4 6 6 2 2 2 2	1 1 1 1 1 1 1 1	©1 E1	6	2	F1	5	2 1 3 2 F	6 6 6 5 4 6 5 4 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6	2 2 2 2 5 2 4 2 4 2	2 31 2 5 2 5 2 5 5 1 1	E 7 E 7	3	6 99	94	1 3 1 3	3						E	996	4	2	· · · · · · · · · · · · · · · · · · ·	· · · · · · · · · · · · · · · · · · ·	/	TOP			
UNREMONIC LDX LDX LSR NOP ORA PHP PLA PLP RTI RTS SBC SEC SEC SEI STA STX STY TAX	$\begin{array}{c} 0 \mbox{ $PFRATION$$} \\  $M + X$ (1) $$$ $$$ $$$ $$$ $$$ $$$ $$$ $$$ $$$ $$	0P A3 09 09	N 2 2 2 2 2 2	2 2 2 2 2	8D 8E 8C	4 4 6 4 6 4 4 4 4	3 3 3 3 3 3 3 3 3 3 3	A6 A4 46 85 26 E5 85 86 84	3 3 5 3 5 3 3 3 3 3 3	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	4A 2A	2	1	EA 48 68 28 40 60 38 F8 78 AA	2 3 3 4 4 6 6 2 2 2 2 2	1 1 1 1 1 1 1 1 1	01 E1	6	2	11 F1	5	2 1 3 3 2 F	14 4 6 6 6 5 4 66 6 5 4 15 4 15 4	2 2 2 2 5 2 4 2 4 2	2 31 2 5 9	C 4 E 7 D 4	3	8 19	94	1 3 1 3	3						E	996	4	2		· · · · · · · · · · · · · · · · · · ·	RES' 7 8 8 1 1 - - - - - - - - - - - - - - - -	TOP	ED)		
UNREMONIC LDX LDX LSR NOP ORA PHA PLA PLP ROL RTL RTS SBC SEC SEC SEC SEI STA STX TAX TAX	OPERATION           M + X         (1)           M + Y         (1)           Q+C         Six           NO OPERATION         AV           AV M + A         A           A-+ Ms         S-1-+S           Six++S         Mi-+A           A + M         X + M           X + M         X + M           X + M         X + X           A + Y         A + Y	0P A3 09 09	N 2 2 2 2	2 2 2 2 2 2	4E 0 D 2E ED 8D 8E 8C	4 4 6 4 6 4 4 4 4 4	3 3 3 3 3 3 3 3 3 3 3	A6 A4 46 95 26 E5 85 86 84	3 3 5 3 5 3 3 3 3 3 3	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	4A 2A	2	1	EA 48 68 68 28 40 60 38 F8 78 78 AA	2 3 3 4 4 6 6 6 2 2 2 2 2 2 2 2	1 1 1 1 1 1 1 1 1 1	©1	6	2	F1	5	2 1 3 2 F	6 6 6 6 95 4	1 2 2 2 5 2 5 2 1 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	2 31 2 F	E 7	3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	8 99	9 4	1 3 1 3	3						Ę	996	4	2	2 2 2 1 2 1 1 1 2 1 2 1 2 1 2 1 2 1 2	2 2 3 1 3 1 1 1 2 3 2 1 3 1 1 1 1 1 3 3	RES (3 1 	TOF	ED)		
UNREMONIC LDX LDX LSR NOP ORA PHA PLA PLP ROL RTI SBC SEC SEC SEC SEC SEC SEC SEC STA STX STX STX STX	$\begin{array}{c} 0 \text{ DPERATION} \\ M + X & (1) \\ M + Y & 11 \\ g + $	0P A3 09 09	N 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	2 2 2 2 2	4E 4E 8D 8D 8D 8E 8C	4 4 6 4 6 4	3 3 3 3 3 3 3 3 3 3 3	A6 A4 46 0 5 26 E5 85 86 84	3 3 5 3 5 3 3 3 3 3 3	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	4A 2A	2	1	48 08 68 28 40 60 38 F8 78 78 AA AB	2 3 3 4 4 4 6 6 6 2 2 2 2 2 2 2 2 2 2 2 2	1 1 1 1 1 1 1 1 1 1 1 1 1 1	©1 E1	6	2 1	F1	5	2 1 3 2 F	6 6 6 6 95 4	2 2 2 3 3 4 2 4 2 4 2 4 2 4 2 4 2 4 2 4	2 31 2 31 2 5 1 1	E 7	3	8 F1	9 4	4 3 5 3	3						E	996	4	2				TOF	= = = = = = = = = = = = = = = = = = =		
UNREMONIC LDX LDX LSR NOP ORA PHA PLA PLP ROL RTI SBC SEC SEC SEC SEC SEC SEC SET A STX STX STX STX STX STX	DPERATION           M + X         (1)           M + Y         (1)           Q+C         Sec           NO OPERATION         AV           AV M + A         A           A	0P A3 09 09	N 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	2 2 2 2	4E 4E 8D 2E 8D 8D 8E 8C	4 4 6 4 6	3 3 3 3 3 3 3 3 3 3	A6 A4 46 0 5 26 E5 85 86 84	3 3 5 3 5 3 3 3 3 3	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	4A 2A	2	1	EA 48 68 68 28 40 60 38 F8 78 78 AA AB BA	2 3 3 4 4 6 6 6 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	1 1 1 1 1 1 1 1 1 1 1 1 1 1	©1 E1	6	2 1	F1	5	2 1 3 2 F	6 6 6 6 75 4 95 4	2 2 2 5 1 2 2 1 2 2 2 2 2 2 2 2 2 2 2 2	2 31 2 F	E 7	3 3 3 3 3 3 3 3 3 3 3 3 3	6 19	94	1 3 1 3	3						5	996	4	2		· · · · · · · · · · · · · · · · · · ·	RES' V RES' 1 (3) 1 	TOF			
UNREMONIC LDX LDX LSR NOP ORA PHA PLA PLP ROL RTI RTS SBC SEC SEC SEC SEC SET STX STX STX TAX TAX TXA TXA	OPERATION           M + X         (1)           M + Y         (1)           g+[	0P A1 0 0 0 0 0 0 0 0	N 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	2 2 2 2	4E 4E 8D 2E 8D 8D 8D 8D 8D 8D	4 4 6 4 6 4 4 4 4	3 3 3 3 3 3 3 3 3 3 3	A6 A4 46 05 26 E5 85 86 84	3 3 5 3 5 3 3 3 3 3	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	4A 2A	2	,	48 08 68 28 40 60 38 F8 78 78 AA AB ABA BA	2 3 3 4 4 6 6 6 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	©1 81	6 6	2	91	5	2 1 3 2 F	6 6 5 4 6 6	2 2 2 5 5 1 2 1 2	2 31 2 F	E 7	· 3	8 99	94	i 3	3						Ę	996	4	2		2 2 2 1 2 1 1 2 2 2 1 2 1 1 1 1 2 2 2 1 2 1 2 1 2 2 2 1 2 1 2 2 2 1 2 1 2 1 2 2 2 1 2 1 2 2 2 2 1 2 2 2 2 1 2		TOF	=		
UNREMONIC LDX LDX LSR NOP ORA PHP PLA PLP ROL RTI RTS SBC SEC SEC SEC SEI STA STX TAX TAY TSX TXX TXX TXX	OPERATION           M + X         (1)           M + Y         (1)           Q+D         Six           NO OPERATION         AV           Av M + A         A           AMs         S-1-+S           Six1-+S         MisA           Six1-+S         MisA           Six1-+	0P A1 A0 09	N 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	2 2 2 2	AE AC 4E 8D 2E ED 8D 8E 8C	4 4 6 4 6 4 4 4 4 4	3 3 3 3 3 3 3 3 3 3 3	A6 A4 46 05 26 E5 85 86 84	3 3 5 3 3 3 3 3 3	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	4A 2A	2	1	48 08 68 28 40 60 38 F8 78 78 AA AB BA BA BA BA 9A 98	2 3 3 4 4 6 6 6 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	©1	6 6	2	91	5	2 1 3 2 F	6 6 5 4 6 6 95 4	2 2 2 2 5 2 1 2 1 2 1 2 1 2	2 31 2 5 9 2 7	E 7	· 3	8 19 8 99	9 4	1 3 1 3	3							996	4	2		2 2 2 1 2 1 1 2 2 2 1 2 1 1 1 1 2 2 2 1 2 1 2 1 2 2 2 1 2 1 2 1 2 2 2 1 2 1 2 1 2 2 2 1 2 1 2 1 2 2 2 2 1 2		TOF	ED)		
ID X           L D X           L D X           L D X           L S R           N O P           O R A           P H A           P L A           P L A           S B C           S B C           S E I           S T A           S T A           S T Y           T A X           T X S           T X S           T Y A           (1) AOC	OPERATION           M + X         (1)           M + Y         (1)           Q+C         Six           NO OPERATION         Av           Av M + A         A           A-MK, S-1-+S         Six++S           Six++S         Mi-+A           Six++S         Mi-+A           Six++S         Mi-+A           Six++S         Mi-+A           Six++S         Mi-+A           A-M-C         A           1 + C         1           1 + C         1           1 + D         1 + 1           A + M         Y + M           A + X         A           A + Y         S           Y + A         X           Y + A         X           Y + A         X           D TO 'N'' IF PAGE BOULD	0P A3 A0 09 E9	N 2 2 2 2 2 2 2 2	2 2 2 2 2 2	AE AC 4E 8D 2E ED 8D 8E 8C	4 4 6 4 6 4 4 4 4 4 4	3 3 3 3 3 3 3 3 3 3 3 3 3 3	A6 A4 46 05 26 E5 85 86 84	3 3 5 3 3 3 3 3 3 3	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	4A 2A	2		48 68 68 68 68 68 68 68 68 68 78 78 78 AAA 8A 8A 8A 94 94 95 78 78 78 78 78 78 78 78 78 78	2 3 3 4 4 6 6 6 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	©1	6	2 1	F1	5 6	2 1 3 2 F	6 6 5 4 6 6 5 4 95 4 94 4	2 2 2 2 5 3 1 2 1 2 1 2	2 31 2 51 2 51 2 51 2 51 2 51 2 51 2 51 2 5		· 3	8 F1	9 4	4 3 4 3	3		Exc		IVE	OR	ę	996	4	2	× + + + + + + + + + + + + + + + + + + +	2 2 2 1 2 1 1 2 2 2 1 2 1 1 1 1 2 2 2 1 2		TOP	ED)		
ID X           L D X           L D X           L D X           L S R           N O P           O R A           P H P           P L A           P L P           R O L           R T S           S B C           S E I           S T A           S T X           T A Y           T S X           T Y A           (1) ADD           ADI	OPERATION           M + X         (1)           M + Y         (1)           Q+C         Single           NO OPERATION         AV M + A           A - Ms         S-1-+S           Single         Single           Single         Single           Gef Fig. 1)         Single           A - Mc         A           Single         Single           A - Mc         A           Single         Single           A - Mc         A           A - Mc         A           A - Mc         A           A + C         A           A + Y         Single           Single         Single           Y + A         X           D TO 'N'' IF PACE BOUND           D TO 'N'' IF PACE BOUND	0P A3 A0 09 E9	N 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	2 2 2 2 2 2 2 2 2	AE AC 4E 2E ED 8D 8E 8C 8C 0SSI	4 4 6 4 6 4 4 4 4 4 4 4 4 0 PAG	3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	A6 A4 46 85 26 E5 85 86 84	3 3 5 3 5 3 3 3 3 3 3 3	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	4A 2A X Y	2	1 1 NDE	48 68 68 28 40 60 38 F8 78 78 AA AB BA BA BA BA SA SA SA SA SA SA SA SA SA S	2 3 3 4 4 6 6 6 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Ø1	6	2 1	F1	5	2 1 3 2 F	6 6 5 4 6 6	AD	2 31 2 51 2 51 2 51 2 51 2 51 2 51 2 51 2 5	C 4 E 7 D 4 E 7	3	8 F1	9	1 3 1 3			EXC			OR	5	996	4	2		2 2 2 2 1 2 1 2 2 2 2 1 2 1 1 1 1 2 2 2 1 2		TOP	= = = = = = = = = = = = = = = = = = =		
INNEMONIC           L D X           L D X           L D X           L S R           N O P           O R A           P H P           P L A           P L P           R O L           R T I           R T S           S B C           S E C           S E I           S T A           S T X           T A Y           T S X           T X A           T X A           T Y A           (1) ADD(2)           (2) ADD(3)	OPERATION           M + X         (1)           M + Y         (1)           Q+C         Sec           NO OPERATION         AV M + A           A-Mis         S-1-+S           S-1-+S         Mis-+A           S-1++S         Mis-+A           S'+1++S         Mis-+A           S'+1++S         Mis-+A           S'+1++S         Mis-+A           S'+1++S         Mis-+A           S'+1++S         Mis-+A           S'+1++S         Mis-+A           A-M-C         A           A + M         X + M           X + M         A + Y           S + X         X + A           X + S         Y + A           D 1 TO "N" IF PAGE BOU         D 2 TO "N" IF BRANCH O           D2 TO "N" IF BRANCH DOROW.         MIN T- BORROW.		N 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	AE AC 4E 8 D 2E ED 8D 8E 8C 8C	4 4 6 4 6 4 4 4 4 4 4 4 4 9 0 9 00 9 00	3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 5 6 6 8. NT P	A6 A4 46 85 26 E5 85 86 84	3 3 5 3 5 3 3 3 3 3 3	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	4A 2A X Y A	2		48 48 68 28 40 60 38 F8 78 AA AB BA BA BA BA BA BA BA BA	2 3 3 4 4 6 6 6 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	01 E1 81	6 6	2 1 2 1	91	5 6	2 1 3 2 5 2 1 3 3 2 F	∧	AD SUI	2 31 2 5 2 5 2 7 5 9 2 2 3 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	E 7		8 F <sup>1</sup>	9 4	i 3	3 3 4		EXC			OR IED	5	996	4	2		2 2 2 1 2 1 1 2 2 2 1 2 1 1 1 1 1 2 2 2 1 3	RES 0	TOP	ED)		

## MCS6501 - 40 Pin Package

The MCS6501 is a bus compatible replacement for the MC6800 microprocessor. As such, this product uses a two phase high level (5 volt) clock input consistent with the MC6800 device requirements. The MCS6501 while pinout compatible with the M6800 address bus does not have the three-state buffers on the address pins. As such the MCS6501 always has valid addresses on the address bus, with this feature allowing the single cycle mode of operation.



- \* 65K Addressable Bytes of Memory
- \* IRQ Interrupt
- \* NMI Interrupt
- \* RDY Signal (can be used for single cycling)

- \* 8 Bit Bi-Directional Data Bus
- \* Pin Compatible With MC6800
- \* Bus Available Signal
- \* Data Bus Enable

Features of MCS6501

The MCS6502 combines the MC6800 bus compatibility features of the MCS6501 with an on-the-chip clock oscillator and driver which eliminates the requirement for a two phase 5 volt clock input. This feature allows the chip to be driven from a single TTL level input clock, or an RC time base or Crystal time base. Additionally, the MCS6502 has a SYNC line output which signals each time an OP CODE fetch is being performed, thus allowing single instruction execution.



- \* 65K Addressable Bytes of Memory
- \* IRQ Interrupt
- \* NMI Interrupt
- \* On-the-chip Clock
  - ✓ TTL Level Single Phase Input
  - ✓ RC Time Base Input
  - Crystal Time Base Input

- \* SYNC Signal (can be used for single instruction execution)
- \* RDY Signal (can be used for single cycle execution)
- \* Two Phase Output Clock for Timing of Support Chips

Features of MCS6502

## MCS6502

## TIME BASE GENERATION OF INPUT CLOCK

# <u>CRYSTAL</u> (Suggested ranges for $R_F$ , $C_F$ : $0 < R_F < 500K\Omega$ , $2pf < C_F < 12pf$ .)



RES 1 28 \$2 (OUT)	
VSS 2 27 0 0 (IN)	* 4K Addressable Bytes of
IRQ 3 26 R/W	Memory (AB00-AB11)
ŇMI □ 4 25 □ DBØ	
	* On-the-chip Clock
ABØ 🗖 6 23 🗖 DB2	
ABI C 7 22 DB3	* IRQ Interrupt
AB2 8 21 DB4	and a state of the
Ab3 🖸 9 20 🗆 DB5	* NMI Interrupt
AB4 10 19 DB6	
AB5 11 18 DB7	* 8 Bit Bi-Directional Data Bus
AB6 12 17 AB11	
AB7 C 13 16 AB10	
AB8 14 15 AB9	
MCR4502	

	RES L 1	$\frac{28}{28} \begin{bmatrix} \emptyset_2 \text{ (OUT)} \end{bmatrix}$	
	VSS L 2	27 🗖 🖗 0 (IN)	
	IRQ 3	26 🗆 R/W	* 8K Addressable Bytes of
	VCC 4	25 DBØ	Memory (AB00-AB12)
	ABØ C 5	24 DB1	
	AB1 C 6	23 DB2	* On-the-chip Clock
/	AB2 🗖 7	22 DB3	
	AB3 🗖 8	21 DB4	* IRO Interrupt
	AB4 C 9	20 DB5	
	AB5 [10	19 DB6	* 8 Bit Bi-Directional Data Bus
	AB6 [11	18 DB7	o bit bi birectional bata bas
	AB7 [12	17 AB12	
	AB8 13	16 AB11	
	AB9 14	15 AB10	
	MCS6	504	Features of MCS6504

	RES C 1	28	Ø 2 (OUT)	
	Vss 🗆 2	27	Ø <sub>0</sub> (IN)	
	RDY C 3	26	R/W	
		25	DBØ	
	VCC 5	24	DB1	
1.00	ABØ 🗖 6	23	DB2	
	AB1 🗖 7	22	DB3	
	AB2 🗖 8	21	DB4	
	AB3 🗖 9	20	DB5	
	AB4 [ 10	19	DB6	
	AB5 [11	18	DB7	
	AB6 [12	17 -	AB11	
1	AB7 [ 13	16 🗖	AB10	
Y	AB8 [ 14	15	AB9	

	Features of MCS6504
* /	4K Addressable Bytes of Memory (ABOO-AB11)
* (	On-the-chip Clock
*	IRQ Interrupt
* ]	RDY Signal
* (	8 Bit Bi-Directional Data Bus
	Features of MCS6505

## TIME BASE GENERATION OF INPUT CLOCK

<u>CRYSTAL</u> (Suggested ranges for  $R_F$ ,  $C_F$ :  $0 < R_F < 500K\Omega$ ,  $2pf < C_F < 12pf$ .)

