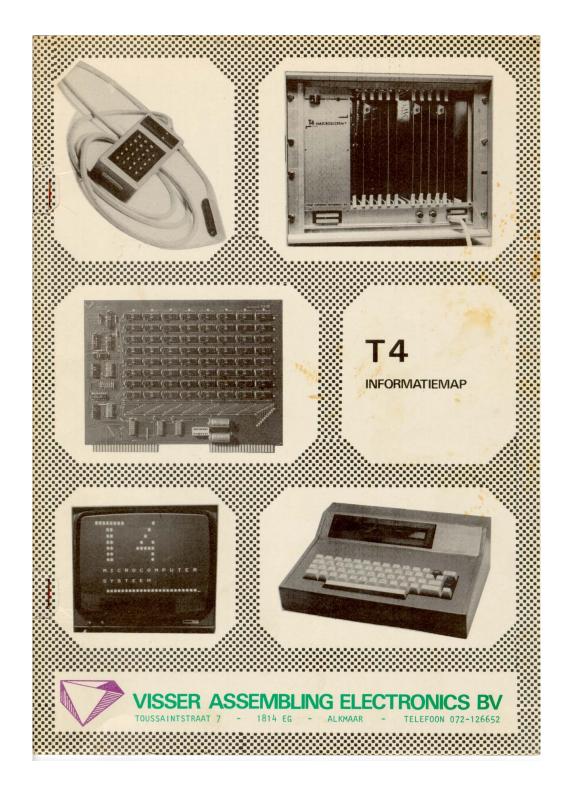
Visser Assembling Electronics/Forbo KIM-1 T4 Expansion system

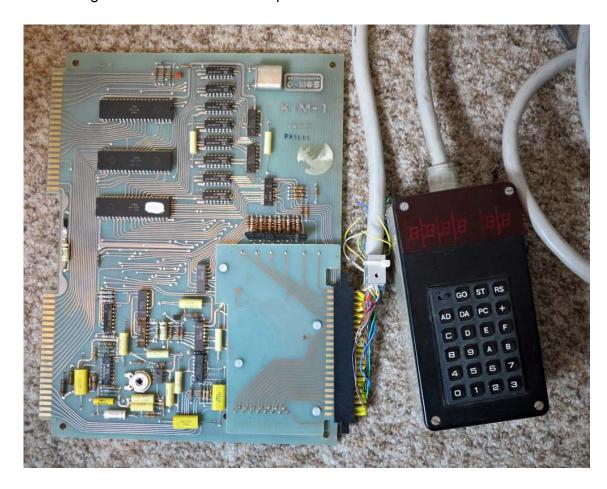


T4 system

- System based on cards same size as the KIM-1
- KIM-1 adapted to fit in a board cage, keyboard/LEDs via adapter board and cable outside of the cage
- Input/output digital and analog
- Video card
- Memory cards, RAM, EPROM

Contents

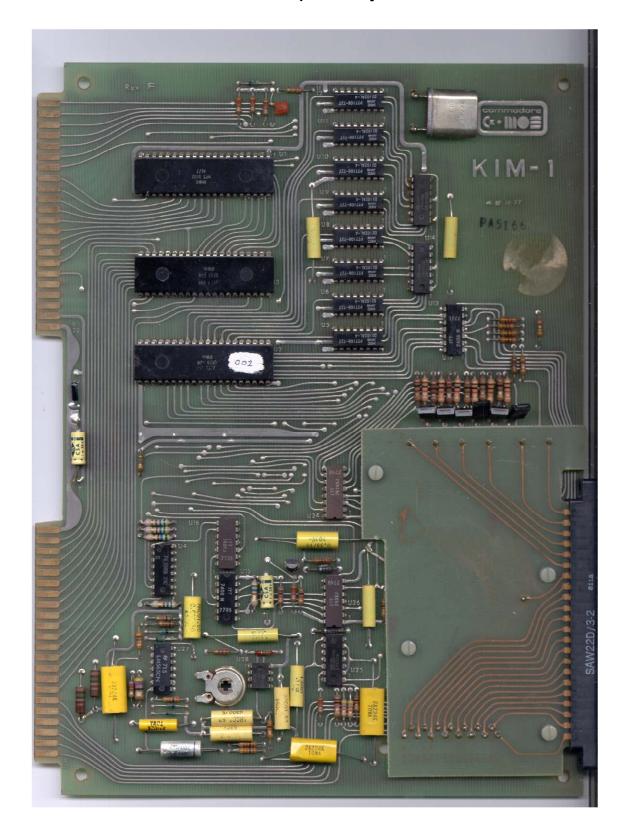
- 1. Adapted KIM-1 for board cage
- 2. Photos of cards.
- 3. T4 folder and descriptions.
- 4. Circuit diagrams and connector descriptions.



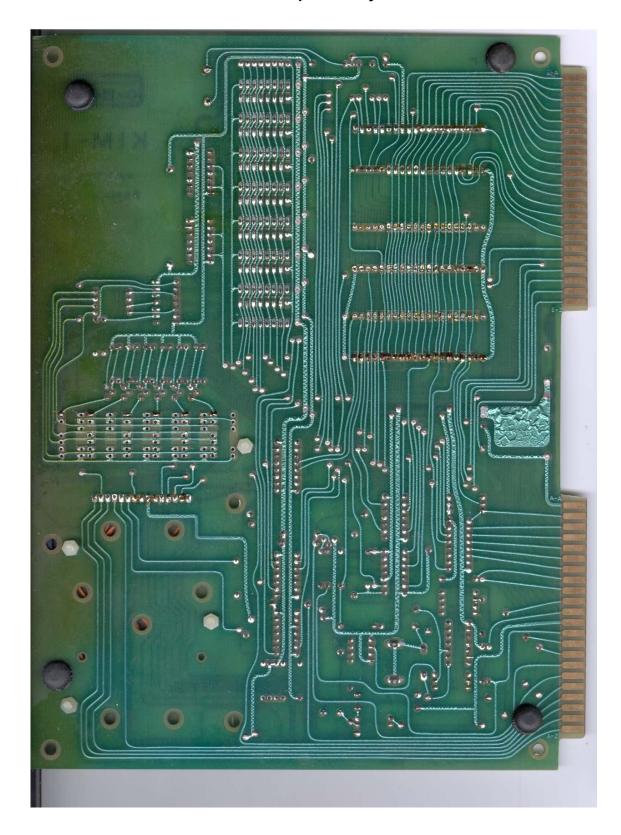
T4 KIM-1 expansion system



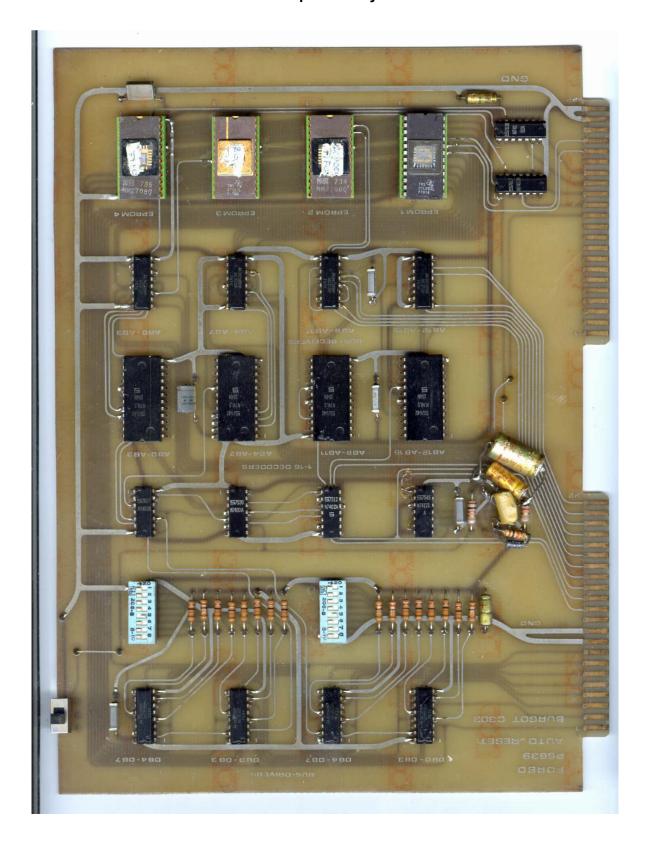
T4 KIM-1 expansion system



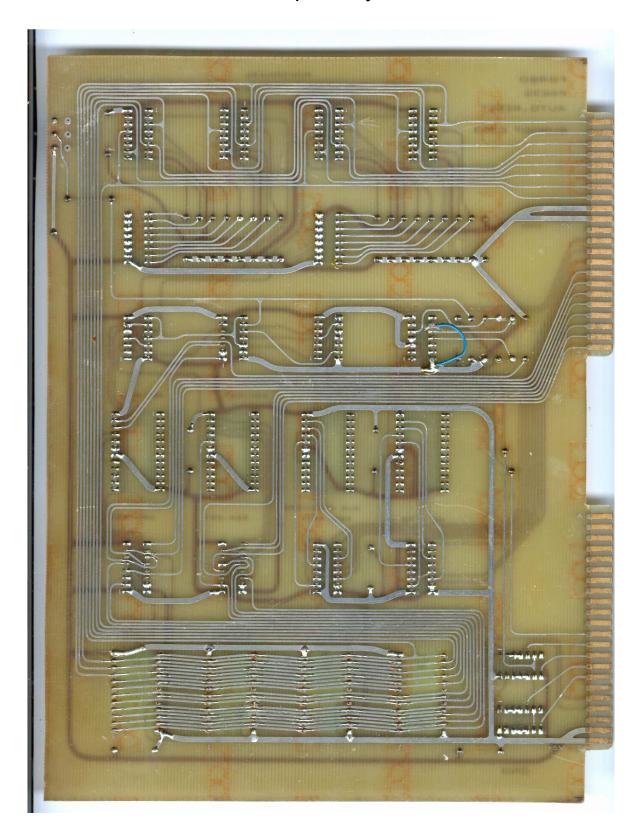
T4 KIM-1 expansion system



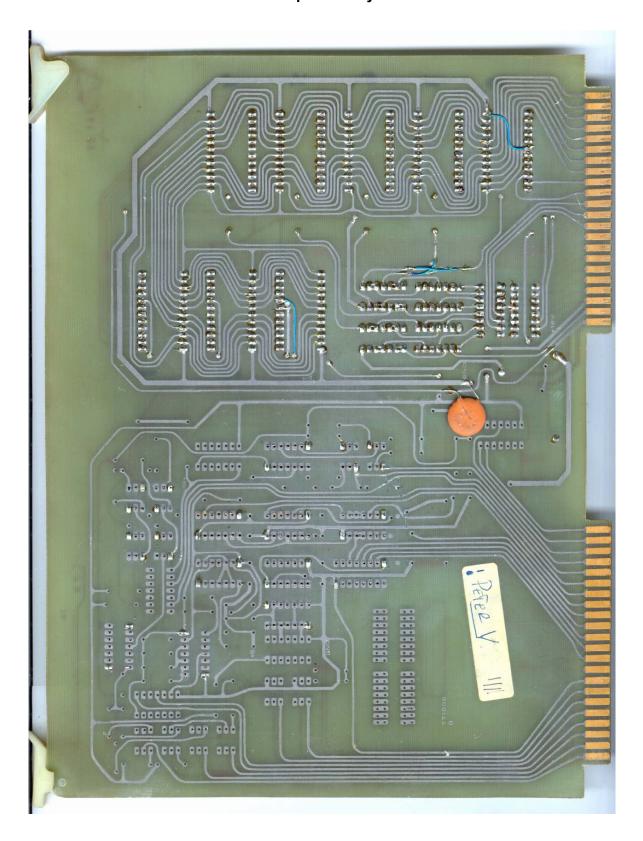
T4 KIM-1 expansion system



T4 KIM-1 expansion system



T4 KIM-1 expansion system



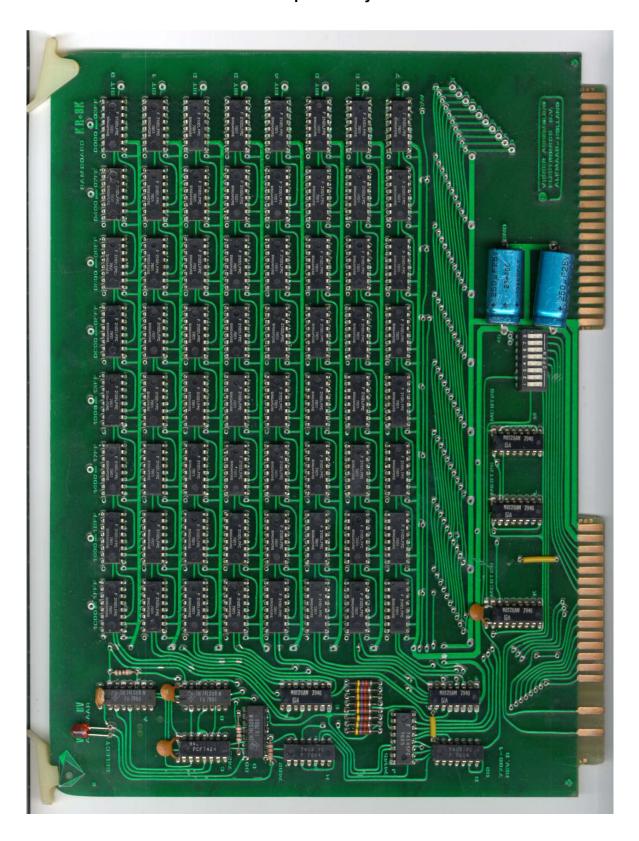
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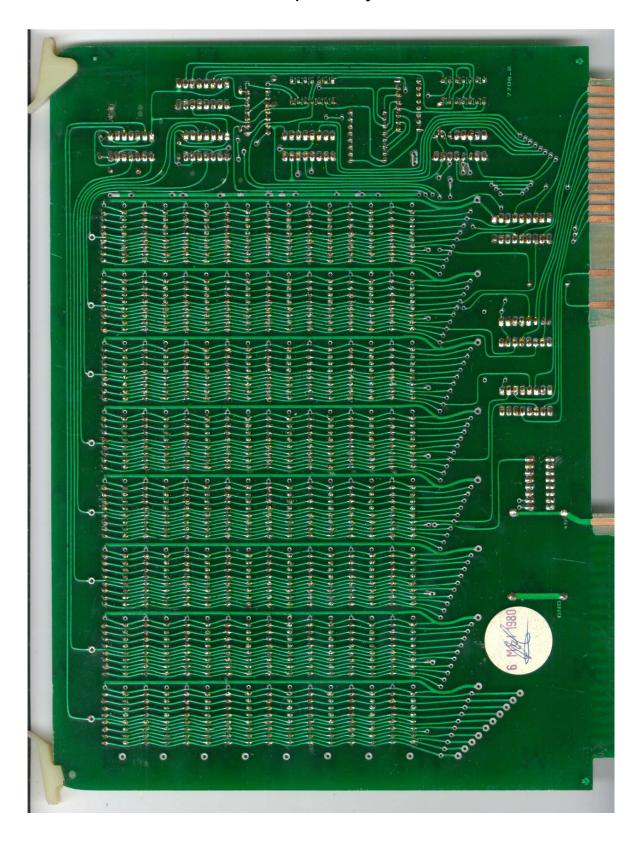
T4 KIM-1 expansion system



T4 KIM-1 expansion system



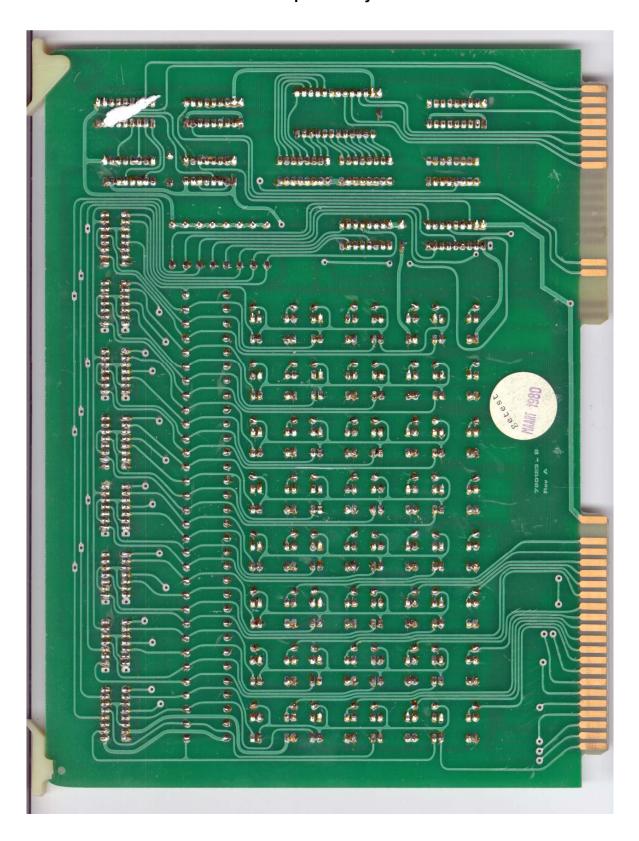
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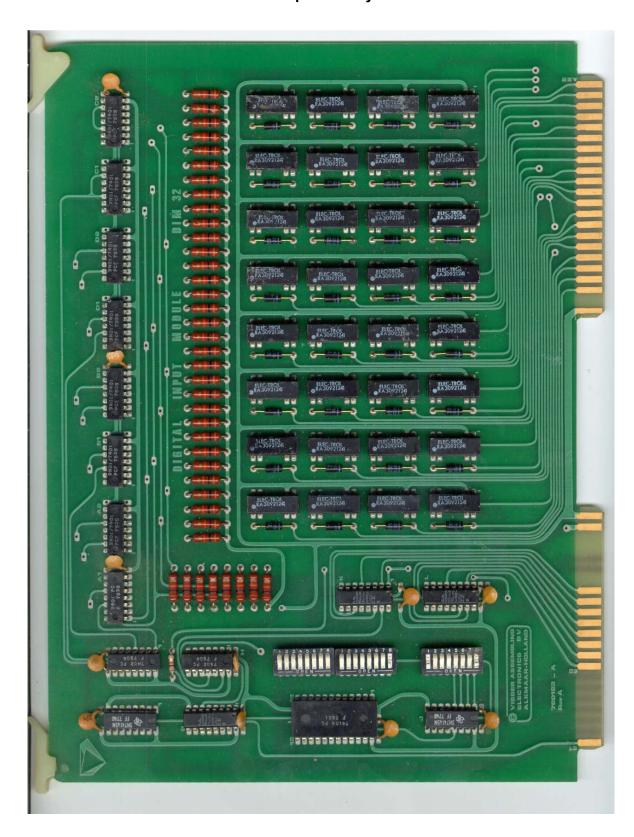
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T4 KIM-1 expansion system



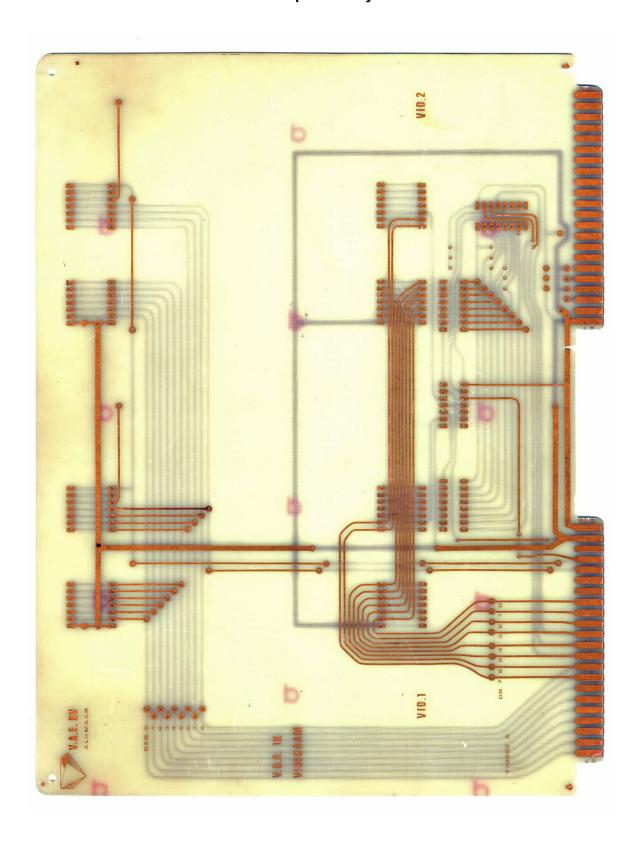
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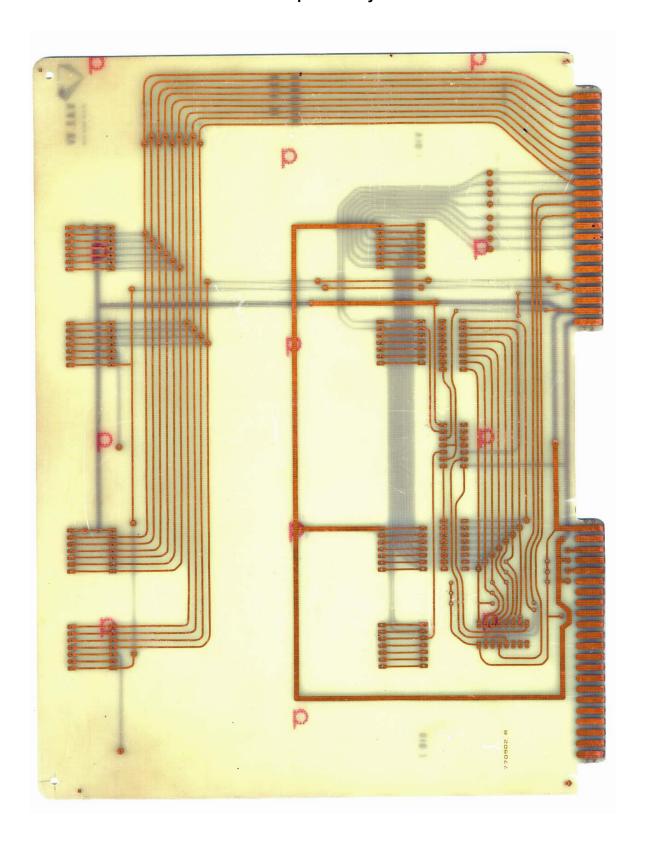
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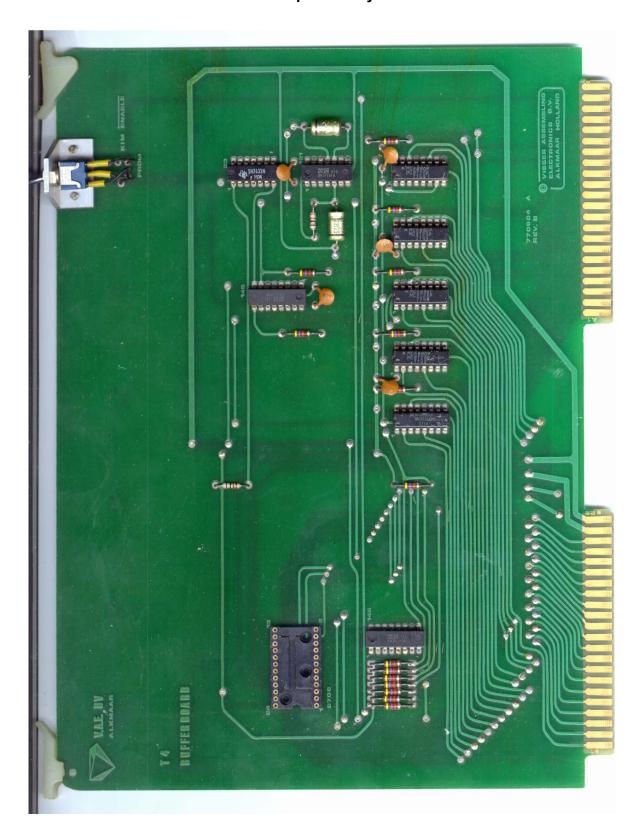
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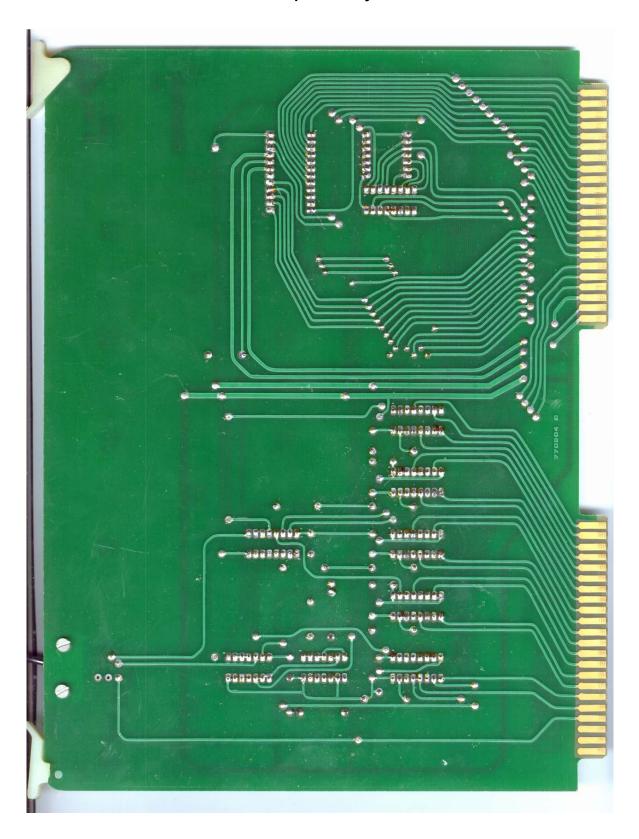
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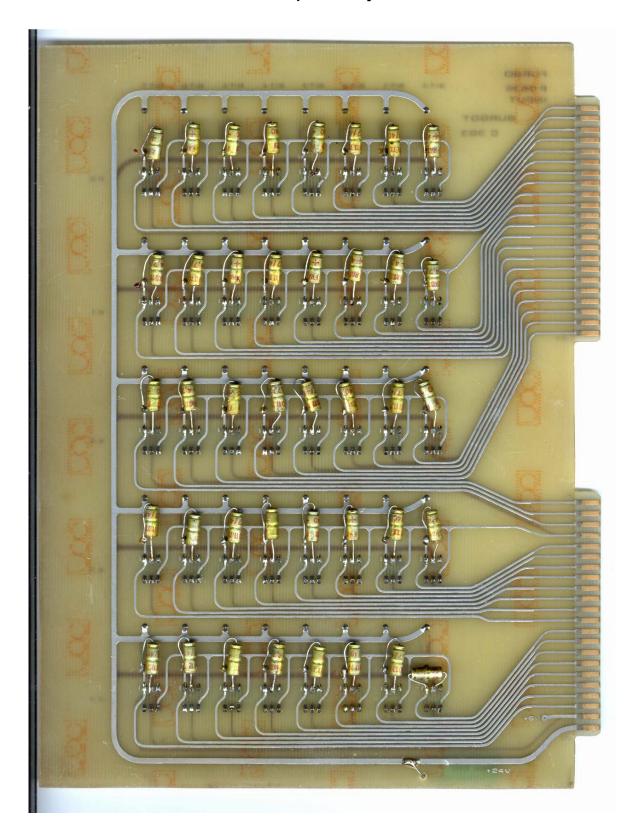
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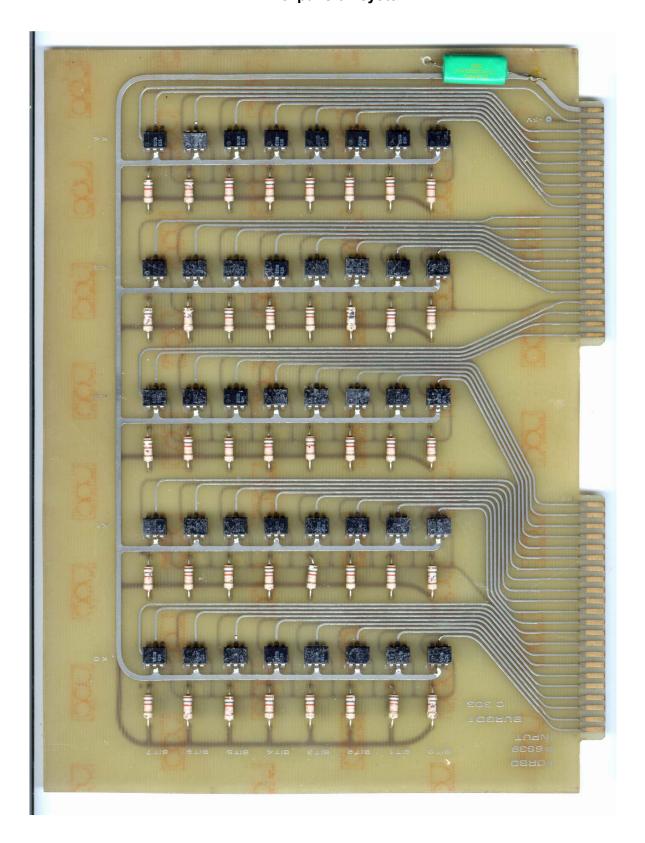
T4 KIM-1 expansion system



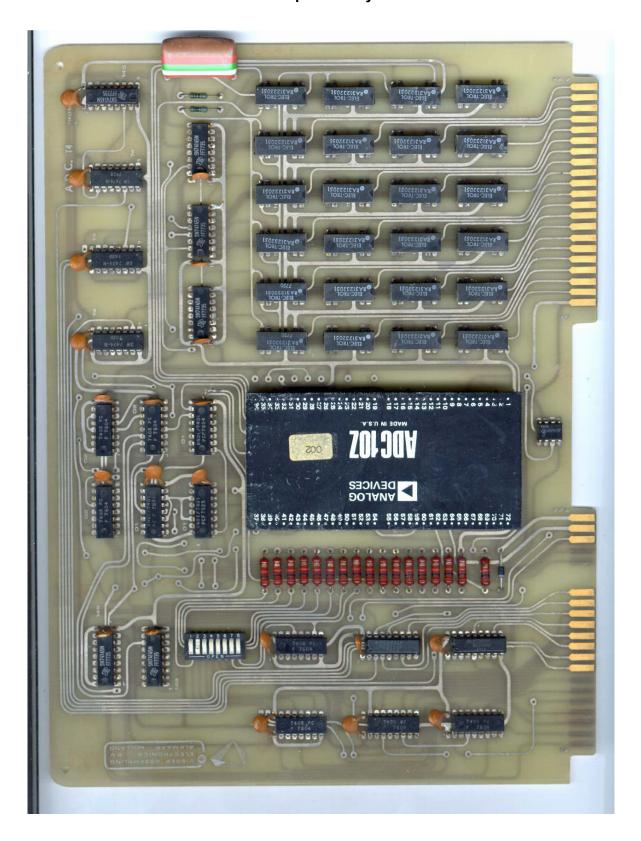
T4 KIM-1 expansion system



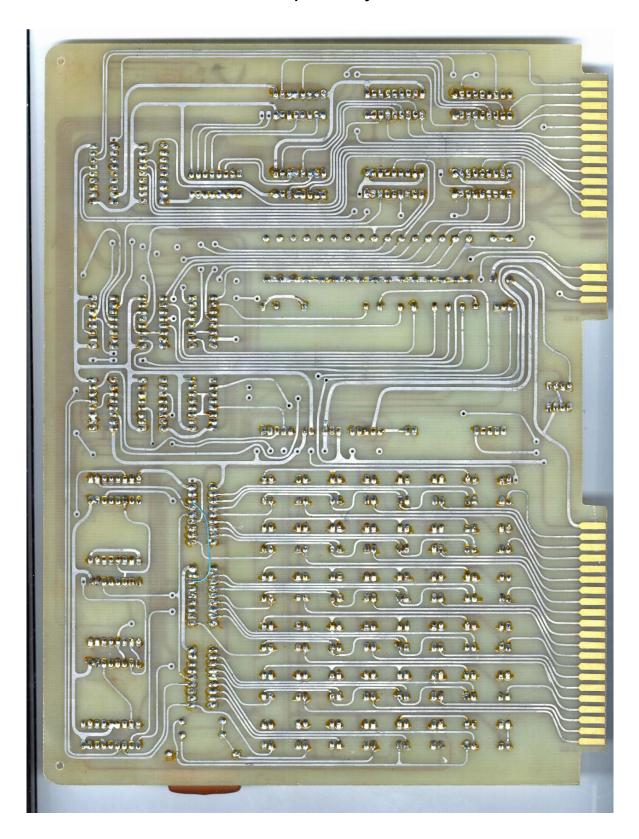
T4 KIM-1 expansion system

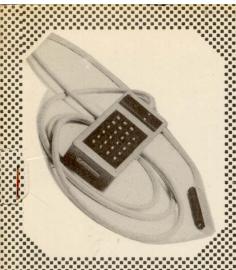


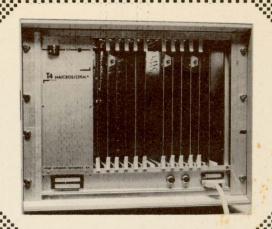
T4 KIM-1 expansion system

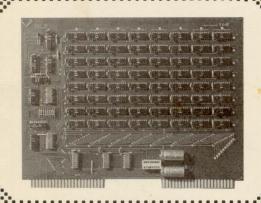


T4 KIM-1 expansion system









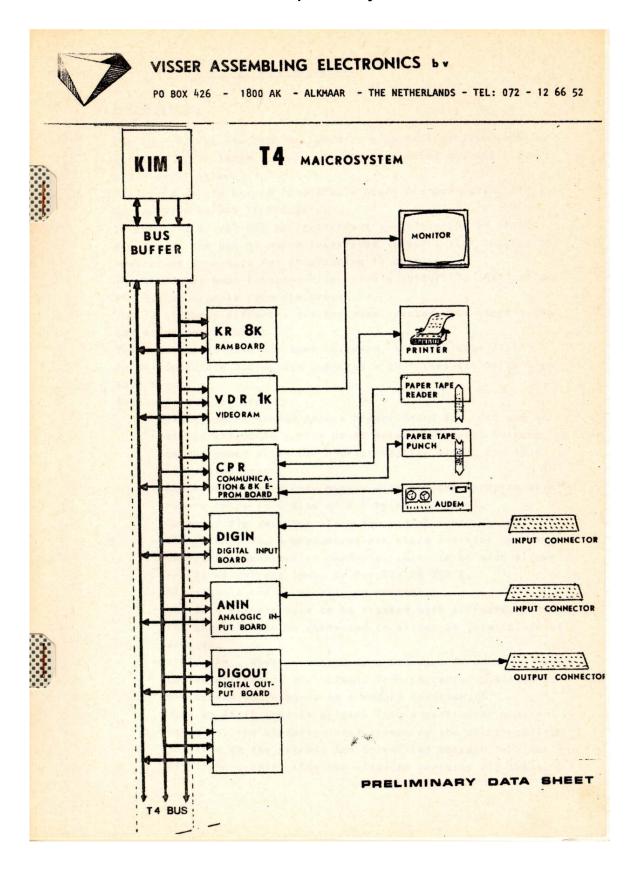
T4
INFORMATIEMAP







T4 KIM-1 expansion system



T 4 SYSTEM DESCRIPTION

Introduction.

The T4 - System has been designed as a general purpose computer suitable for a large variety of process control and small scale E D P applications.

The basis of the system is a single board microcomputer, KIM I as produced by MOS TECHNOLOGY .

T4 consists of various peripheral and interface boards around the KIM I. The use of these interfaces is such, that an easy to understand procedure for programming is obtained.

The KIM I has been expanded first with a BUSBUFFER, that buffers all output signals from the processor.

Thus a slightly different bus has been created with signals that can stand heavy loads.

The datasignals have not been buffered, thus the data lines to all interface boards are buffered with threestate buffers on each board.

Available modules are:

- RAM board. Random Access Memory board for read and write operations in a size of 8K bytes per board. Switches on the board allow for address-setting within the 65 K addressing space.
- ROM board. Read Only Memory with erasable programmable memory chips in a size of 8 K bytes per board.
 On board dip switches allow for variable addressing.
- COMMUNICATIONS. A communications board contains two asynchronous communication channels, that can be used either for 20 mA current loop, or for EIA RS 232 C.
 All signals are under program control.
 The data signals have to be created with software. Each of the channels can be connected to either as terminal or as dataset.
- VIDEO RAM . When connected to a standard TV monitor, text can be written on the screen. Each character position of the screen corresponds to a memory location. When an ASCII code is written into a particular memory location, the character will appear on the corresponding position on the screen. The screen can contain 16 lines of 32 characters, thus the videoram contains 512 bytes.

-DIGITAL INPUTS. The digital input board can accept 32 signals from the field. Input is fully isolated. The 32 signals can be read from 4 consecutive addresses.

input boards are either using opto isolators or reed relais for isolation.

- DIGITAL OUTPUTS. A digital output board houses 32 output signals, that are ending in either opto isolator driven darling-ton transistors or in reed relais. The signals are organized in groups of 8 bits, thus occupying 4 different addresses.
- ANALOG IMPUT; An analog inputboard is a complete subsystem that is capable of reading 22 different analog signals with a range of either -5 through +5 Volts or 0 - 10 Volt. A flying capacitor is used for full isolation. Each board contains a separate zero and full scale calibration channel. All multiplexer timing is software driven. The multiplexer is using reed relais.

The T 4 BUS occupies all 44 pins of the EXPANSION CONNECTOR. All expansionconnectors starting at the BUSBUFFER can be wired through.

ADDRESSING SCHEME OF T 4 .

18 18 18 -06 + 18"

The full 65 K addressingspace of the 6502 processor is being used within the T4 system configuration.

Fixed addresses have been assigned for the various peripheral boards.

Address 0000 - 1FFF is occupied by the KIM 1 including 1K RAM on location 0000 - 03FF and the KIM MONITOR in the 6530 ROM'S at location 1800 - 1FFF. The leftover space from 0400 - 17FF is partially used by the timers and may be used for an additional 4K RAM or EPROM. (Not standard T4)

Address 2000 - DFFF is assigned for any type of memory, that is organized in 8K amounts. Each 8 K starts 2000 higher than the

The total capacity of T 4 for RAM and EPROM is thus 6 x 8 = 48K This means for example 16 K EPROM and 32 K of RAM. Any mix of 8K boards can be used.

3

Address E000 - EFFF is for VIDEORAM applications. The total capacity is 8 VIDEORAM's, thus 8 different TV monitors.

Address F000 - F1FF is used for analog inputs. Since one board occupies 2 addresses for addressing 22 channels, this gives a total capacity of 512 x 22 = 11264 different channels.

Address F200 - F7FF is not assigned. It is reserved for future expansion.

Address F800 - FBFF is for digital in- and output.

Each address contains 8 inputbits (when a read-type instruction is executed) and 8 output bits (with any write-type instruction) This gives a system capability of 8192 input signals and 8192 outputsignals.

Address FCOO - FFFF is assigned for the 1K EPROM that is on the BUSBUFFER board.

0000-1FFF KIM 1 Microcomputermodule. (Can have RAM/PROM in location 0400-13FF). 2000-3FFF Memory. RAM/PROM/GRAPHICS 4000-5FFF sor enliques bloodysvendesd. 6000-7FFF 8000-9FFF and the correspondent A000-BFFF COOO-DFFF E000-EFFF VIDEO RAM MODULES F000-F1FF ANALOG INTERFACE (Input/output) F200-F7FF Not assigned F800-FBFF DIGITAL INPUT/OUTPUT MODULES FC00-FFFF 1K PROM on busbuffer wich can contain vectors of KIM 1 (switch selectable)

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BUSBUFFER BOARD.

The bufferboard of T4 acts as interface between the KIM 1 processorboard and the T4 BUS. All output signals from the bufferboard are buffered through an 8T26 (+ 100 TTL loads)

KIM 1 signals that are buffered are:

- AB 0 AB 15 Address lines. On the T4 BUS these signals are named BAB 0 - BAB 15
- \$2 and \$2 second phase of microprocessor clock. All data for write type instructions is available at the rising edge of $\phi 2$, while data for read type instructions must be available at the falling edge of Φ 2. Addresses and RW are stable throughout 02.

These signals are named B\$\psi_2\$ and B\$\psi_2\$ on the T4 BUS.

- RW and RW. Read-write control. The RW-signal is high during a processor read and low during a processor-write. These signals are named BRW and BRW on the T4 BUS.
- During powerup, the bufferboard generates the RST, that is required for processorstart and various peripherals. When active the signal is low. It is available on the T4 BUS and fed back into the processorboard.
- A decoding circuit on the bufferboard supplies the signals KIM ENABLE, 8K1, 8K2, 8K3, 8K4, 8K5, 8K6 and 8K7. The signals 8K1 - 8K7 indicate, that the current memory address falls into a particular multiple of 2000(hex). For example when address 31A6 is on the bus, the signal 8K1 will be low. 8K1 -8K7 are T4-bus signals. These signals are open collector driven and can stand 10 TTL-loads.
- KIM ENABLE is fed back to the processor and enables the first 8K of the addressingspace. It is generated either when address 0000 - 1FFF is on the addressbus, or when the switch on the bufferboard is in the position "KIM" and address, FCOO - FFFF is on the addressbus. The signal I/O SELECT is a T4-bus signal, generated when address FOOO - FBFF is on the addressbus. It is used for digital and analog I/O selection.

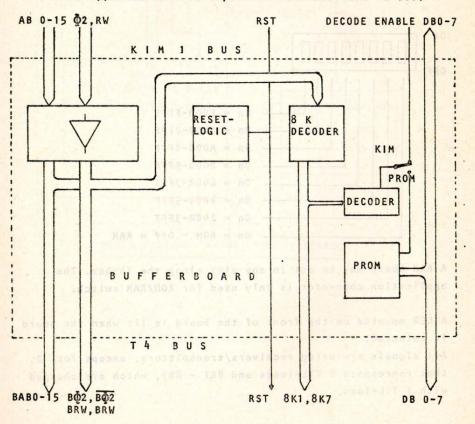
On the bufferboard is an EPROM-socket available that can receive a 2708 1K byte EPROM. This EPROM occupies the uppermost 1K in the addressingspace. When addresses FCOO - FFFF appear on the addressbus, this either triggers the EPROM or the KIM locations 1COO - 1FFF. This can be selected with the PROM/KIM switch on the bufferboard.

If the T4-system resets due to power up, this EPROM has to contain the vectors when the switch is in the PROM-position.

If no PROM available, the switch must be in the KIM-position.

Various monitor PROMS can be supplied, that contain KIM-monitor-like programs, suitable to a particular configuration.

The bufferboard must have its own fixed place in the mounting, since both application- and expansion-connector are in use.



BLOCK DIAGRAM BUSBUFFER MODULE.

5

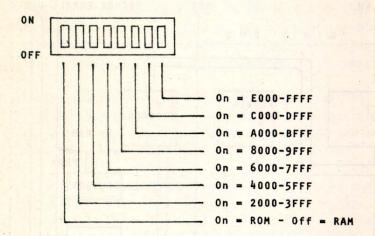
RAM - BOARD.

A RAM-board contains an array of 64×2102 1K bits chips, that is organized as 8K bytes.

The RAM can be used to read and write data.

An onboard switch allows for read-only operation. If a program has to be tested, that finally must reside in PROM, a suitable procedure will be to load the program in RAM and then set the RAM to read-only to simulate the features of a ROM. This switch can also be connected external on the applications connector of the RAM-board.

The first address of an 8K RAM board can be set to any integer multiple of 2000(hex), except for 0000. A jumper has to be soldered on the board to make address E000 - FFFF available. Switch settings:

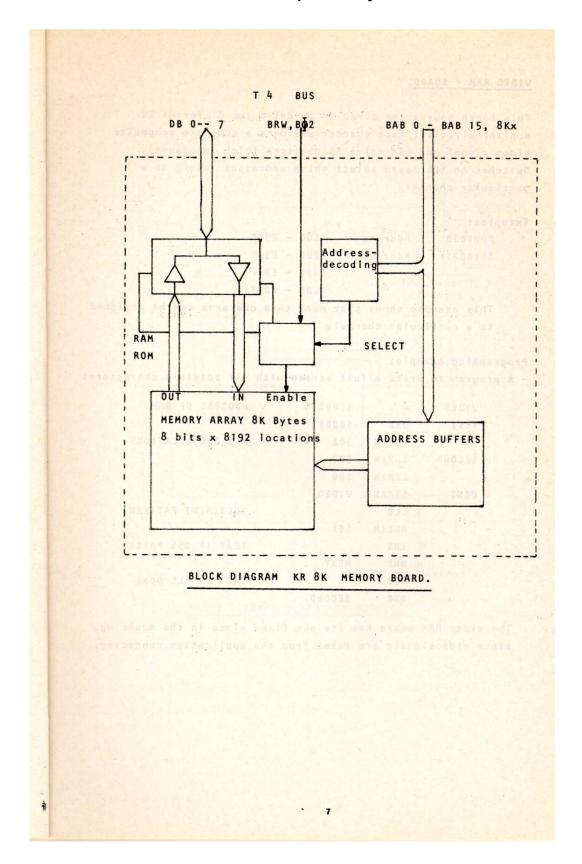


A RAM board may be put in any slot along the T4-bus. The application connector is only used for ROM/RAM switch.

A LED mounted on the front of the board is lit when the board is selected.

All signals are using receivers/transmittors, except for 2, that represents $8\ TTL$ -loads and 8K1 - 8K7, which are charged with $1\ TTL$ -load.

T4 KIM-1 expansion system



VIDEO RAM - BOARD.

This board houses the circuits to drive two different TV-monitor-circuits. Each channel delivers a complete composite video signal and can drive 25 monitors (high impedance). Switches on the board select which addresses belong to a particular channel.

Examples:

0001000	Address		E800	-	E9FF	
0110001	Address		E200	-	E3FF	
	+ "	,	EAOO	-	EBFF	
			FCOO	-	EDFF	

This example shows that more than one area can be assigned to a particular channel.

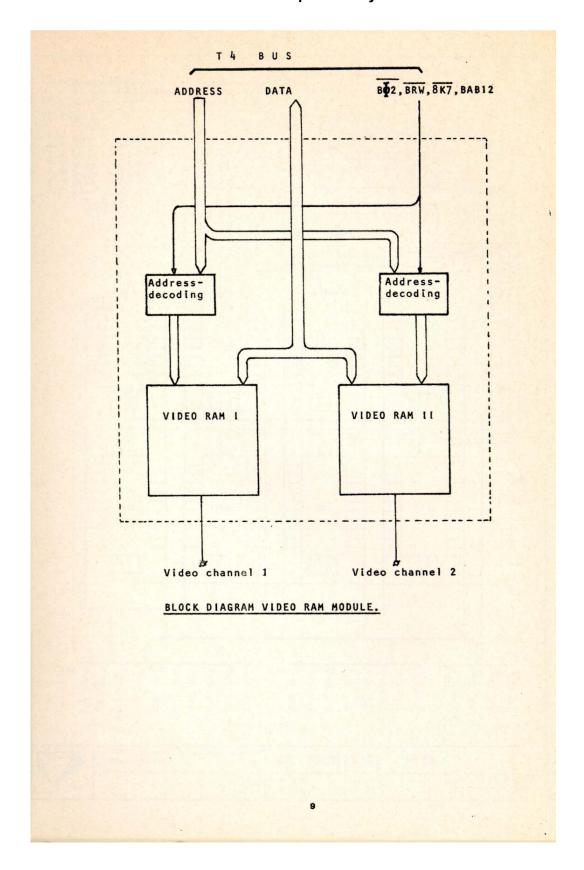
Programming example:

- A program to write a full screen with all possible characters:

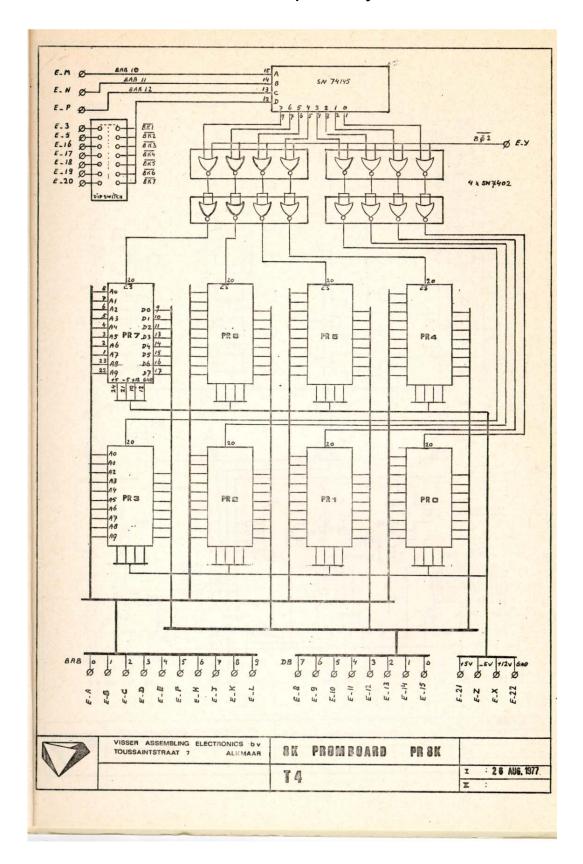
VIDEO	À	\$E000	ADDRESS OF RAM
TEST	ORG	\$0000	
	LDYIM	\$02	2 X 256 LOCATIONS
SECOND	LDXIM	\$00	
	LDAIM	\$00	
NEXT	STAAX	VIDEO	
	CLC		INCREMENT PATTERN
	ADCIM	\$01	
	INX		TEST IF 256 PASSED
	BNE	NEXT	
	DEY	ия вк нем	TEST IF ALL DONE
	BNE	SECOND	

The video RAM board has its own fixed place in the mounting, since videosignals are taken from the application connector.

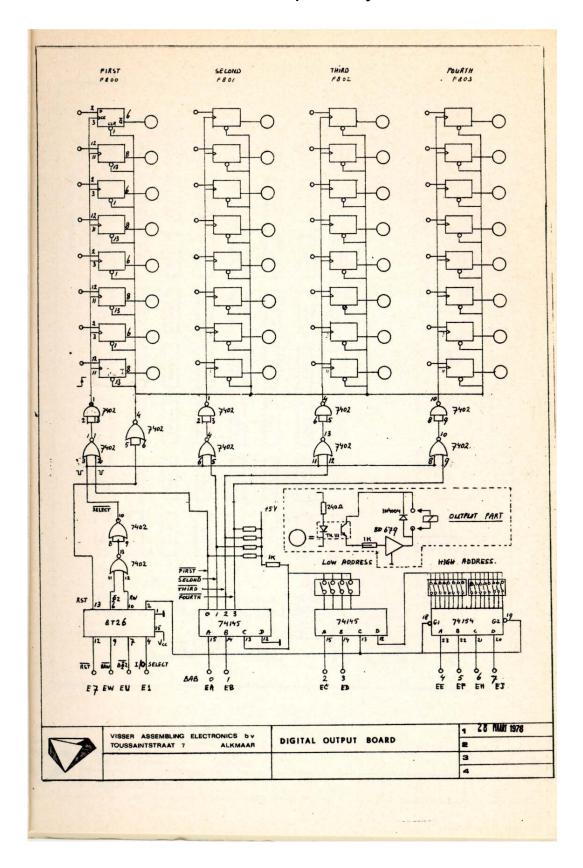
T4 KIM-1 expansion system



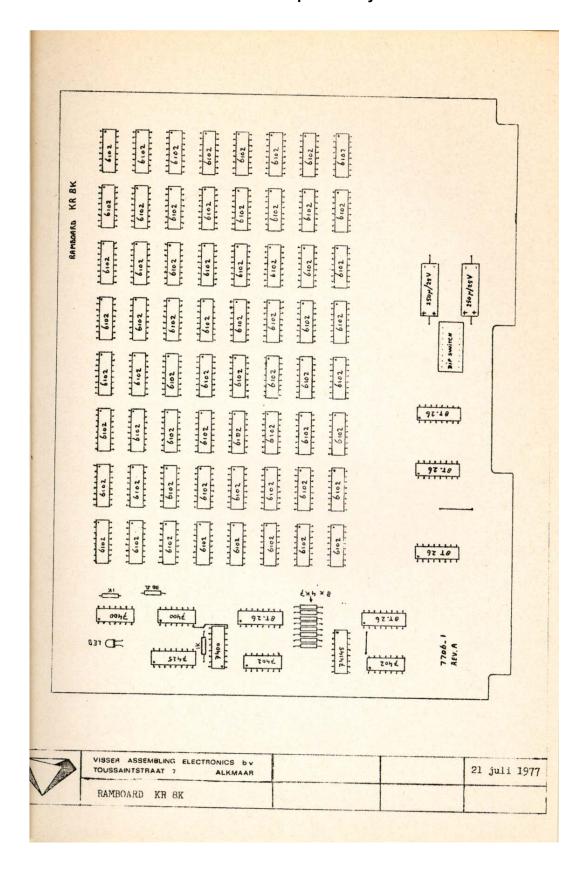
T4 KIM-1 expansion system



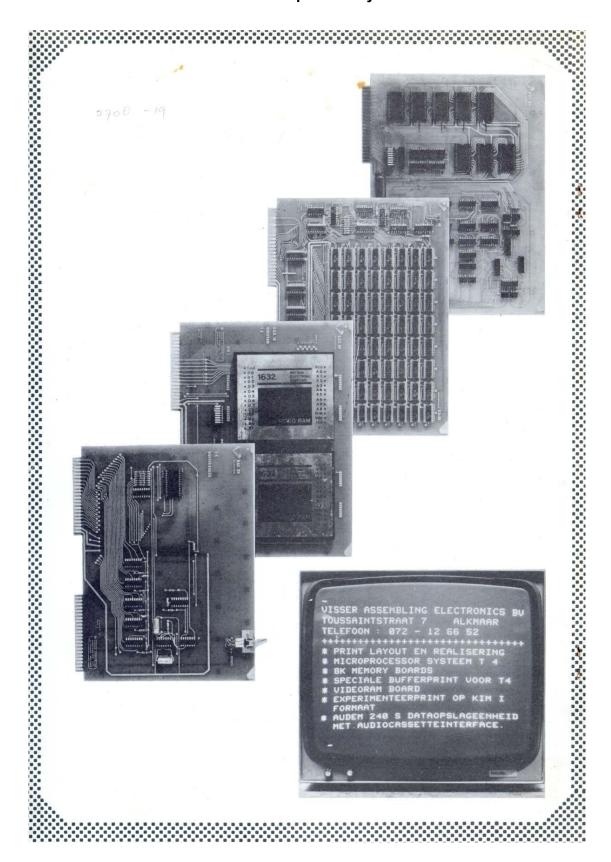
T4 KIM-1 expansion system



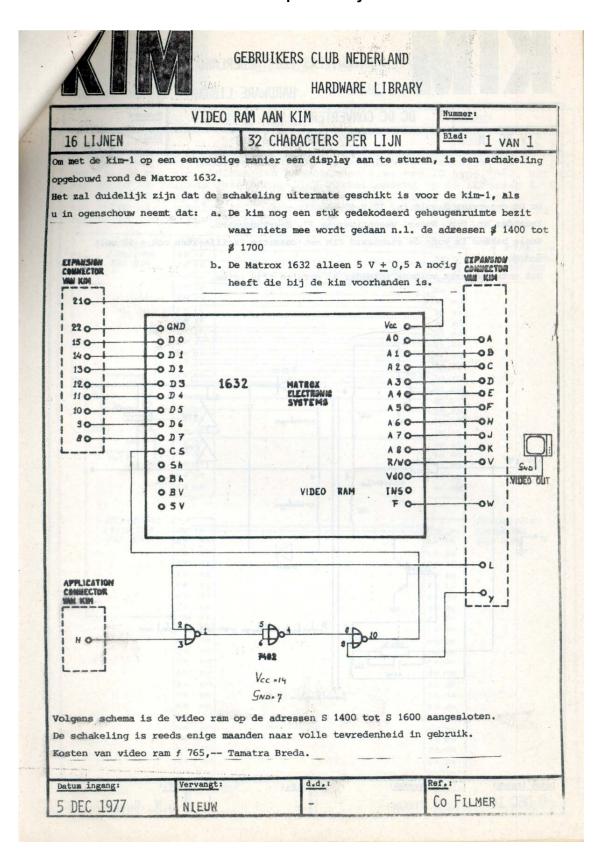
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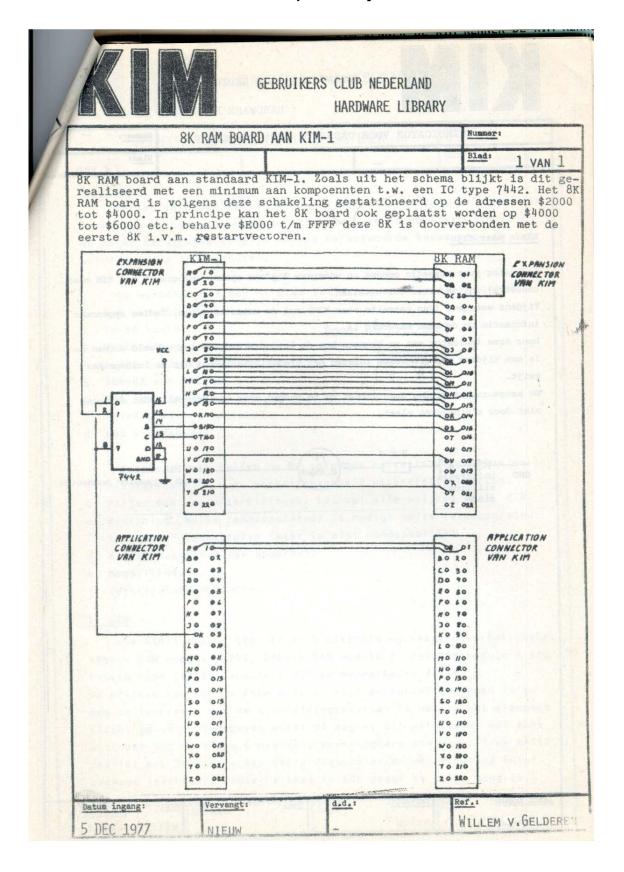
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T4 KIM-1 expansion system



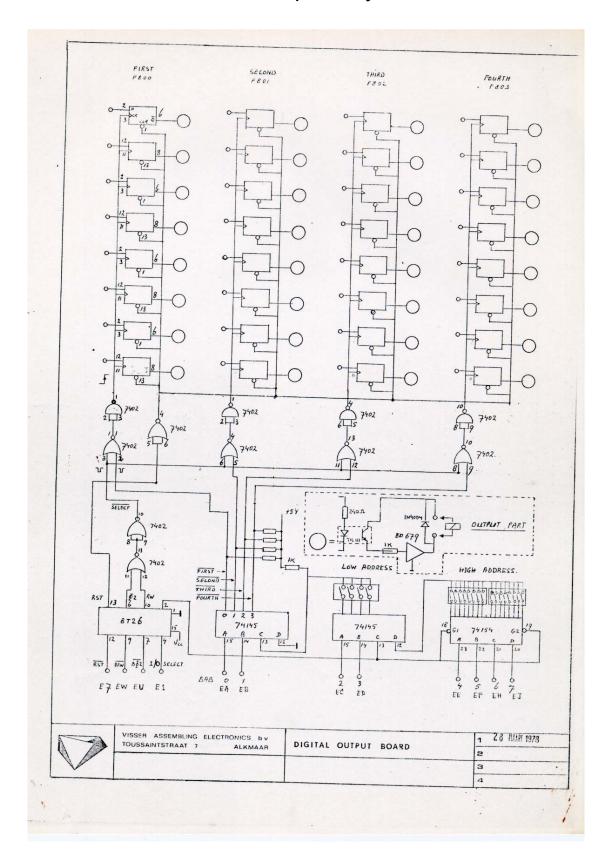
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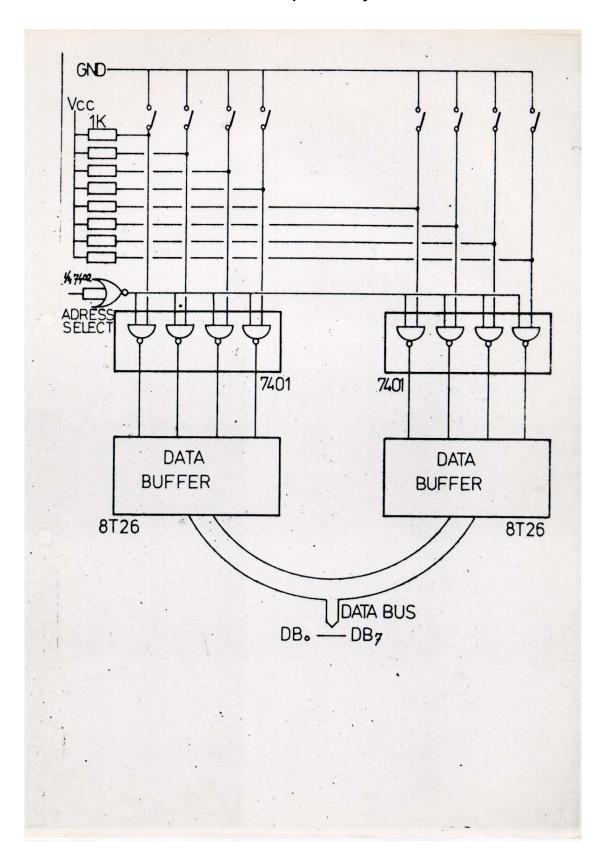
T4 KIM-1 expansion system

2 RDY 4 IRQ 6 NMi 7 RST 7 8 6 9 5 00 9 11 3 12 2 13 1 14 0 15				
Adres 0-15 Ekim Phi 2 2º ph. clock RST Decode enable Databus 0-7	A -	Bush	ffer	
		E7		

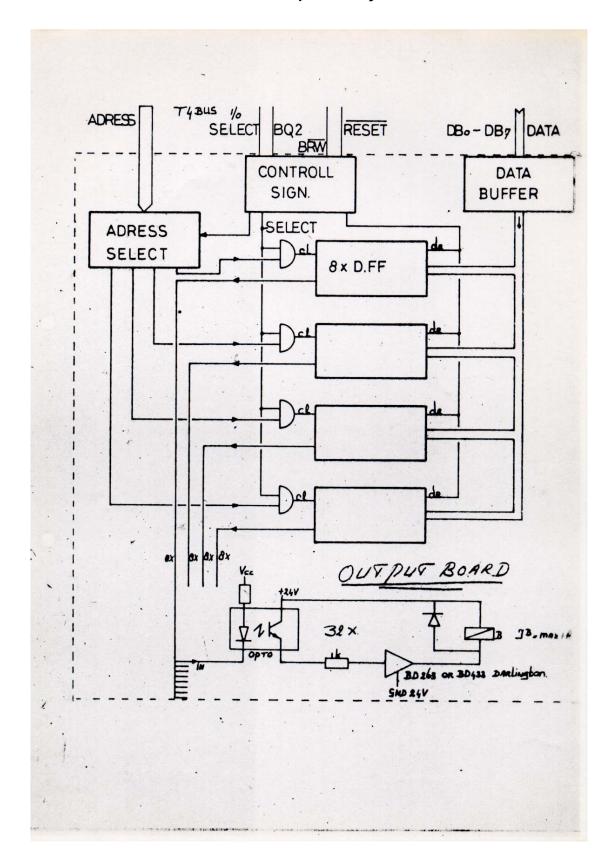
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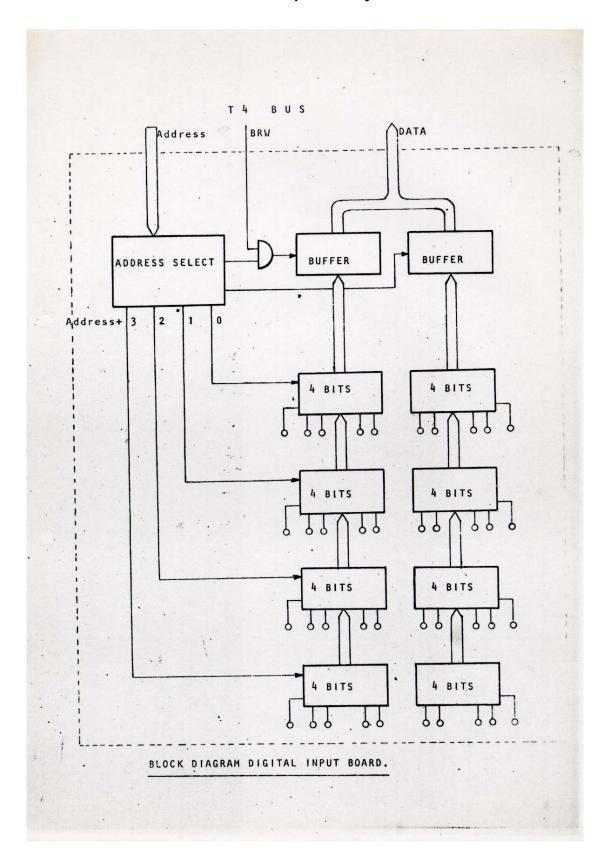
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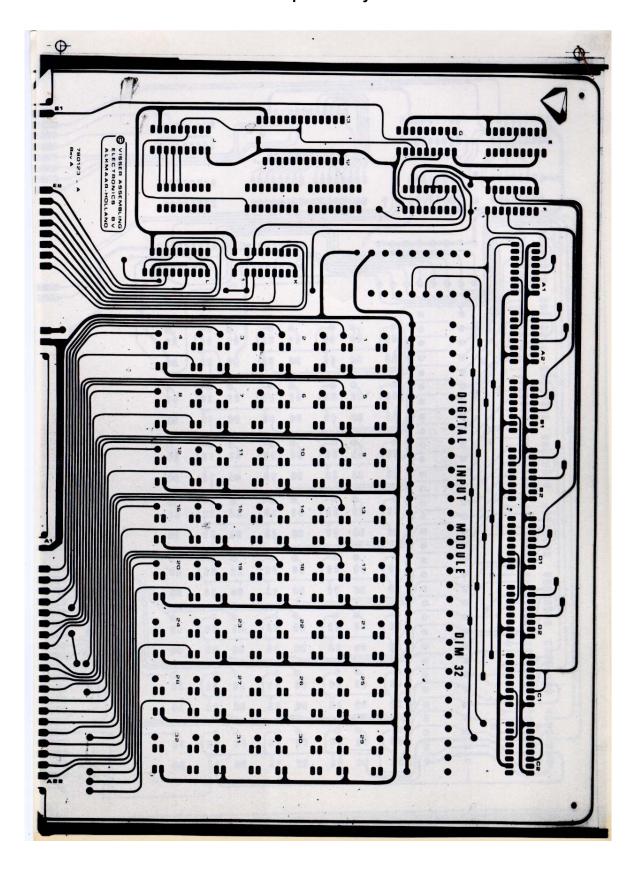
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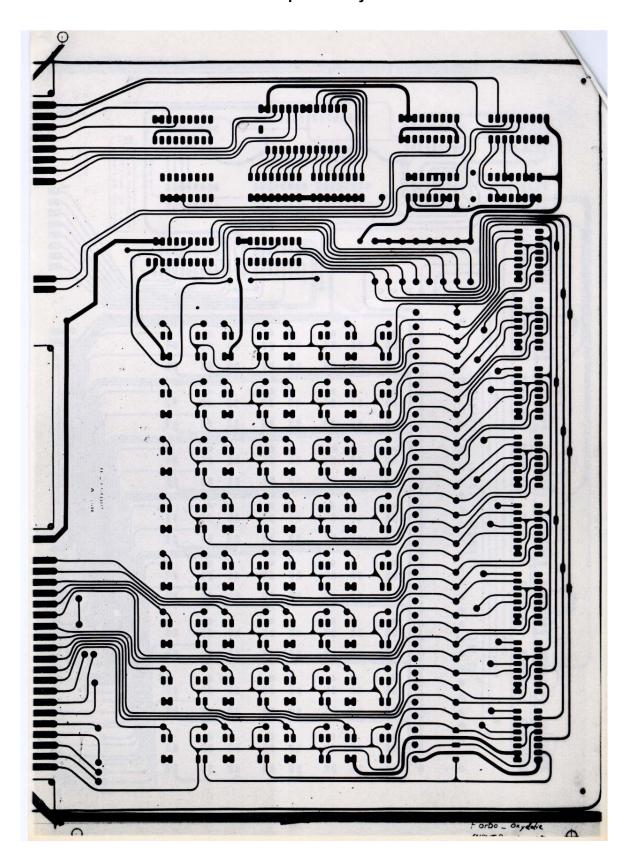
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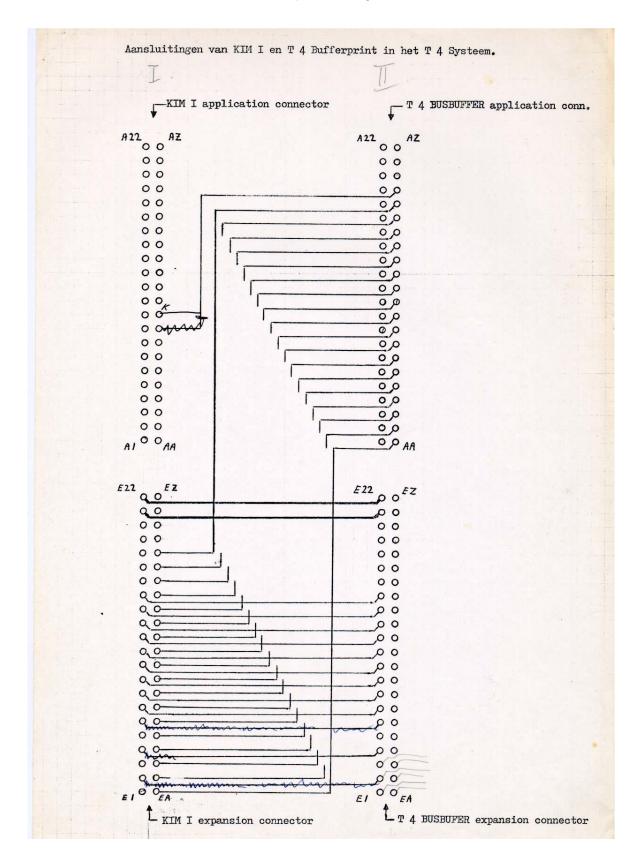
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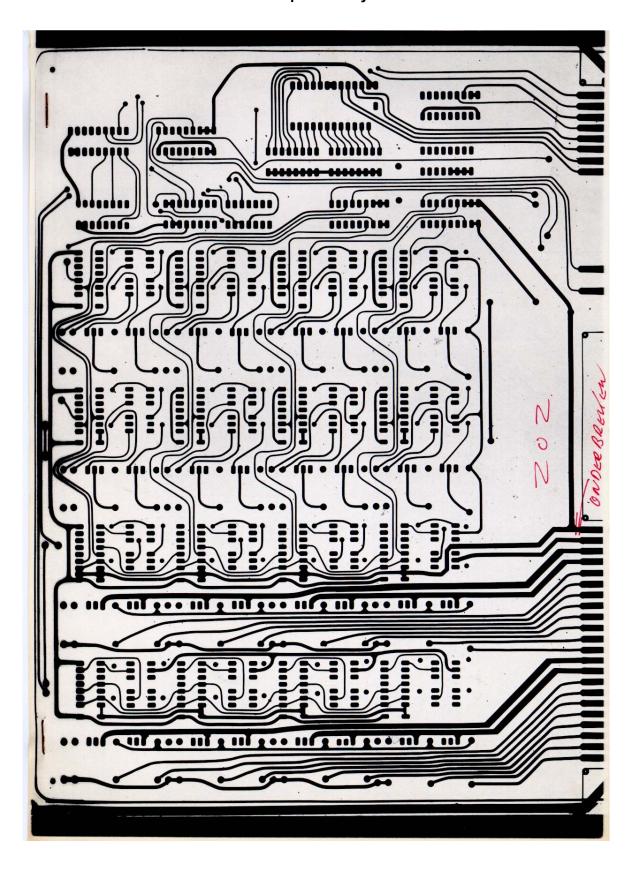
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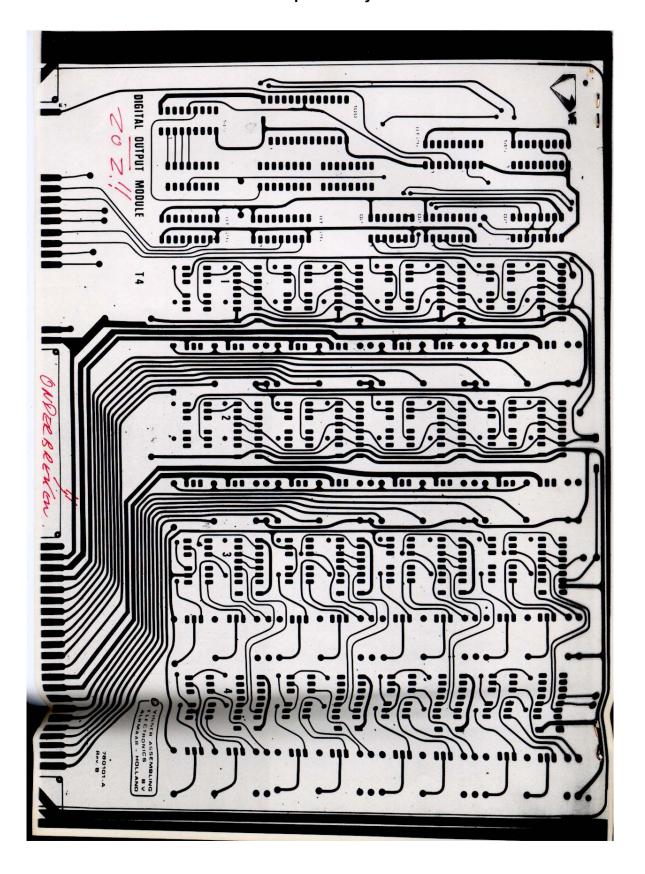
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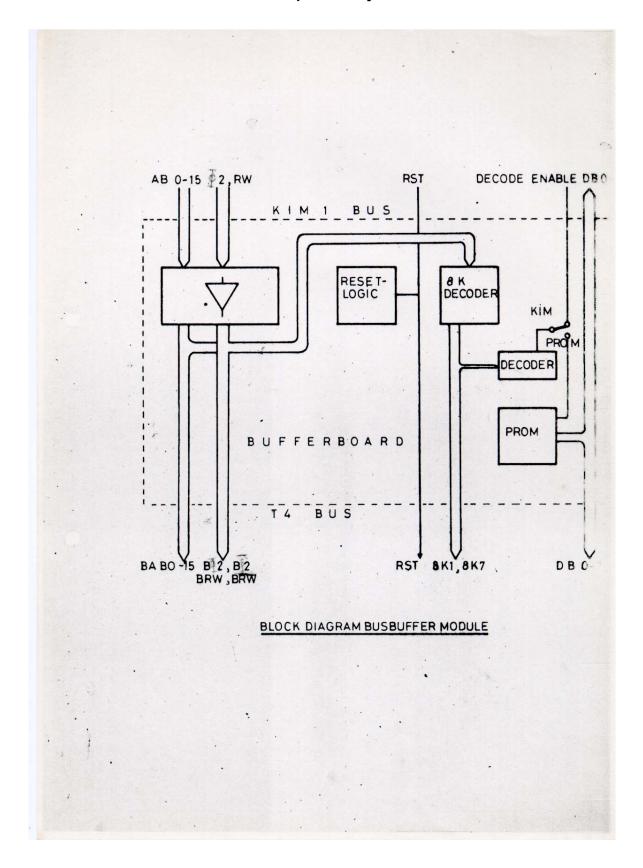
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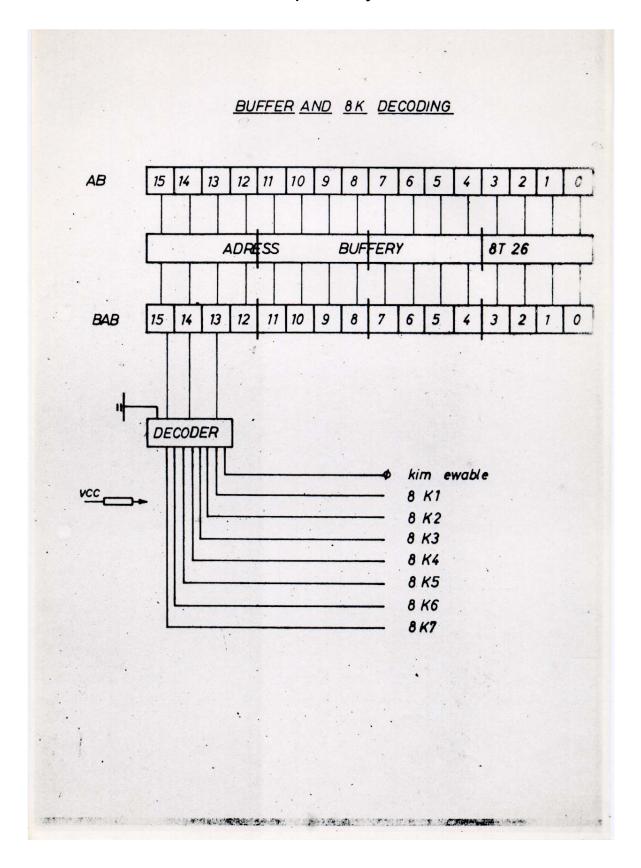
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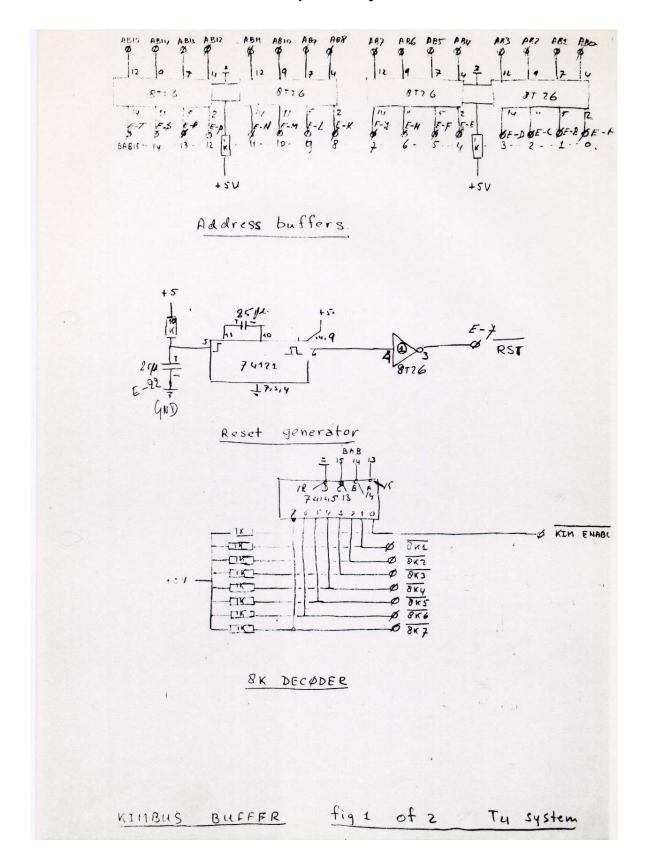
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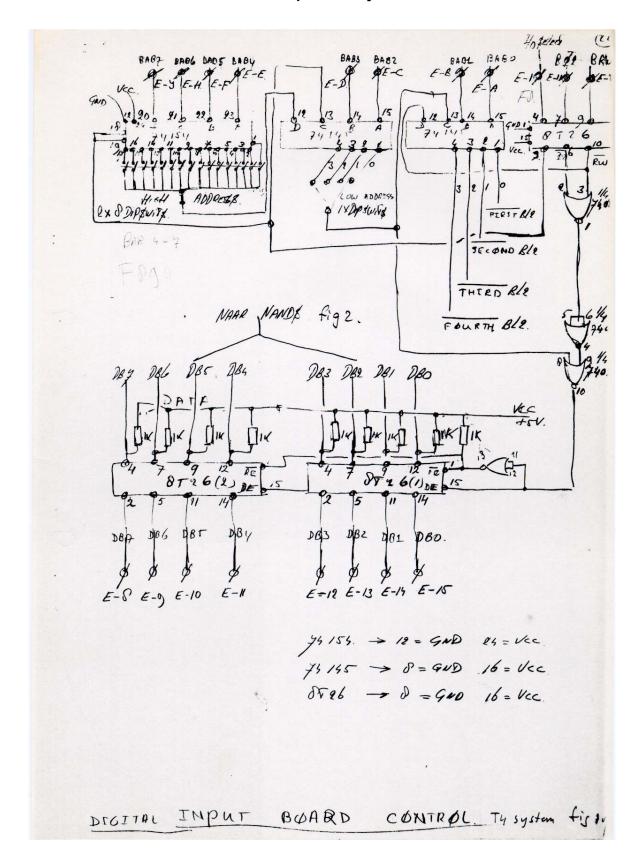
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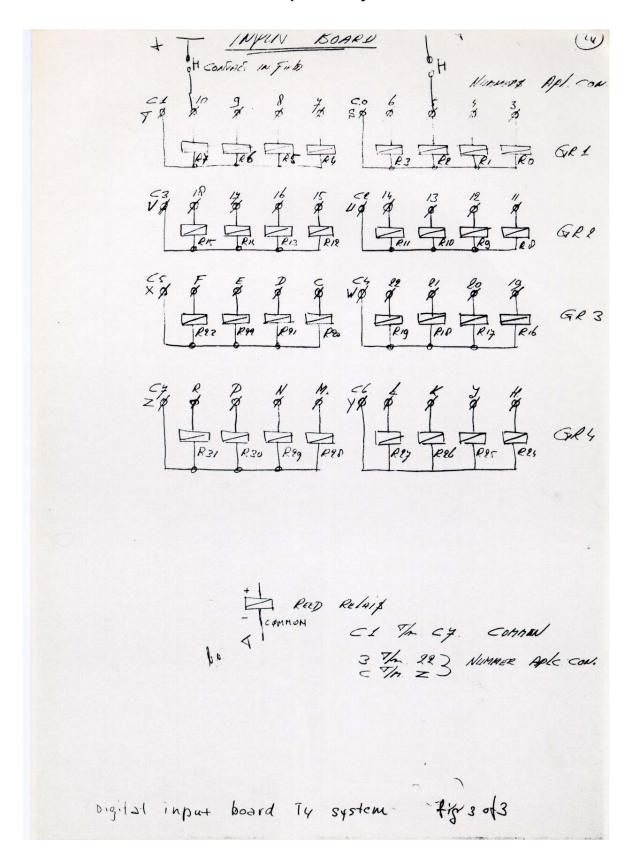
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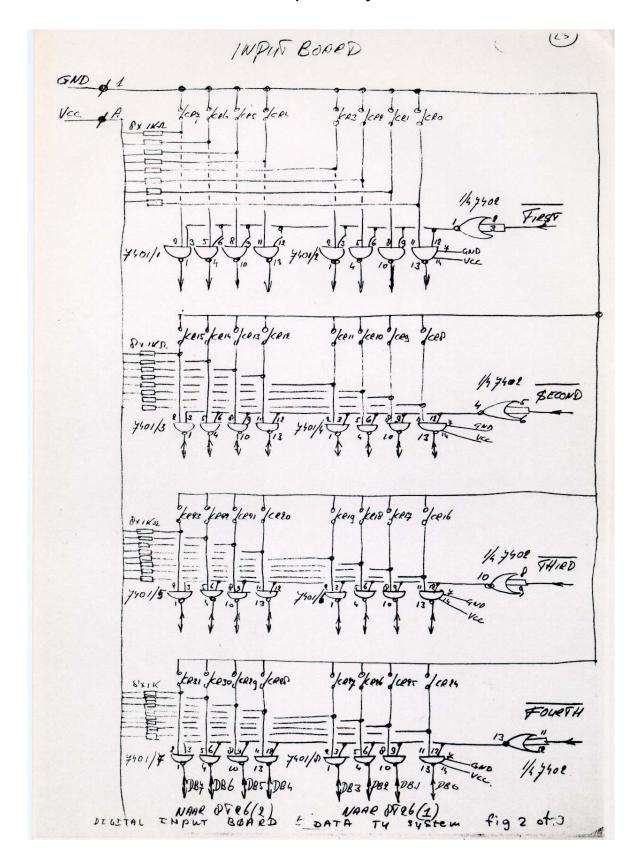
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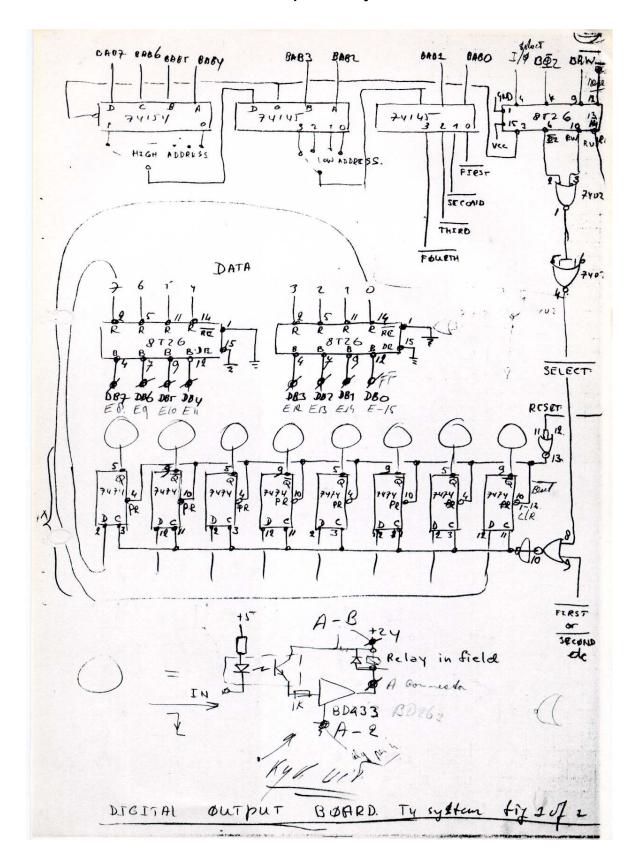
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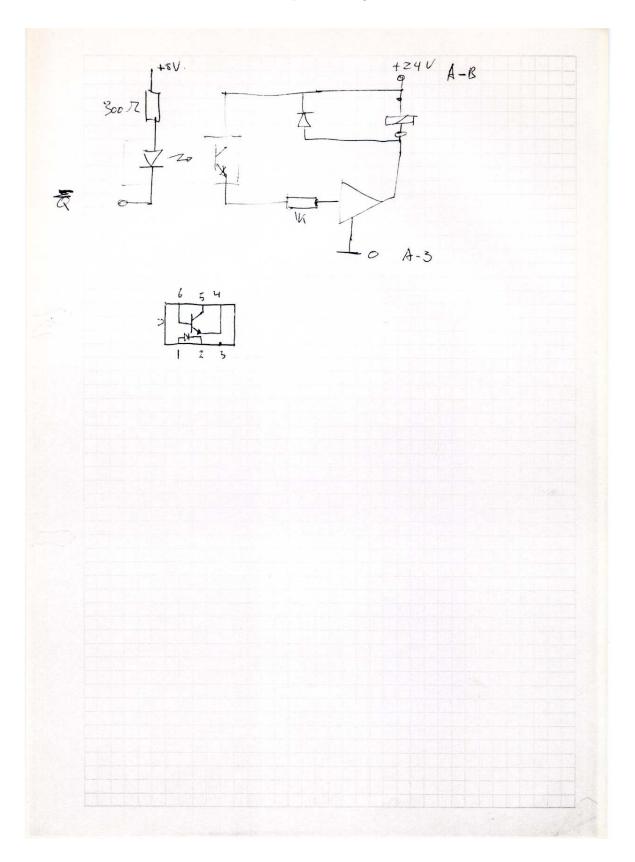
T4 KIM-1 expansion system

bovens conn.		npuz					APPL.	connec	Tor	
NR										
	,	-	input	٥			A -	3		
	2	-		,			A -			
	5		.,	2 3			A -	6		
	5	-	-1	4						
	6			5			A - A -	8		
	7	-		6			A -			
	3456789	-		7			A -	10		
	9	-		1.0			A -			
	10	-	-,	1.1			A -			
	12	-	19 -	1.2			A -			
	13	-	',	1.4			A -			
	14	_		1.5			A -			
	15	-	"	1.6			A -			
	16	-		4.7			A -	18		
	17	-		2.0			A -	19		
	18	-		2.1			A -			
	19		**	2.2 2.3			A -			
	21	-	*	2.4			A - A -			
	22	_	"	2,5			A -			
	23	-		2.6				E		
	24	-	.,	2.7			A -			
	52	-		3.0			A -			
	26	-	**	3.1			A -			
	53			3.2 3.3			A -			
	29	-		3.4			A -			
	30	-	"	3.5			A -			
	31	-	n	3.6		APPL.Ca	. A -	P		
	32	-	,,	3.7			A -	R		11111
	33 34 35 36	15		gemeenschappelig N.C	Ke input.	A-B	TA-S	Alg VO	or igals	1-2-3-4
	34	154		N.C	1	-24 V.	FA-7	Callete	and red line	
	36			N. C N. C			FA- V	A Contract		
	37	-		N, C			+A-V	1		17-18.19-3
	"						- A -		" "	21 - 22-2
							100	4 .	, ,	25-26-8
								Z ,,		29-30-3
							-24V			

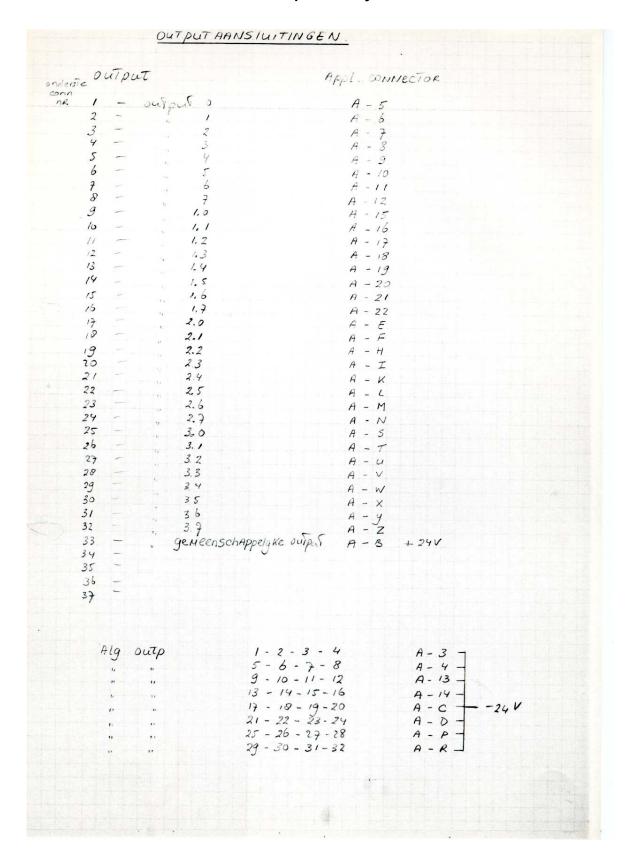
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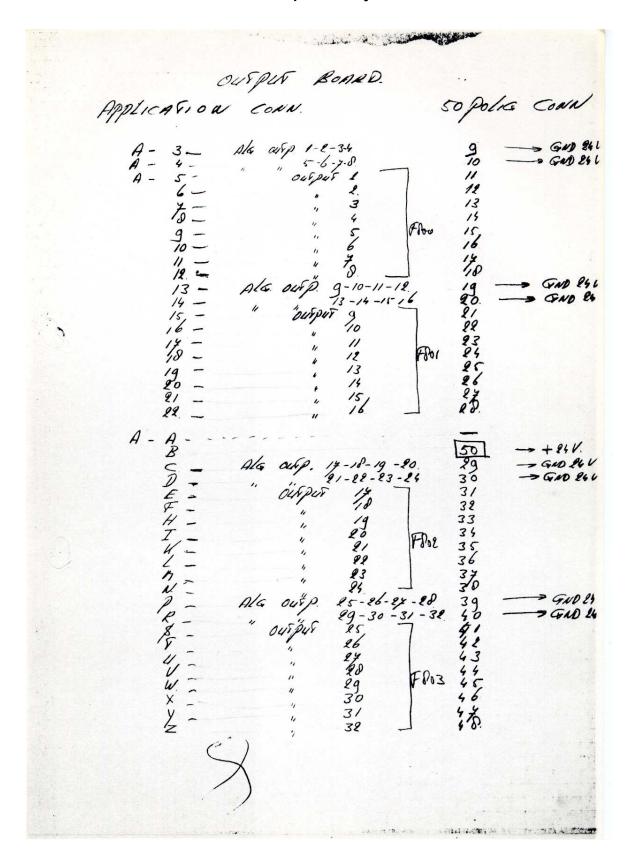
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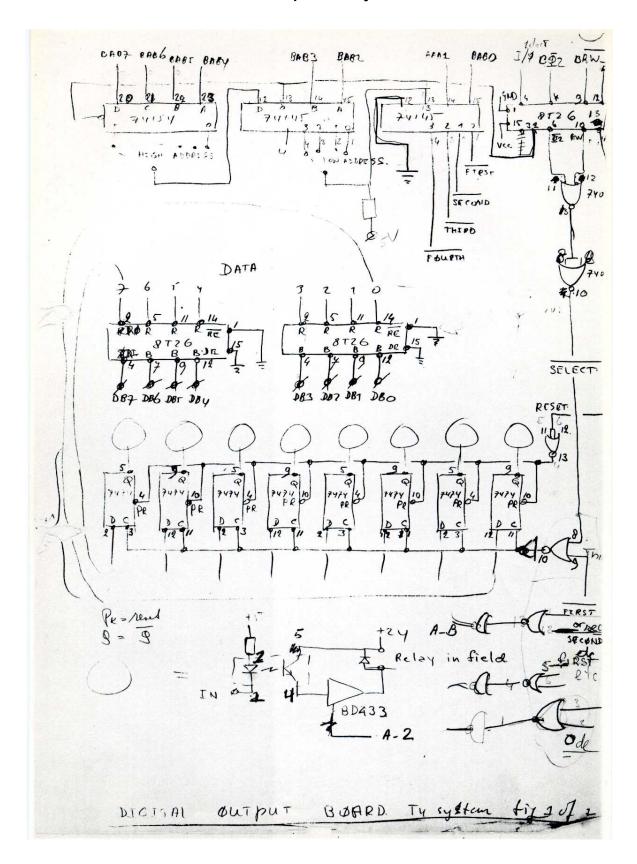
T4 KIM-1 expansion system



T4 KIM-1 expansion system



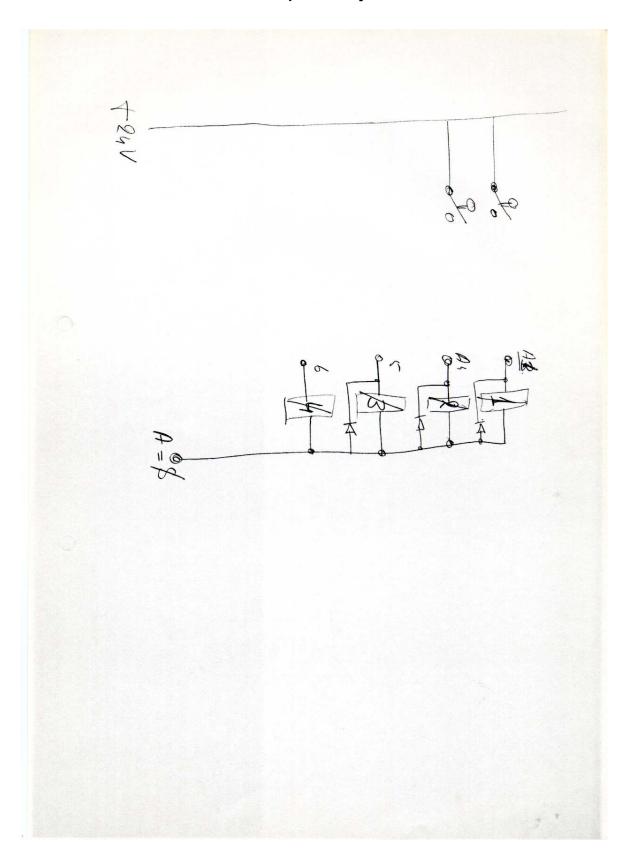
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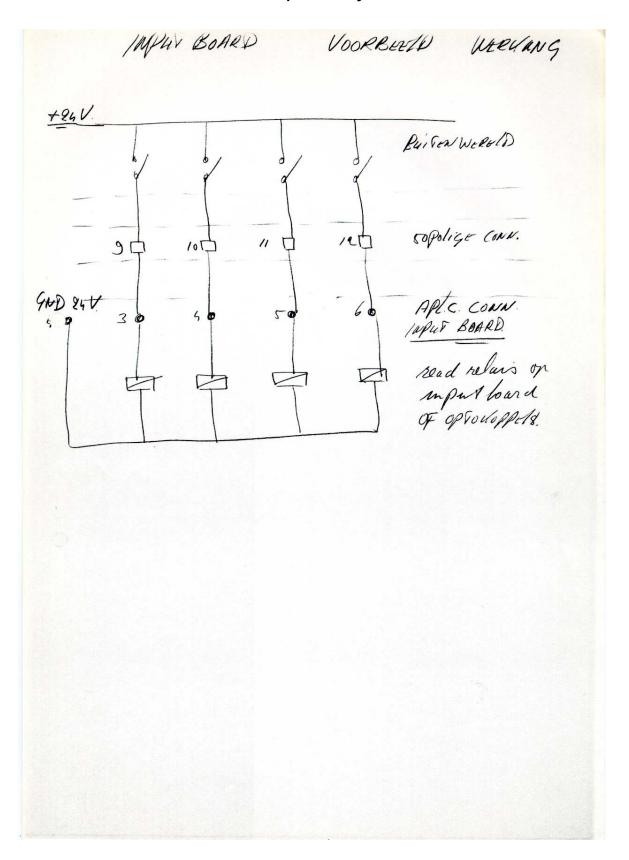
T4 KIM-1 expansion system

```
PIN
                             DESCRIPTION
        SIGNALNAME
                        HIGH IF ADDRESS = F800 - FBFF
       RDY
                        KIM- SIGNAL (PROCESSOR)
 3
        8K1
                        LOW IF ADDRESS = 2000 - 3FFF
                        KIM- SIGNAL (CALLED IRS)
        100
        8K2
                        LOW IF ADDRESS = 4000 - 5FFF
                        KIM- SIGNAL (CALLED NMI)
       NMI
                        RESET PROCESSOR AND PERSPHERALS IF LO
       PST
       DB7
 9
       DB6
 10
        DB5
                           DATA - BUS
                                        BITS
 11
       DB4
 12
       DB3
 13
       DB2
 14
        DBL
       DBO
 15
                                 ADDRESS = 6000 - 7FFF
 16
        8K3
                        LOW
                            IF
                                        . 8000- 9FFF
17
       8K4
                                         . A000 - BFFF
        8K5
                                        . C000 - DFFF
 19
       8K6
                             W
                                         " E 000 - FFFF
 20
        8K7
                                 POWER
       +5 V
 21
                        supply
       GROUND
 22
                                    ADDRESS
                                              BIT
 A
       BABO
                        BUFFERED
 B
       BAB1
                                                  1
 0
       BABZ
                                                  2
 D
       BAB3
                                                  3
 E
       BABY
                                                   456
 F
       BAB 5
 H
       BAB 6
       BAB &
                                                   78
 J
 K
 L
                                                  10
       BABQ
 M
       6A 610
 N
       B A B 11
                                                  11
       BABIZ
                                                  12
 R
       BAB13
                                                  13
                                                  14
        BAB14
                                                  15
 T
       BABI5
                       PHASE 2 PROCESSOR
 u
       B$2
                                           CLOCK
      BRW
 V
                      HIGH IF
                                READ
 W
      BRW
                       HIGH IF WRITE
       +12 V
                                POWER
 ×
                       supply
      B 02
                                PHASE 2 PROCESSOR CLOCK
                      INVERTED
        -5 V
                                POWER
                       hidding
                   EXPANSION
                                       T4 system
                          STONALS.
               KIMBUS
  BUFFERED
```

T4 KIM-1 expansion system



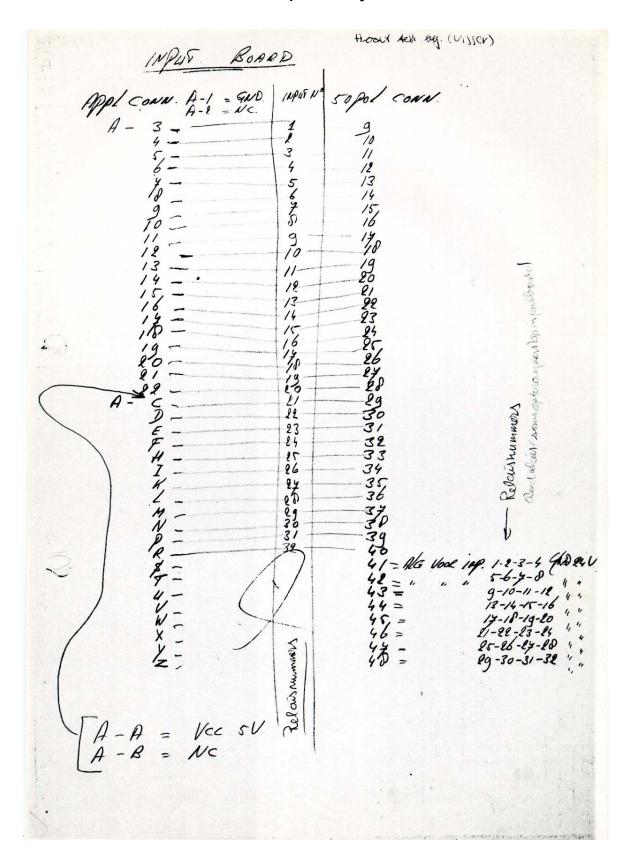
T4 KIM-1 expansion system



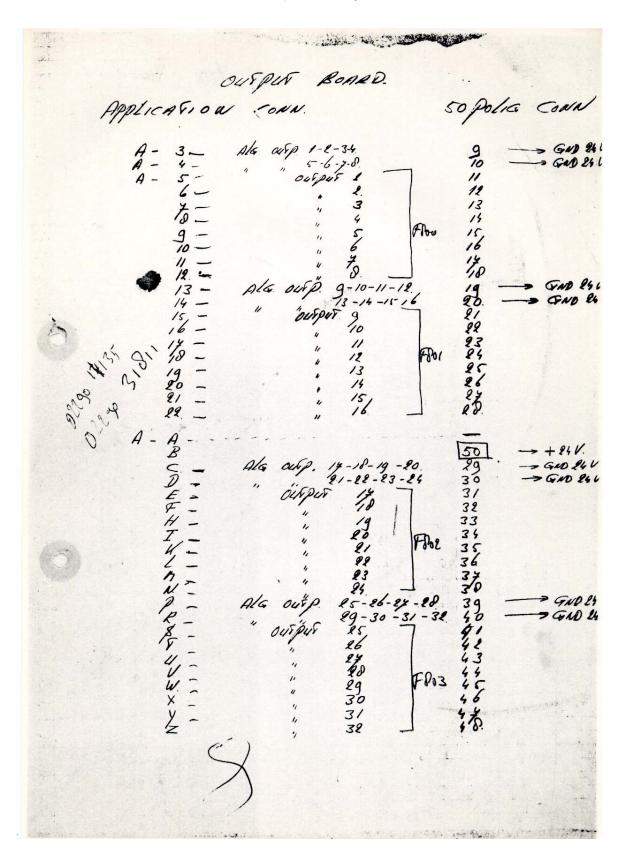
T4 KIM-1 expansion system

INPUT CONN. 50 Police	APPLICATION COON.
1NP48 1 1 2 3 4 5 6 6 4 5 6 6 4 5 6 6 4 5 6 6 4 5 6 6 4 5 6 6 6 6	A-3 -4 -5 -4 -9
12345670 901123456409012345640901234564090123456409012334	- 10 - 11 - 12 - 13 - 14 - 15 - 16 - 14
	-14 -19 -19 -20 -21 -22 -2
25 25 25 25 25 26 27 20 29 29 29 29 29 29 29 29 29	- D = F + H + H + H + H + H + H + H + H + H +
. eg eg 20 . 30 30 . 31 31 . 32 32 . 33 . 35 . 35 . 35 . 35 . 35	- Z
ALG. V 1-2-3-4	- 8 - 4 - 4 - V
17-18-19-20 - 34 V 21-22-23-24 - 46 V 25-26-27-20 - 46 V 29-30-31-32 - 49 49 Allen AAN GND 24 Volt	Application con $A - A = Vcc 5V$
	A = B = N.C.

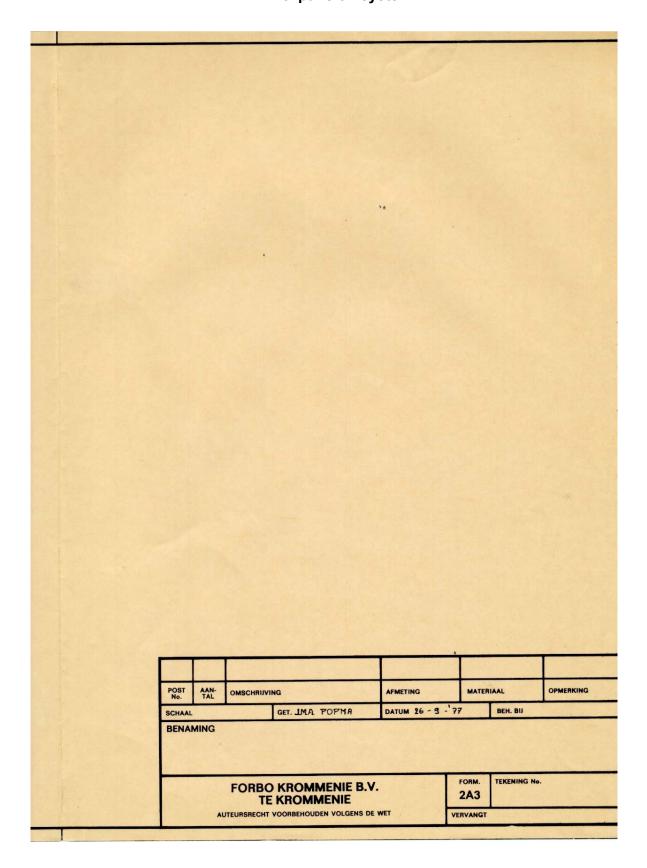
T4 KIM-1 expansion system



T4 KIM-1 expansion system



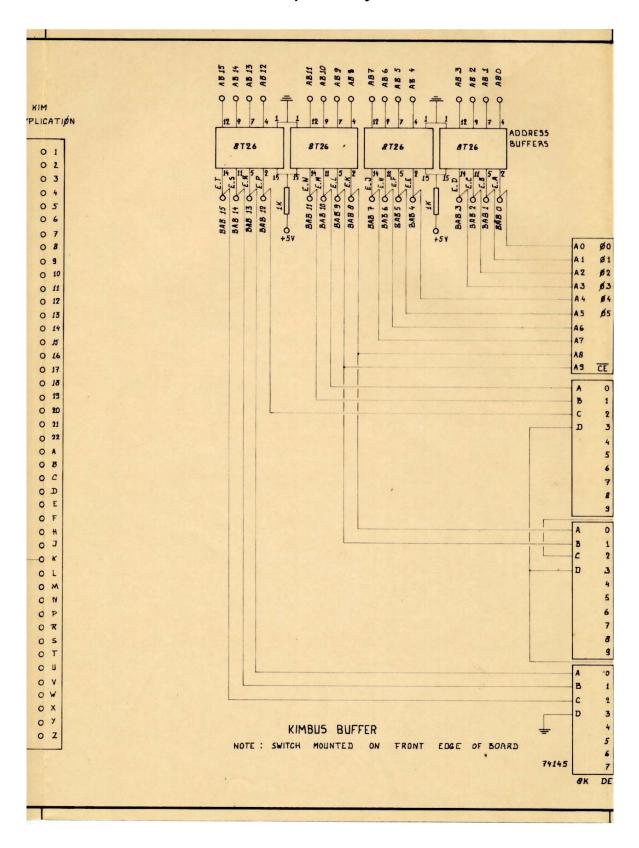
T4 KIM-1 expansion system



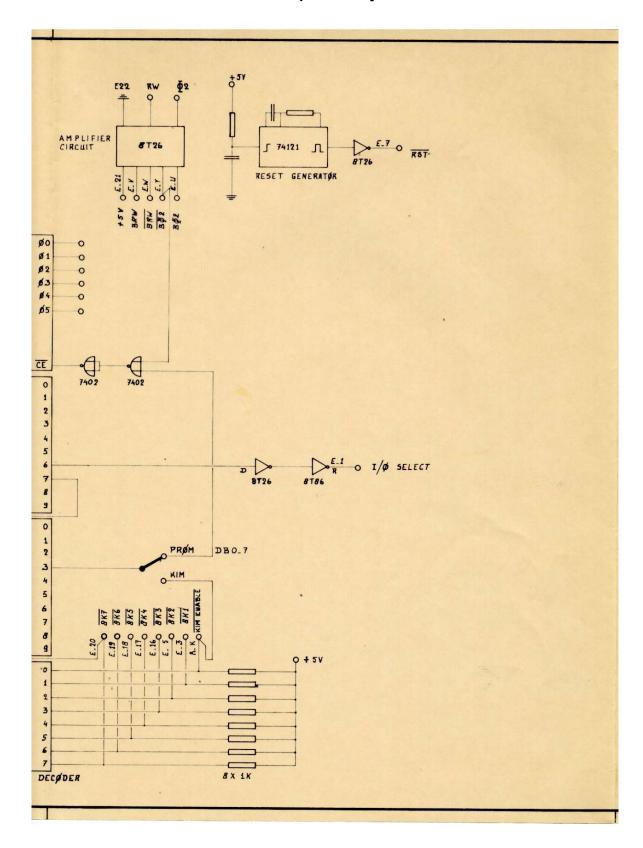
T4 KIM-1 expansion system

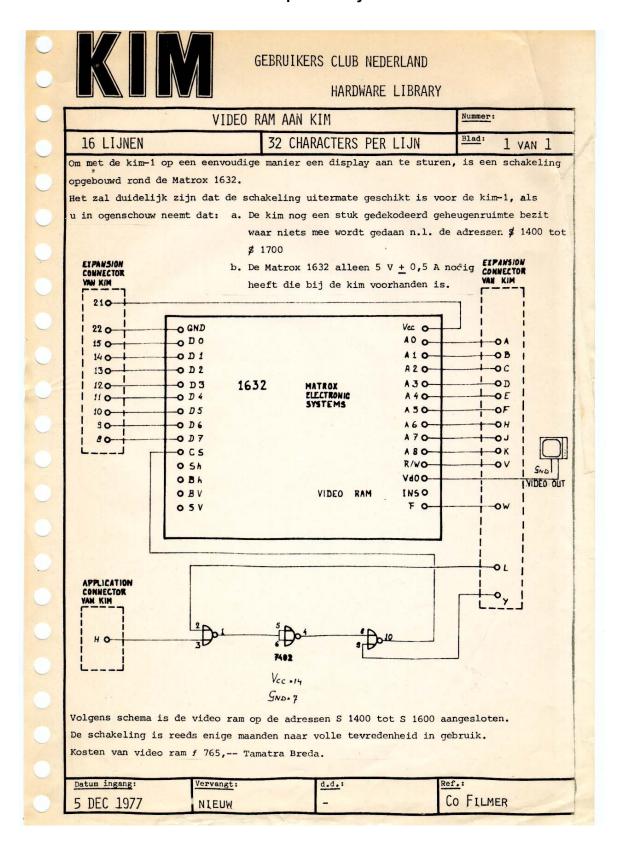
BUSBUFFER Expansión	KIM EXPANSIØN	BUSBUFFER APPLICATION	KIM APPLIC
10	0 1	01	
2 0	0 2	0 2	
3 0	0 3	0 3	
40	0 4	0 4	
50	0.5	0.5	
60	0 6	0 6	
70	0 7	0 7	
8 0	0 8	0 8	
4 3 0	0 9	0 9	
10 0	0 10	0 10	(
11 0	0 11	0 11	
	0 12	0 12	
15 O	0 13	0 13	
15 0	0 14	0 14	
16 0	0 15	0 15	
17 0	0 16	0 16	0
180	O 17 O 18	0 17	
19 0	0 19	O 18	
20 0	0 20	0 19	
21 0	0 21	0 21	
22.0	0 22	0 27	
A O	A 0	O A	
ВО	B 0	0 70	
co	co	- c	4 0
DO	Do	OD	
£ 0	E O .	O E	
FO	FO	O F	0
но	но	O H	0
j o	30	O J	0
KO	ко	ОК	
LO	10	O L	0
MO	MO	O M	0
N O	NO	- N	C
PO	PO	0 P	C
R O 5 O	RO	0 K	0
, , , , ,	5 O	0 5	. 0
u o	ПО	0 T	C
. Y O	V 0	O U	C
w o	WO	O V	0
x o	x o		1 0
70	70	0 7	0
20	zo	o z	0
	120	0 2	

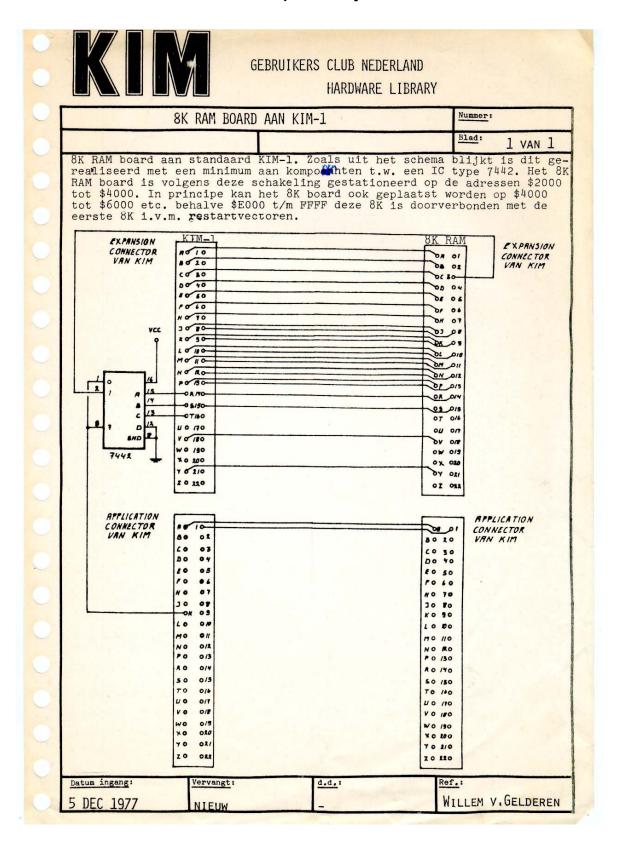
T4 KIM-1 expansion system



T4 KIM-1 expansion system







2. Het T4 systeem.

Het T4 systeem bestaat uit een aantal printen die in een rek kunnen worden geschoven. Voor elke print bevinden zich twee connectors boven elkaar in het rek. De printen in het T4 systeem worden via de bovenste connector met elkaar verbonden.(data-, adres-, en controllijnen). De onderste connector wordt gebruikt voor verbindingen buiten het T4 systeem.(inputs,outputs). De microprocessor bevindt zich op een printkaart, die in de handel is gebracht onder de naam Kim. Op deze kaart bevindt zich de microprocessor 6502 met een aantal ic benodigd voor de besturing. Via een toetsenbord met display is de Kimkaart te bedienen. Op het display wordt het adres en de data hexadecimaal weergegeven. Op het toetsenbord bevinden zich toetsen voor de hexadecimale getallen O t/m f en enkele besturingstoetsen. De volgende signalen worden door de Kimkaart op de bovenste connector gezet\$

- 1 Data DO tot en met D7
 2 Adressen AO tot en met A15
- 2 Adressen AO tot en met A15 3 Control signalen zoals \$\int 2(klokpuls), read/write, I/O select.

Voor het T4 systeem zijn onder anderen nog de volgende printkaarten ontwikkelt:

- 1 inputkaarten
- 2-Outputkaarten
- 3 8K ramkaarten
- ad1 Een input kaart ziet OV als een logische "O" en 24V als een logische "1".
- ad2 Een outputkaart geeft bij een logische "O" OV af en bij een logische "1" 24V.
- ad3 Op een 8K ramkaart kan men 8000 woorden van 8 bits wegschrijven

Dēzs kaarten worden in de volgende hoofdstukken uitvoeriger behandeld.

Met de I/O select geven we een 4line to 16line decoder vrij. Zie functietabel 3.2. Van dit ic (74154) zijn de 16 uitgangen normaal "1". Als de decoder vrij is gegeven wordt afhankelijk van de ingangsvariablen een uitgang "0" gemaakt. Als ingangsvarible zijn adreslijnen A4,A5,A6,A7 gebruikt. Deze adreslijnen hebben betrekking op het derde hexadecimale cijfer van het adres.

Voorbeeld 1: We selecteren het adres \$F823

De I/O select zal "O" zijn (F800 tot en met F8FF)

A4="0" A5="1"

A6="0"

A7="0"

Volgens functietabel 3.2 zal uitgang 2 "O" worden. Normaal gesproken is van de 16 schakelaartjes slechts een contact gemaakt. Ingang D van het volgende ic zal slechts "O" worden als de schakelaar op uitgang 2 gemaakt is.

logic

					FU	NCT	ION	TA	BLE					
NO.		INF	UT:	\$				C	UT	PUT	8			_
	D	C	В	A	0	1	2	3	4	5	6	7		
0	L	L	L	L.	L	н	н	н	н	н	н	н	н	н
1 '	L	L	L	н	н	L	н	н	н	н	н	н	н	н
2	L	L	н	L	н	н	L	н	н	н	н	н	н	н
3	L	L	H	H	н	н	н	L	н	н	н	н	н	н
4	L	н	L	L	н	H	н	H	L	н	н	н	н	н
5	L	н	L	н	н	н	н	н	н	L	н	н	н	н
6	L	н	н	L	н	н	H	н	н	н	L	н	н	н
7	L	н	н	н	н	н	н	н	н	н	н	L	н	н
8	H	L	L	L	н	H	н	н	н	н	н	н	L	н
9	н	L	L	H	н	н	н	н	н	н	н	н	н	L
	н	L	н	L	н	н	н	н	н	н	н	н	н	Н
0	н	L	н	H	н	H	н	н	н	н	H	н	н	н
INVALID	н	H	L	L	н	H	H	н	н	н	н	н	н	н
3	н	H	L	н	н	H	н	н	н	н	н	н	н	н
=	H	H	н	L	н	н	н	н	н	н	н	н	н	H
	н	н	н	н	н	н	н	н	н	н	н	н	н	н

H = high level (off), L = low level (on)

Functietabel 3.2 74154 4 line to 16 line decoder.

logic

		INP	UTS										OUT	PUTS							
G1	G2	D	С	8	A	0	1	2	3	4	6		7		•	10	11	12	13	14	-
L	L	L	L	L	L	L	н	H	н	н	н	н	н	н	н	н	н	н	н	н	-
L	L	L	L	L	H	н	L	H	H	H	H	н	H	H	-	H	H	H			
L	L	L	L	H	L	н	H	L	H	H	H	H	H	H	н	H	н	н	H	н	
L	L	L	L	н	н	н	н	H	L	н	H	H	н	H	H	H		-	H	H	
L	L	L	н	L	L	н	H	н	H	L	н	н	H	H	H	+	H	H		н	,
L	L	L	н	L	H	H	H	H	н	H	L	H	H	+	+		H	-	H	н	
L	L	L	H	H	L	H	H	H	н	H	H	L	н	н	н	н	H	н	H	н	1
L	L	L	H	н	н	H	H	н	н	H	H	H	L	H			H	H	H	H	
L	L	н	L	L	L	H	H	н	н	H	H	н	+	L	-			H	H	H	*
L	L	н	L	L	H	н	H	н	H	H	H	н	H	H	L	н	H	H	н	H	
L	L	н	L	H	L	н	H	н	н	н	H	н	н	н	н	L	H	н	н	H	
L	L	н	L	н	н	н	H	н	н	H	н	н	H	H	H	H	L	H	H	H	j
L	L	н	н	L	L	н	H	н	н	+	H	н	H	H	H	H	H	L	H	H	
L	L	н	н	L	H	н	H	H	H	H	H	н	H	H	H	H	H	H	L	H	
L	L	H	H	H	4	н	H	н	н	H	H	H	H	н	н	H	H	H	н	L	
L	L	н	н	H	н	н	H	н	н	H	H	H	H	н	H	H		H	H	H	4
L	н	×	×	×	×	н	H	н	н	H	H	H	+	H	H	н	н	-	H		
н	L	×	×	×	×	н	н	н	н	+	+	H	H	H	H	н	н	H	H	H	
H	н	×	×	×	×	н	н	н	н	н	H	н	H	H	н	H	н	н	н	H	

Functietabel 3.3 74145 4 line to 10 line decoder.

Opmerking: H = "1" L = "0" 1

-5-

Het functiediagram van het volgende ic (74125) is gegeven in functietabel 3.3. Werzien uit de tabel dat een van de gebruikte uitgangen oas "0" kan worden als zowel de ingang Cals D "0" is. Dit is het geval als het adres overeenkomt met die in de voorgaande trap is ingesteld. Met de schakelaars op de uitgang van dit ic kunnen weer een gedeelte van het adres_ instellen.

Voorbeeld 2. We willen hetzelfde adres selecteren als in voorbeeld 1
Dit adres was \$F823.
Stel dat het voorgaande trap zodenig ingesteld is
dat D "O" wordt.
Uit het adres volgt dat: A2="O"
A3="O"

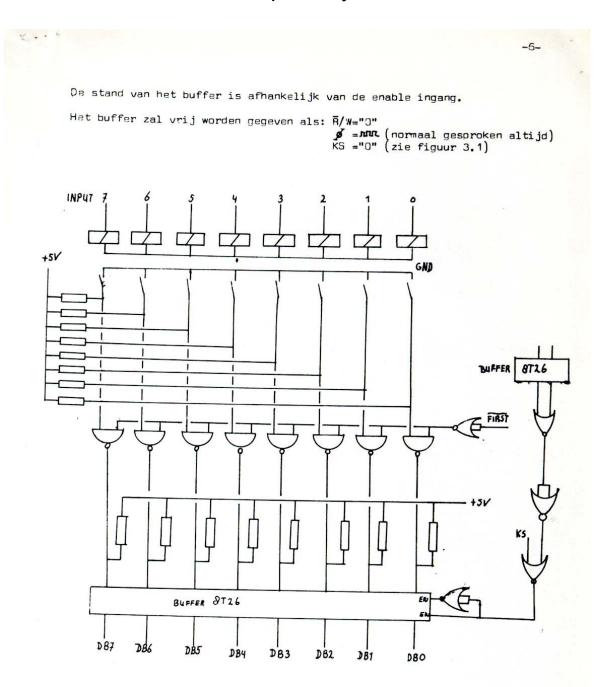
Uit de functietabel volgt nu dat uitgang 0 "0" wordt. Als de schakelaar op uitgang 0 gemaakt is zal de ingangen C en D van het er opvolgende ic "0" zijn. Voor het laatste ic geldt hetzelfde verhaal als voor het voorgaande ic. Nu worden de uitgangen echter gebruikt om een van de 4 woorden aan te sturen. Afhankelijk van AO en A1 zal het 1e,2e,3e of 4e woord aangestuurd worden.

3.2 Inputkaart

Aan een inputkaart kan men 32 inputs aanbieden. Hierbij is een spanning van OV een "O" en een spanning van 24V een "1". De 32 inputs worden in 4 woorden van 8 bits gescheiden. Hieronder zal ik de vewerking van een woord behandelen. De overige 3 woorden lopen hier min of meer parallel aan. De schakeling is getekend in figuur 3.4. Met de inputs wordt een relai aangestuurd. Het schakelcontact van het relai is aangesloten op een spanning van OV en 5V. Als het schakelcontact gemaakt wordt trekt deze de ingang van de nand naar 0 volt ("0"). Bij open contact is dit 5 volt ("1"). Op de andere ingang van de nand is de selectie van het woord aangesloten. Bijvoorbeeld FIRST. Als de gewenste adres op de adresbus staat zal deze "O" gemaakt zijn(zie adressering). Dit signaal wordt geinverteerd op de ingang van de nands aangeboden. Hiermee wordt de nand als invertor vrij gegeven. Met het relai was echter ook al een inversie toegepast, zodat op de uitgang van de nands de niet geinverteerde inputs verschijnen. De uitgangen van de nands gaan naar een buffer 8T26. Op de ingang van dit ic is met behulp van weerstanden en and functie gekreëerd. Hierdoor kan men de uitgangen van de nands van de andere woorden aan elkaar knapen. De uitgangen van de niet aangestuurde woorden zijn "1". Het aangestuurde woord zal zodoende aan de ingang van het buffer worden aangeboden.

De uitgang van het buffer heeft 2 standen: 1 De standen aan de ingang. 2 De stand waarin hij niks

beinvloed.

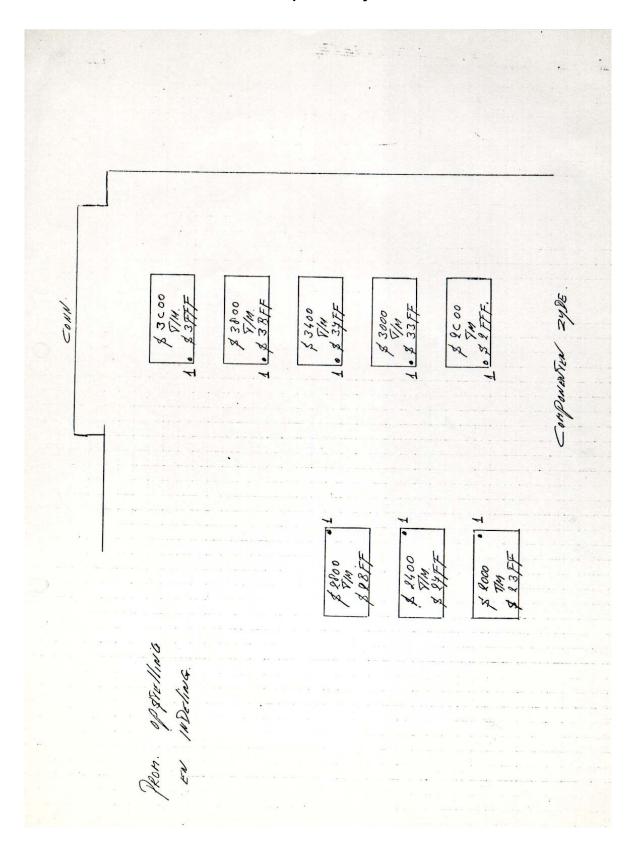


Figuur .4 Inputkaart

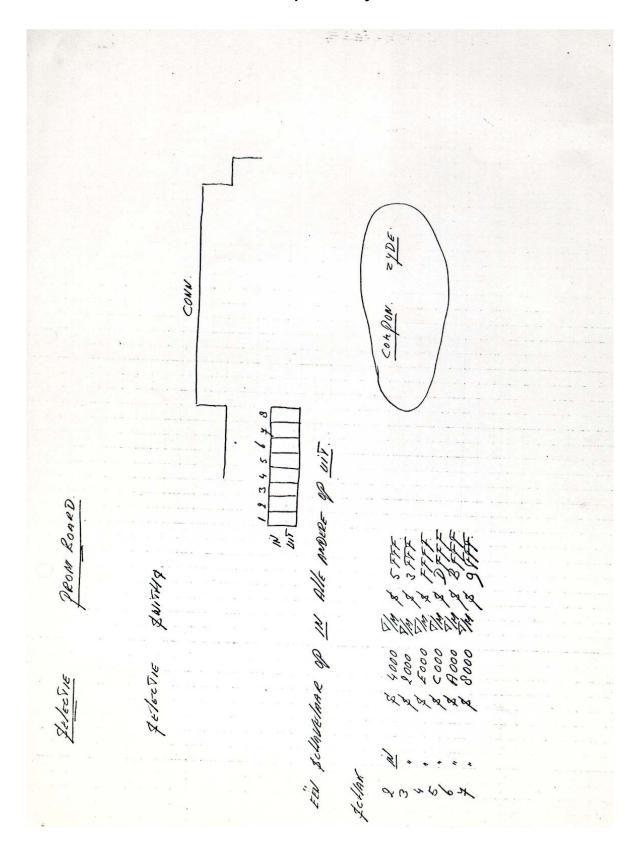
T4 KIM-1 expansion system

			Bylage alf-T4 maps actres Selelatio gegevens
	TOR PROGRAM. , HIM.	ADRES IN PROM BUFFER BUNRD	10N. 81. 8 2000 00.
	409. MONIFOR	The Strike	
BUFFER BOARD		No.	Fee Banes - 5
	Jethavet	& colore	R. Series S. Ser

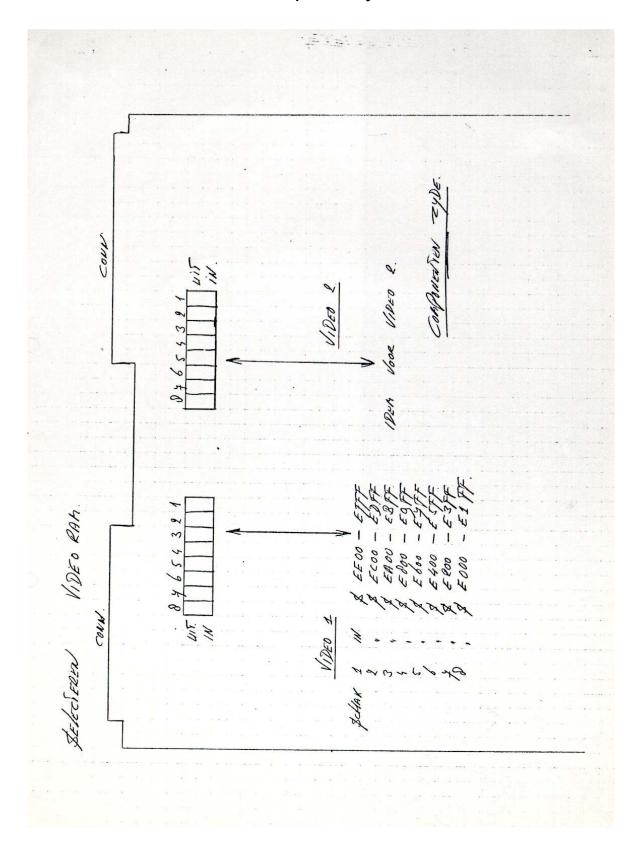
T4 KIM-1 expansion system



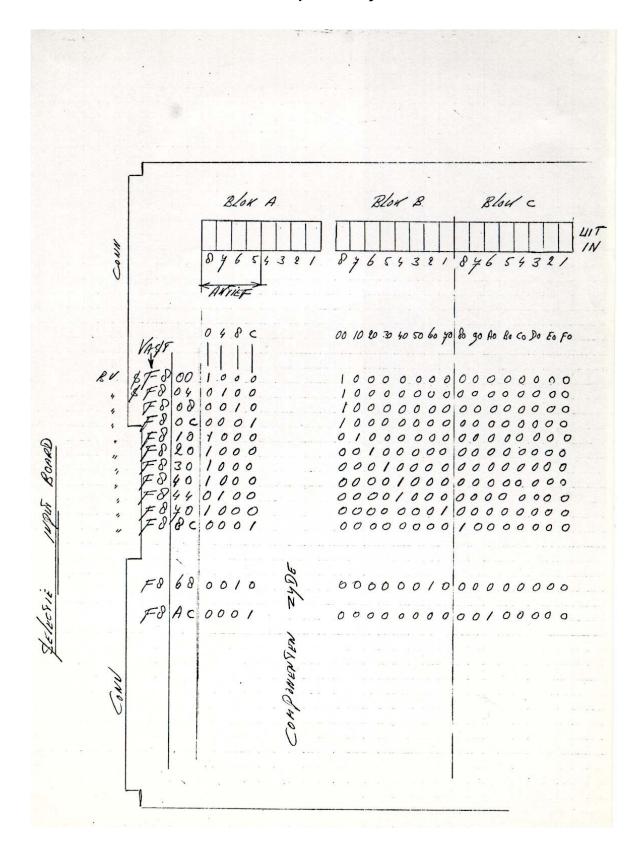
T4 KIM-1 expansion system



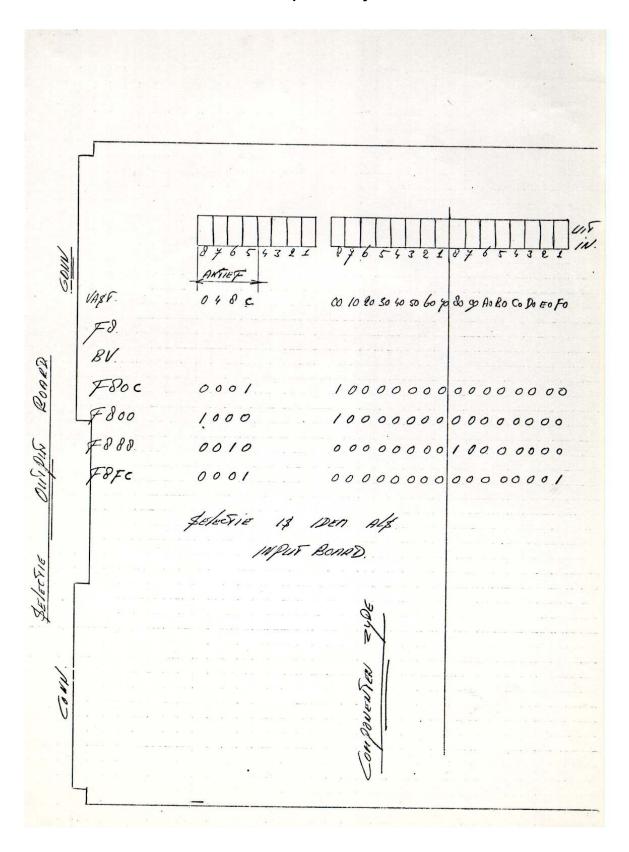
T4 KIM-1 expansion system



T4 KIM-1 expansion system



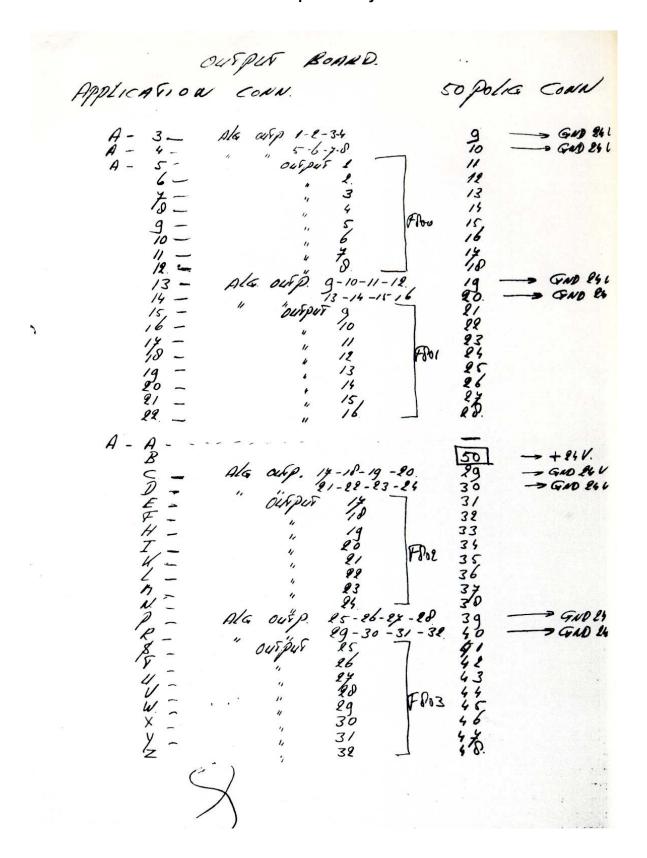
T4 KIM-1 expansion system



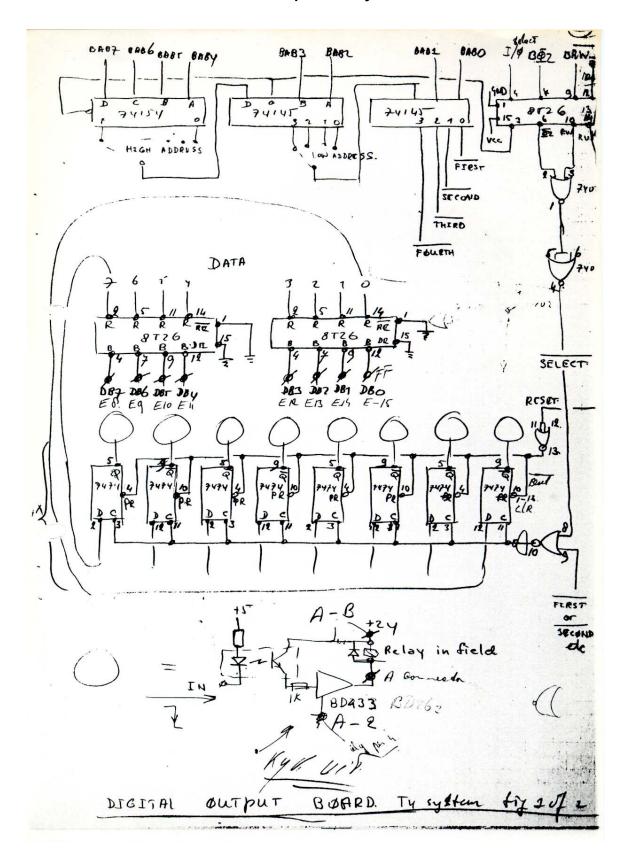
T4 KIM-1 expansion system

```
OUTPUT AAMSLUITINGEN
                                        AFIL DIMECTOR
 2
                   7
                  1.0
                  1.1
                  1. 2
 13
                 14
                                            A - 19
 14
                 1.5
                                           A - 20
 15
                 1.6
 15
                 1.7
                                           A - 22
F - E
A - F
17
                 2.0
                 2.1
19
                 2.2
                                              - H
                 23
21
                2.4
22
                2.5
23
                2.6
              2.7
24
                                           A - N
25
           3-0
                                             - 5
26
                3. 1
27
               3. 2
                                             - u
                3.3
28
29
               34
30
                35
31
                36
                3.7
32
33
              geneenschappelijke outpers
                                                  + 24V
34
35
36
37
                            1-2-3-4
                      5-6-7-8
                          13 - 14 - 15 - 16
                                                      A - 14 -
                         17 - 18 - 19 - 20
21 - 22 - 23 - 24
25 - 26 - 27 - 28
                                                     A - C -
A - D -
A - P -
                          29-30-31-32
```

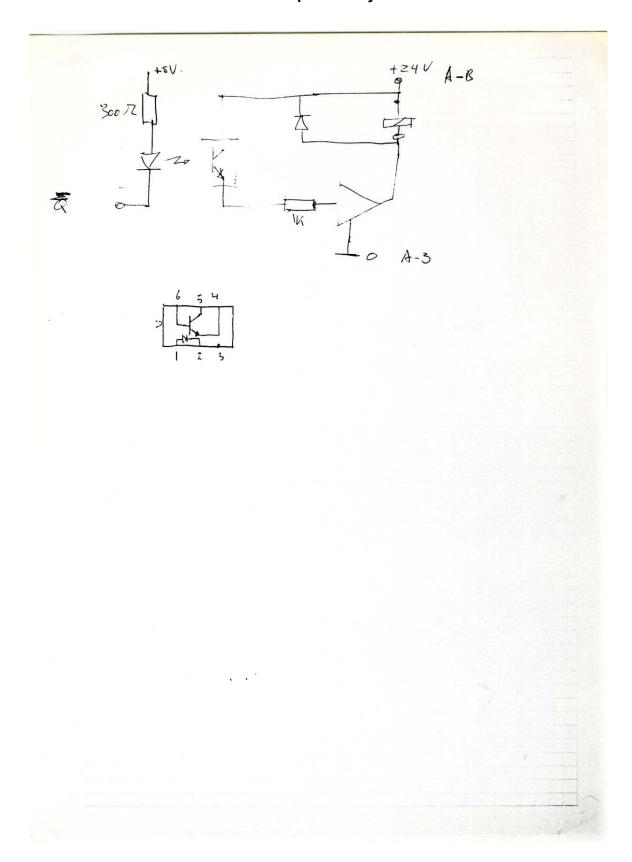
T4 KIM-1 expansion system



T4 KIM-1 expansion system



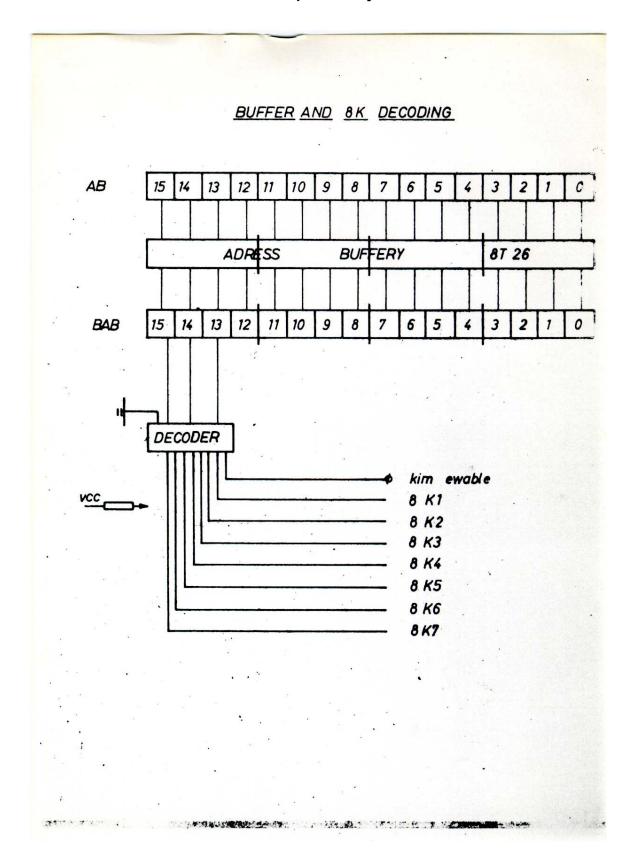
T4 KIM-1 expansion system



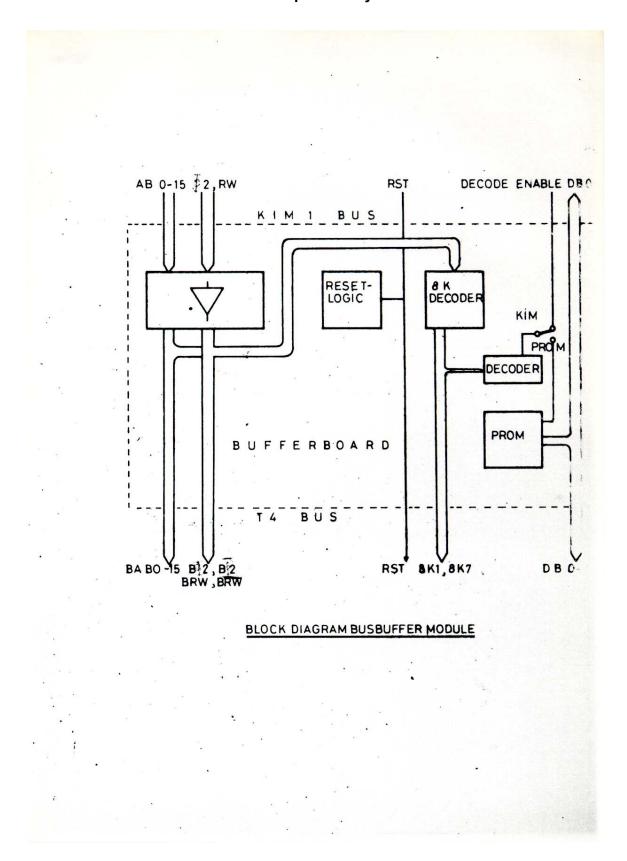
T4 KIM-1 expansion system

```
PIN
                              DESCRIPTION
         SIGNALNAME
                        HIGH IF ADDRESS = F800 - FBFF
       IN SEIFEF
        RDY
                         KIM- SIGNAL (PROCESSOR)
                         LOW IF ADDRESS = 2000 - 3FFF
 3
        8K1
                         KIM- SIGNAL (CALLED IRS)
        100
        8K2
                         LOW IF ADDRESS = 4000 - 5FFF
                         KIM- SIGNAL (CALLED NMI)
        NMI
                         RESET PROCESSOR AND PURIPHEPALS IF LO
        PST
        DB7
 9
        DB6
10
        DB5
                           DATA - BUS
                                         BITS
11
        DB4
 12
        DB3
 13
        DB2
 14
        DBL
        DBO
 15
 16
                         LOW
                             TE
                                  ADDRESS = 6000 - 7FFF
        8K3
17
                                           8000- 9FFF
        8K4
                                            ADDO - BFFF
        8K5
19
                                            COOO - DFFF
        8K6
                                            E 000 - FFFF
 20
        8K7
        +5 V
                                  POWER
 21
                         supply
 22
        GROUND
                                     ADDRESS
                                               BIT O
 A
        BABO
                         BUFFERED
 B
                                                    1
        BAB1
 C
        BABZ
 D
        BAB3
 E
        BABY
 F
        BAB 5
                                       "
 H
        BAB 6
                                       11
        BAB7
BAB8
 J
 L
        BAB9
 M
        6A 610
        BAB 11
 N
        CABIZ
 P
 R
        BAB13
                                                    13
 S
       BAB14
                                                    14
 T
        BABI5
 u
V
       B 1 2
                       PHASE 2 PROCESSOR CLOCK
       BRW
                       HIGH IF READ
      BRW
                        HIGH IF WRITE
 ×
                       SUPPLY POWER INVERTED PHASE
       +12 V
       B 02
                                         2 processor clock
        -5V
                                 POWER
                       ru ppiy
                    EXPANSION
                                        T4 system
  BUFFERED
                KIMBUS
                           SIGNALS.
```

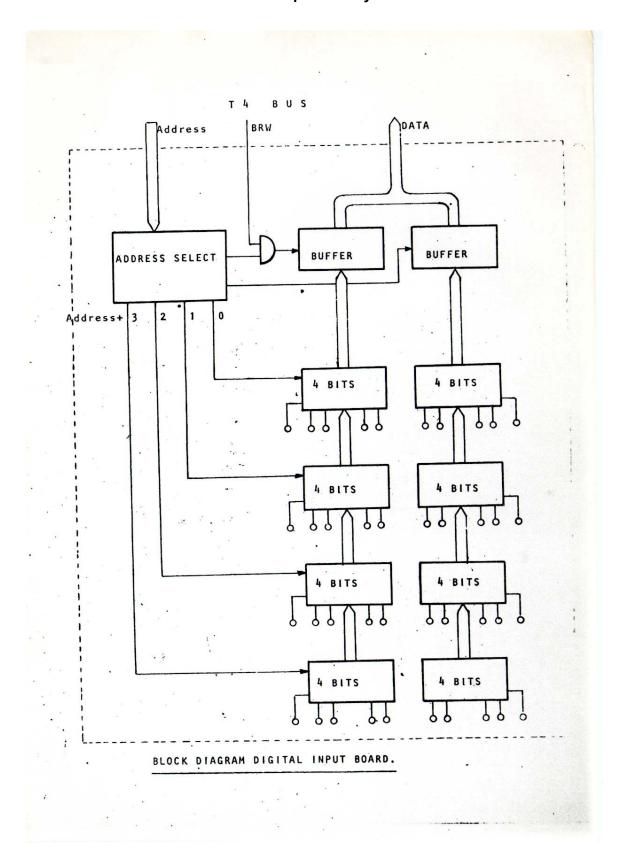
T4 KIM-1 expansion system



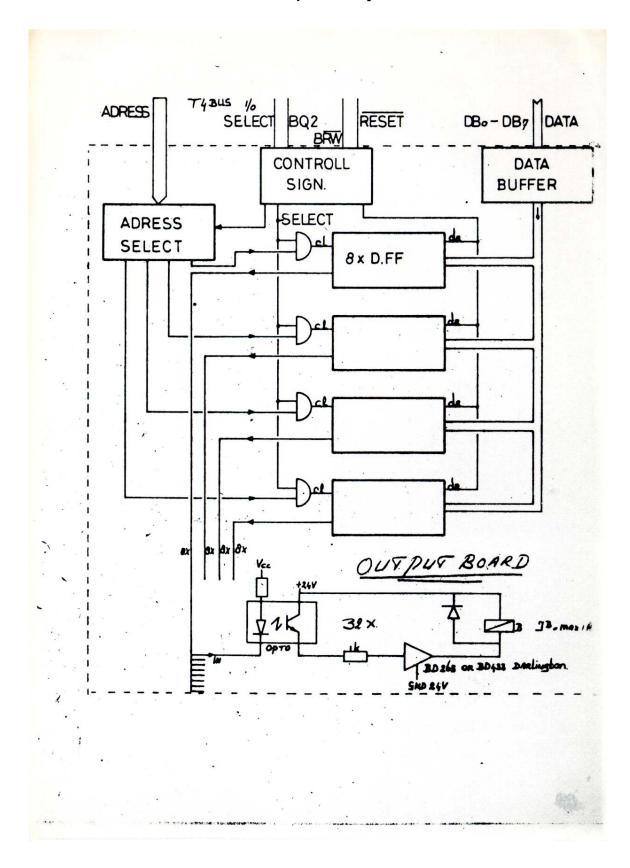
T4 KIM-1 expansion system



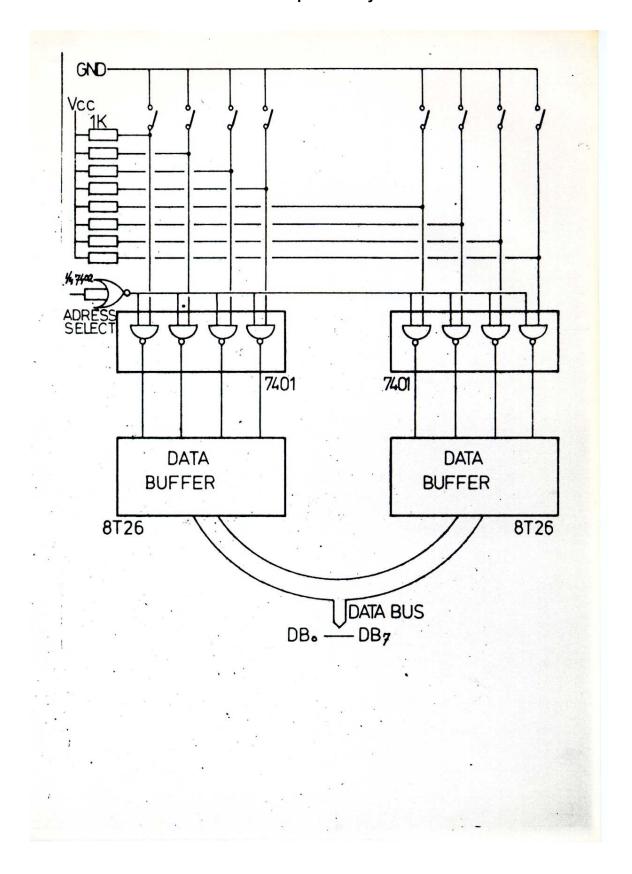
T4 KIM-1 expansion system



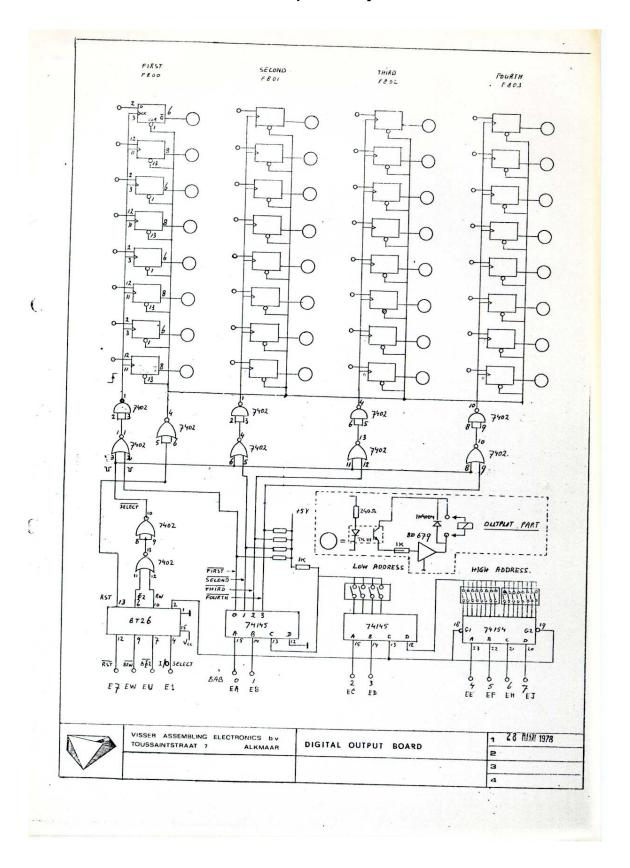
T4 KIM-1 expansion system



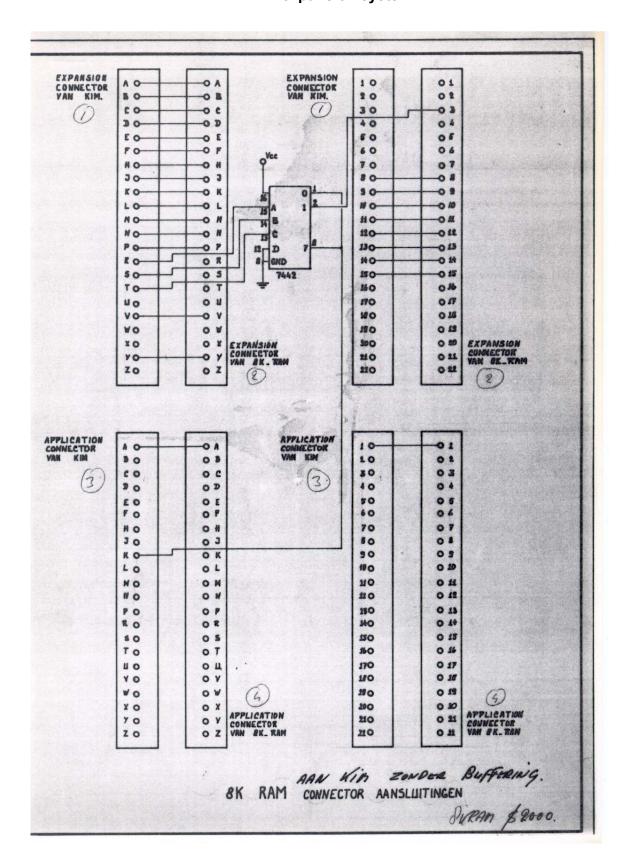
T4 KIM-1 expansion system



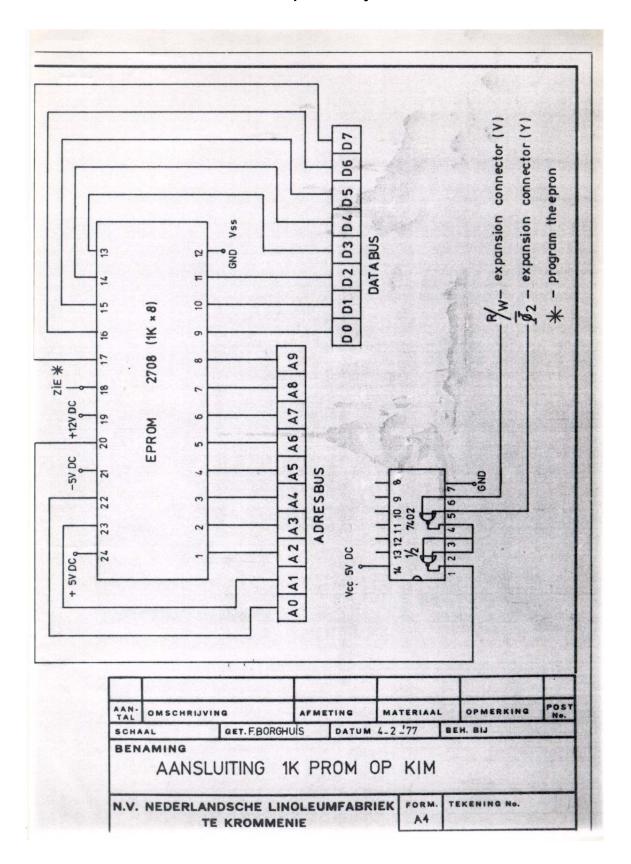
T4 KIM-1 expansion system



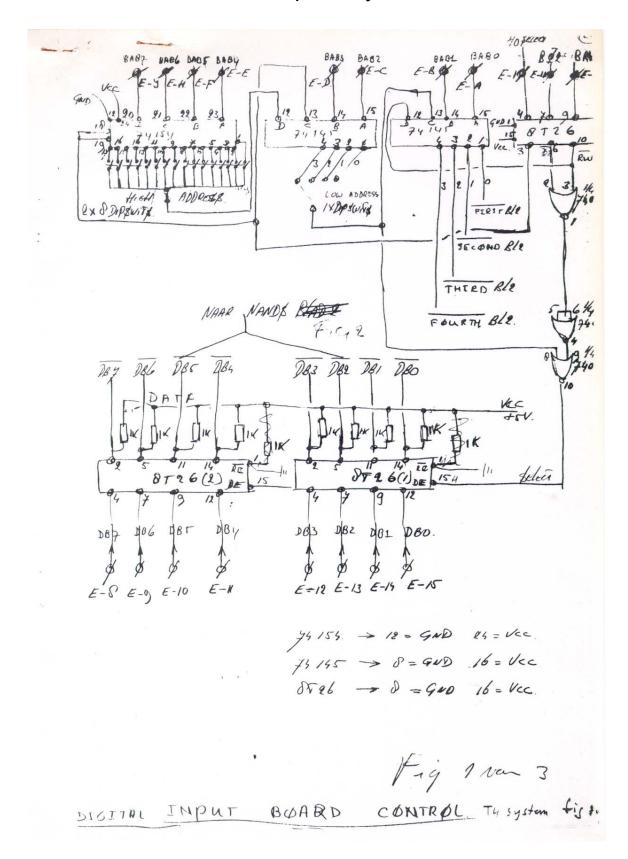
T4 KIM-1 expansion system



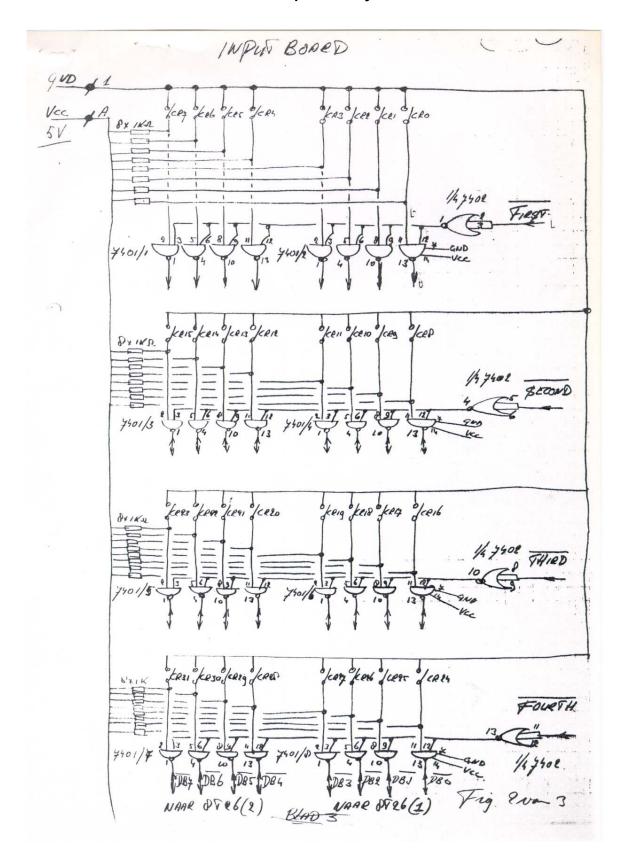
T4 KIM-1 expansion system



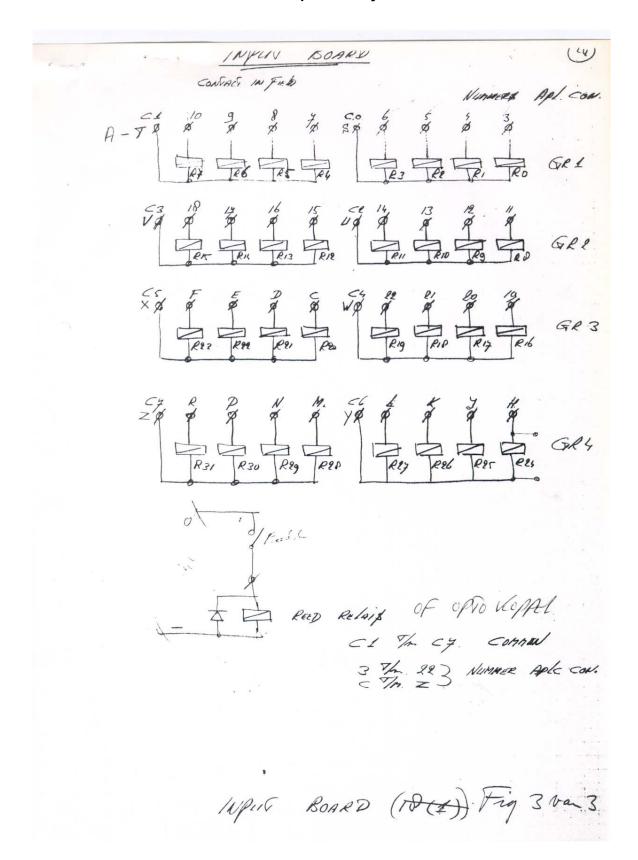
T4 KIM-1 expansion system



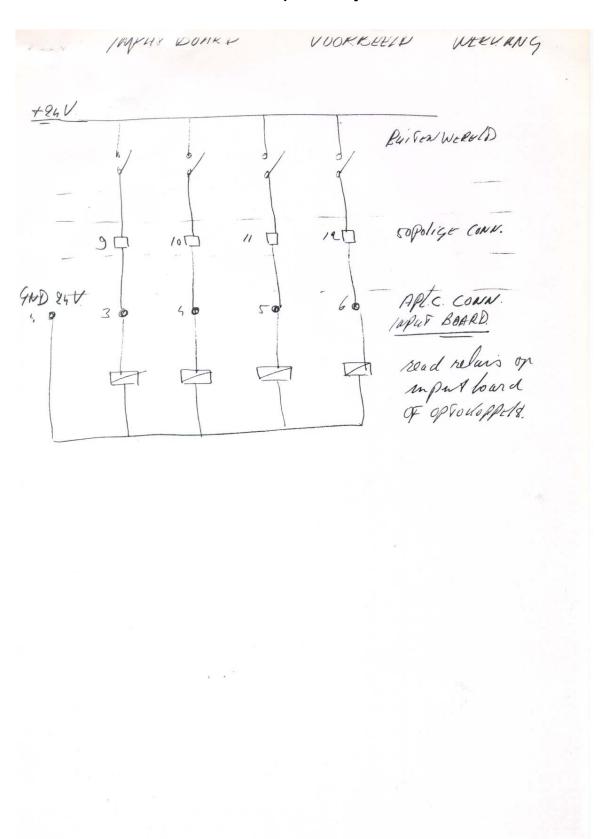
T4 KIM-1 expansion system



T4 KIM-1 expansion system



T4 KIM-1 expansion system



T4 KIM-1 expansion system

	- INTERN	KOARD				
APP	A-3-		5000/	CONN.		
/	A - 3 -		9,0			
	6- 40-		// /2 /3 /4 /5			
	900		15			
	12 -		19			
	15 -		20 21 22			
	18-		25			
	20-		1901234664890123466			
	4-6		29			
	F		32 33 34			
			35			
	N =		370339			
	7-		41	AlG Vool	109. 1-2-3-4 5-6-4-0 9-10-11-12	/-94V
	4		42345/		13-14-15-10	
	X -		4640		13-14-15-16 13-14-15-16 13-18-13-18 15-16-13-16 19-30-31-3	9 "
		4 PT				

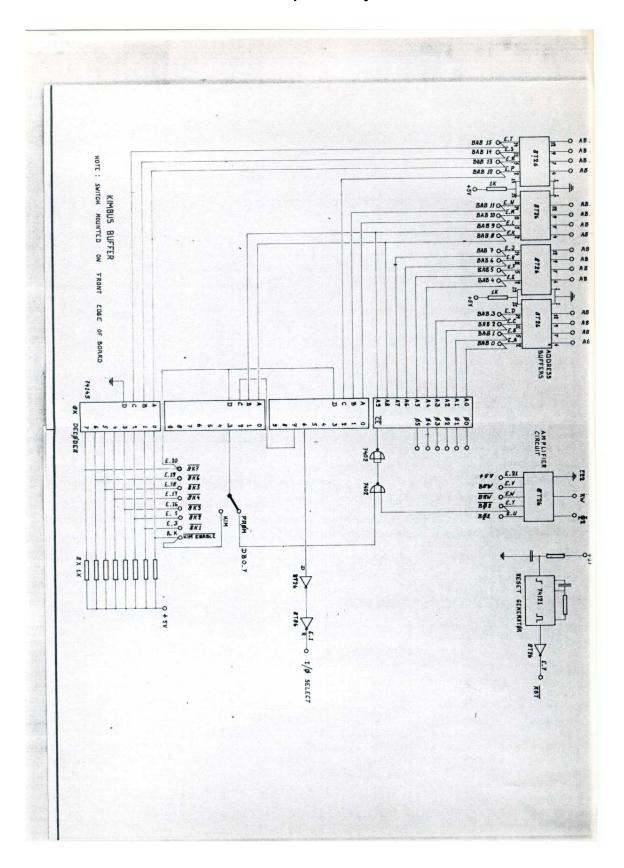
T4 KIM-1 expansion system

	INPUT CONN.	Application Coan.
1NP49	12345670910118134564709012345649990123333	A-4567091011R3355618109011RCDEFHYKLMNPR
	35 36 37 39 39 39 5.6.7.0 41 9-10-11-18 42 13-14-15-16 43 14-15-19-20 44 21-22-23-24 45 21-20-31-32 45 29-30-31-32 45 49 49 49 49 49 49 49 49 49 49	Application con A - A = Vcc 5V A - B = N.C.

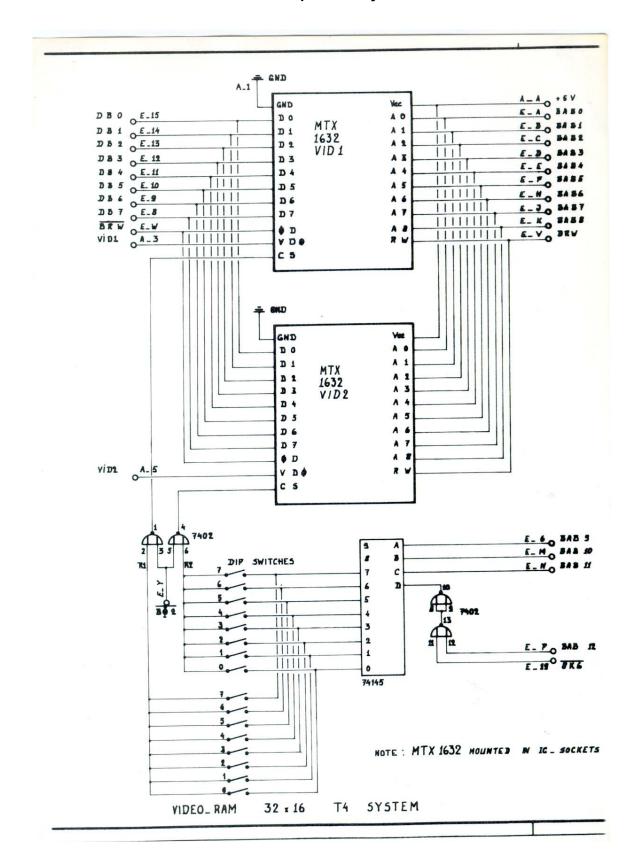
T4 KIM-1 expansion system

BUSBUFFER	кім	BUSBUFFER	KIM
EXPANSION	EXPANSION	APPLICATION	APPLICATION
10	0 1	0 1	0 1
20	0 1	0 2	0 2
30	0 3	0 3	0 3
40	0 4	0 4	0 4
50	0 5	0 5	. 05
60	0 6	0 6	0 6
70	0 7	0 7	0 7
. 80	0 8	0 8	0 8
9 0	0 9	0 9	0 9
u o	0 10	0 10	0 10
12 0	O 11	0 11	0 11
15 0	0 13	0 12	0 12
# 0	0 15	O 13	0 13
15 0	0 15	0 15	0 14
160	0 16	0 16	0 16
170	0 17	0 17 .	0 17
18 0	0 18	0 18	0 18
19 0	0 19	0 19	Pt 0
20 0	0 20	0 20	0 20
21 0	0 21	0 21	O 21
220	O 22	0 22	0 22
A O	A 0	. O A	O A
30	80	0 8	0 8
DO	C O	0 C	0 0
E 0	EO	O D	О. Д
FO	FO	0 F	O E
110	HO	0 #	O F
10	10	O J	0 H
KO	ко	O K	o K
LO	LO	O L	O L
MO	MO	- M	0 M
NO	N O	- N	ON
PO	PO	- O P	OP
RO	RO	O #	OR
50	50	0 5	0 5
· ro	ТО	ОТ	от,
40	и о	O 11	0 11
Y 0	V 0	- v	0 4
A O	WO	WO	0 W
X O	X O	0 X	o x
ZO	z o	0 Y	0 7
	20	o z	0 Z

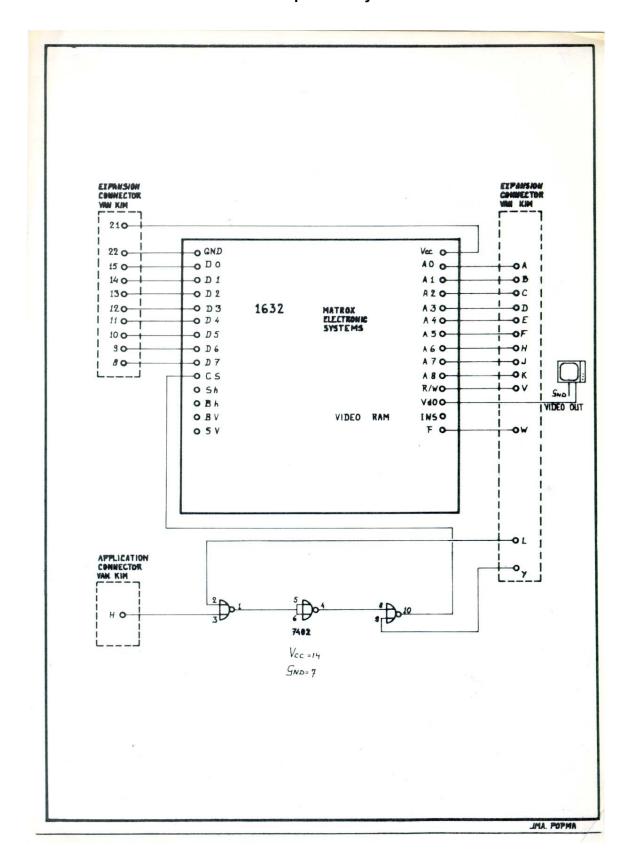
T4 KIM-1 expansion system



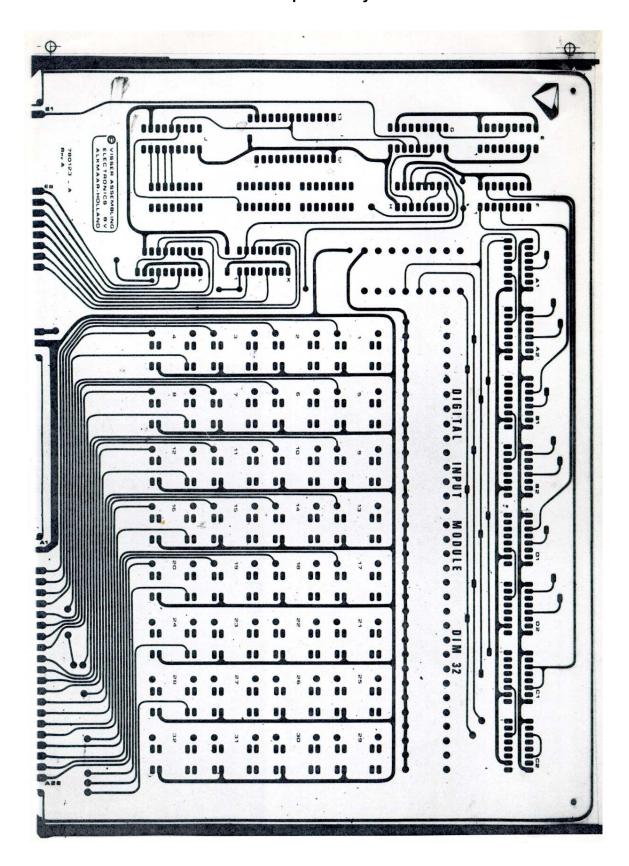
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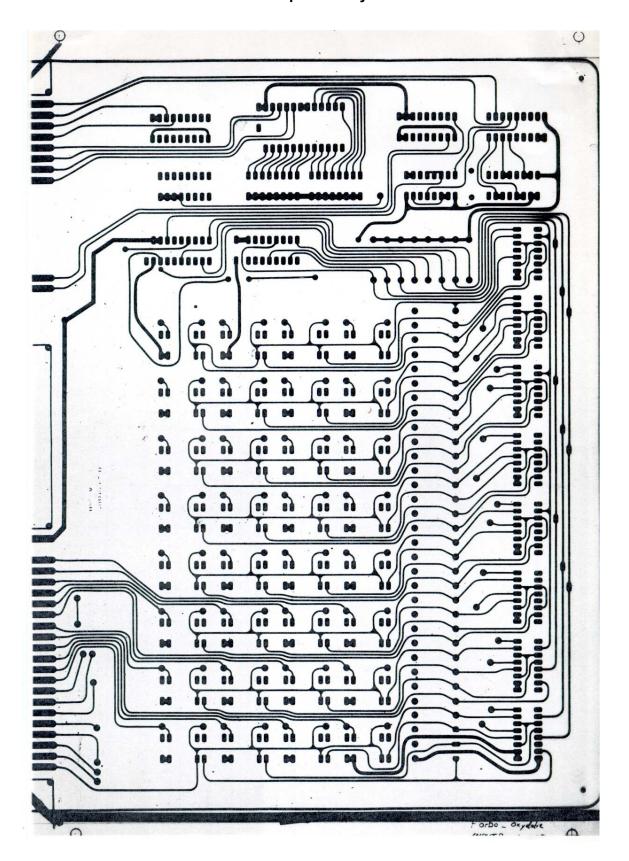
T4 KIM-1 expansion system



T4 KIM-1 expansion system



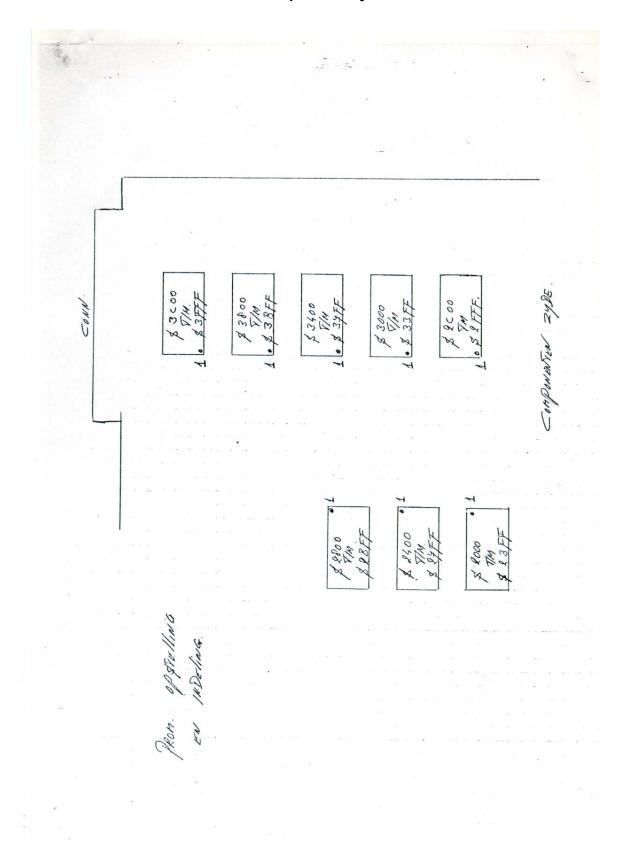
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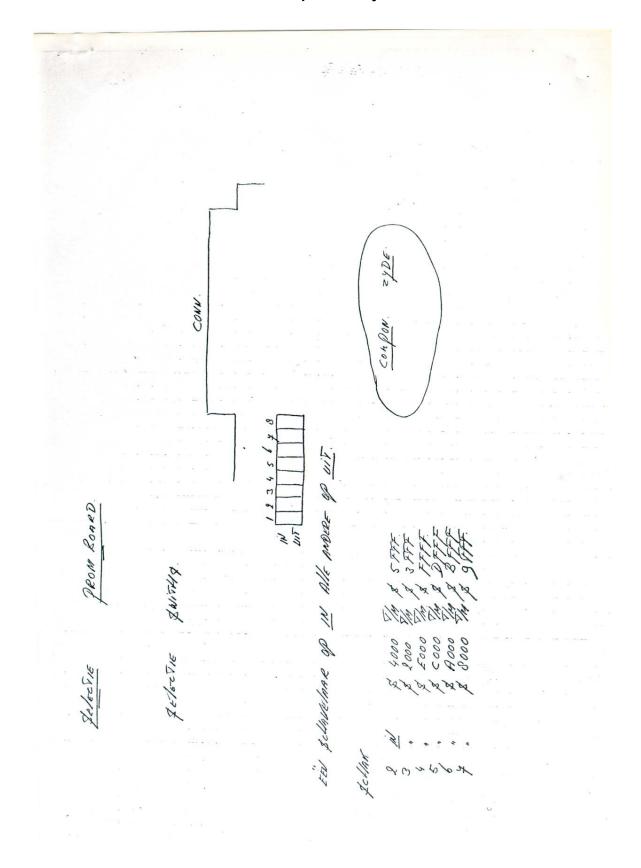
T4 KIM-1 expansion system

			Bylage ad	tres Selelitio gegoveur
	MONISOR PROGRAM. "HIM., STARE ADRER IN PROM BUFFER BOARD	- FFFFF	FFFC LOW 80 8 8000 00.	
BUGFER BOARD	011420 G.	- Jess	1 VESOR	
	g chasel	De Deun Buf.		

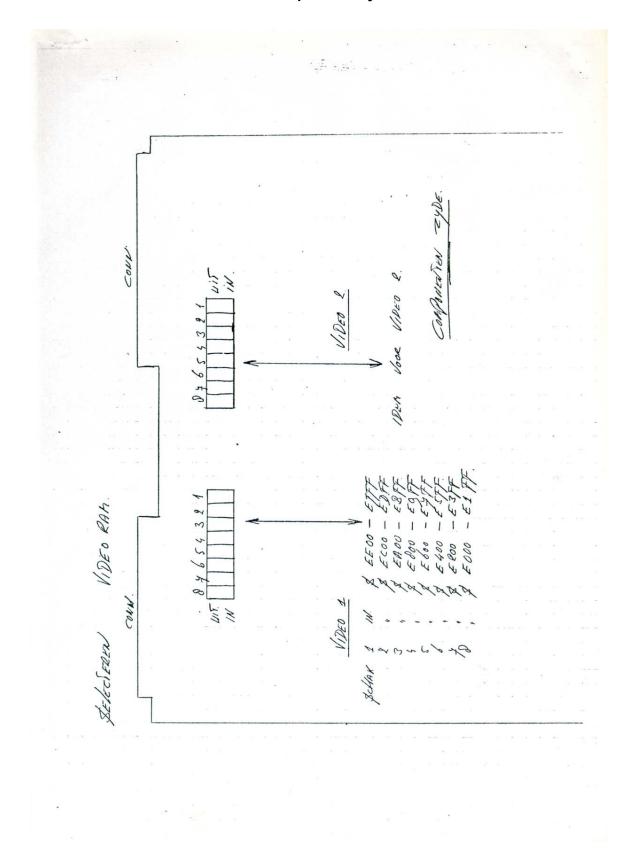
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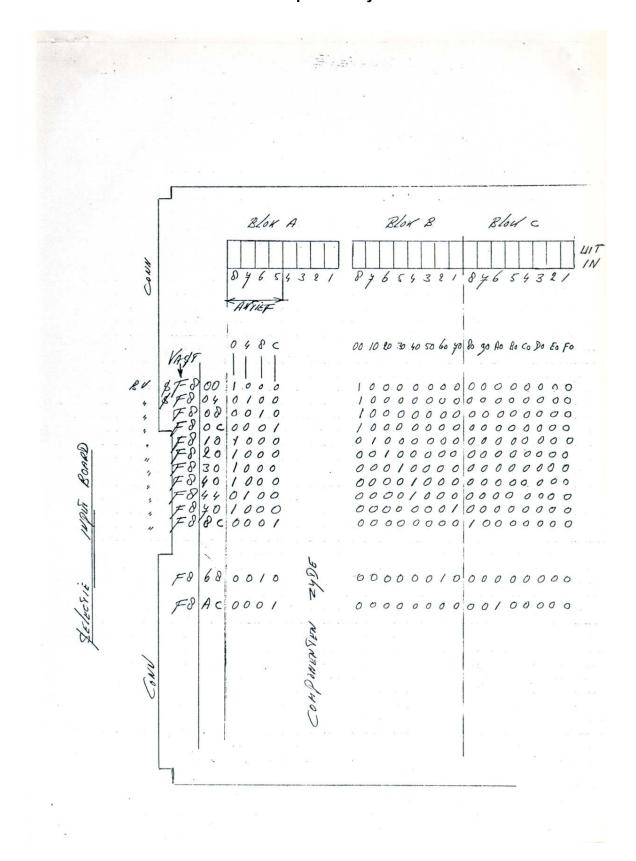
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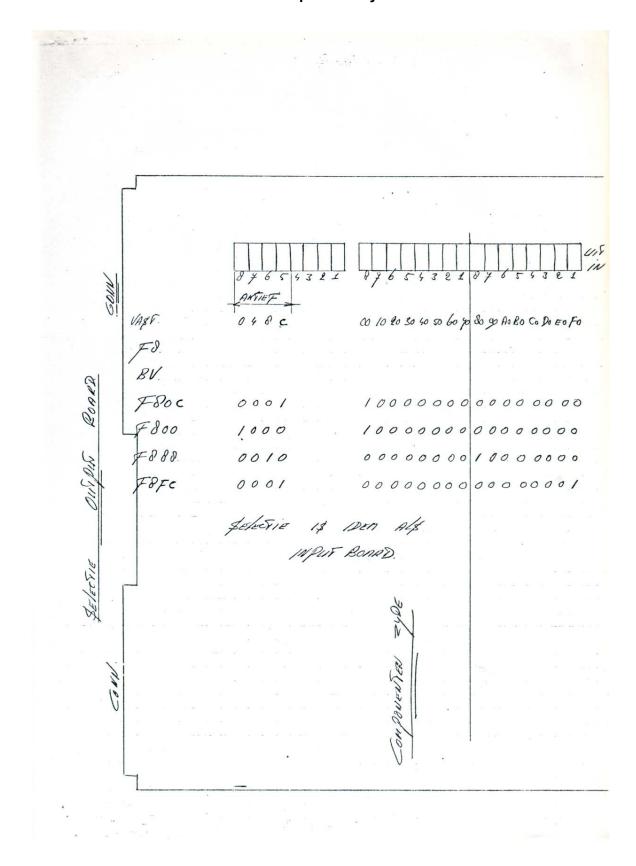
T4 KIM-1 expansion system



T4 KIM-1 expansion system



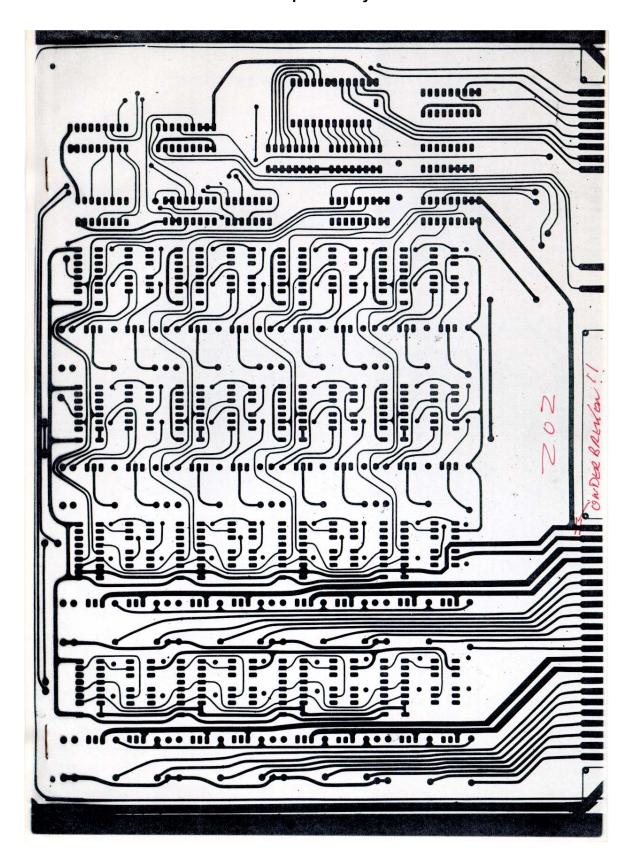
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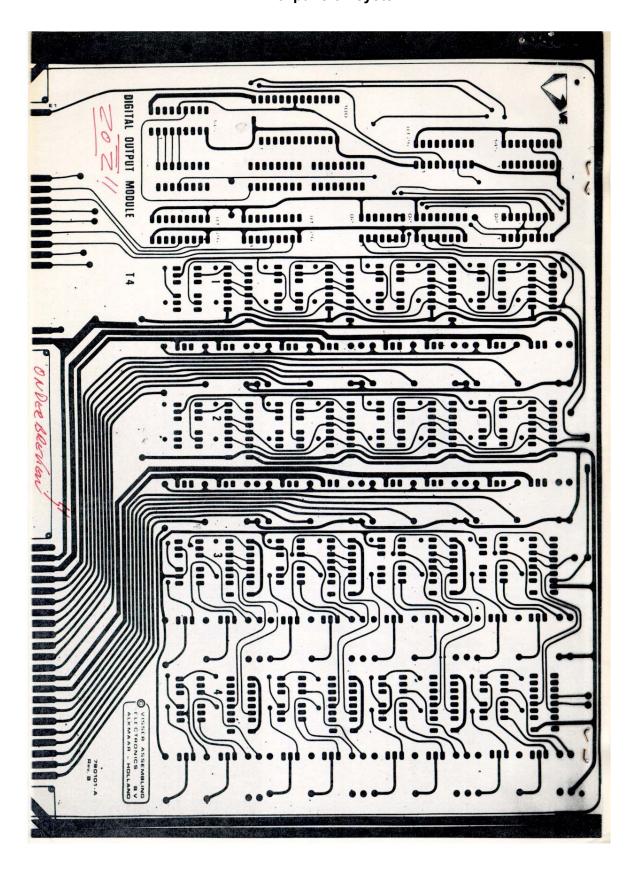


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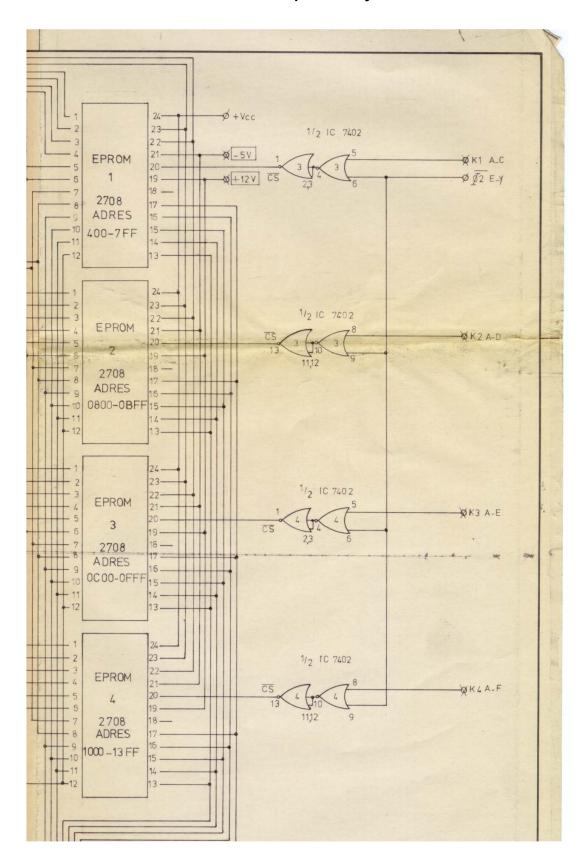
By OUT PUT MODELLE 9 BANER ONDER BREVER ZOALS IN ROOD MANGEGENEW. OP /AY 045 DIT I. N. M. EXVERNE 24 V = Spanning GElyK

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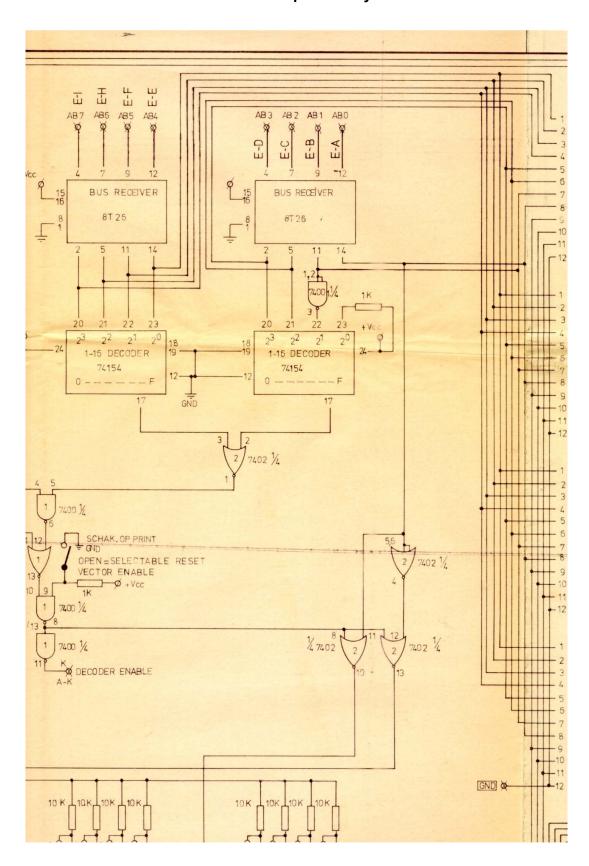




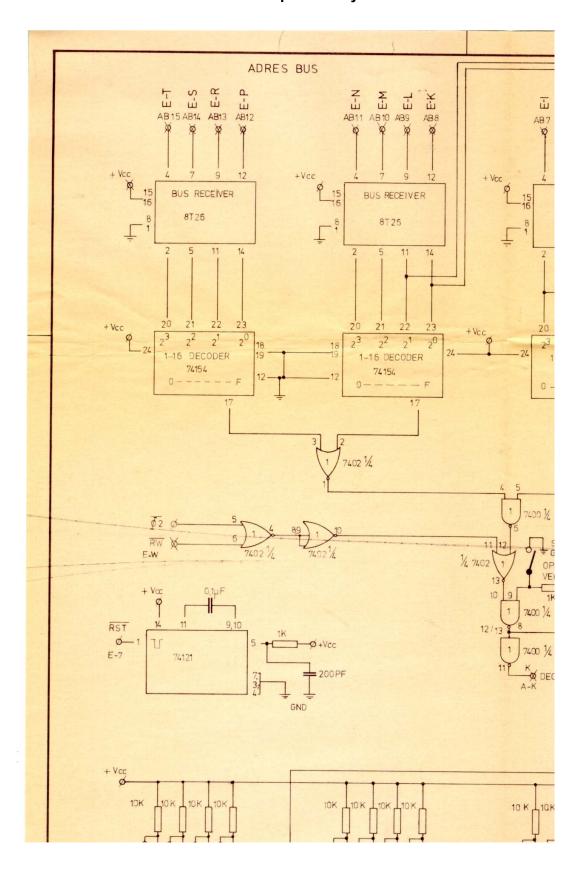
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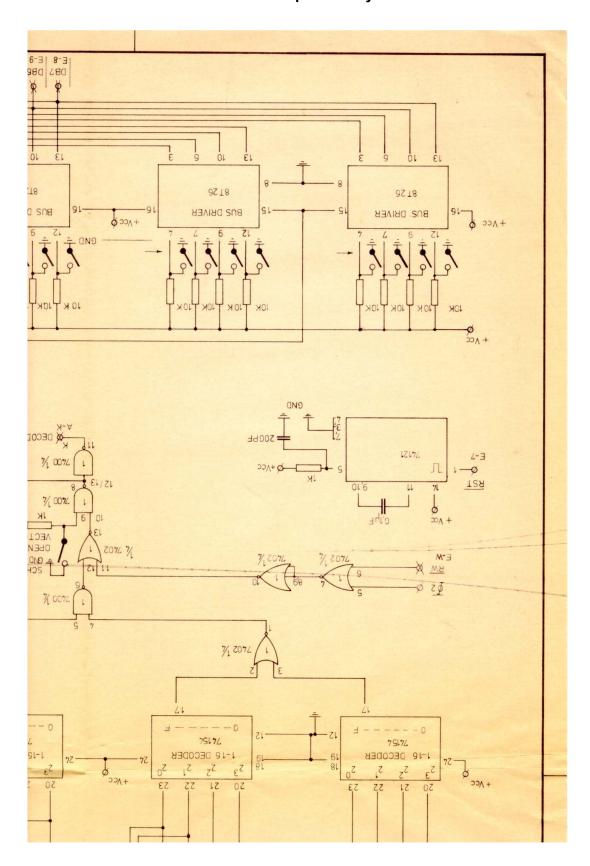
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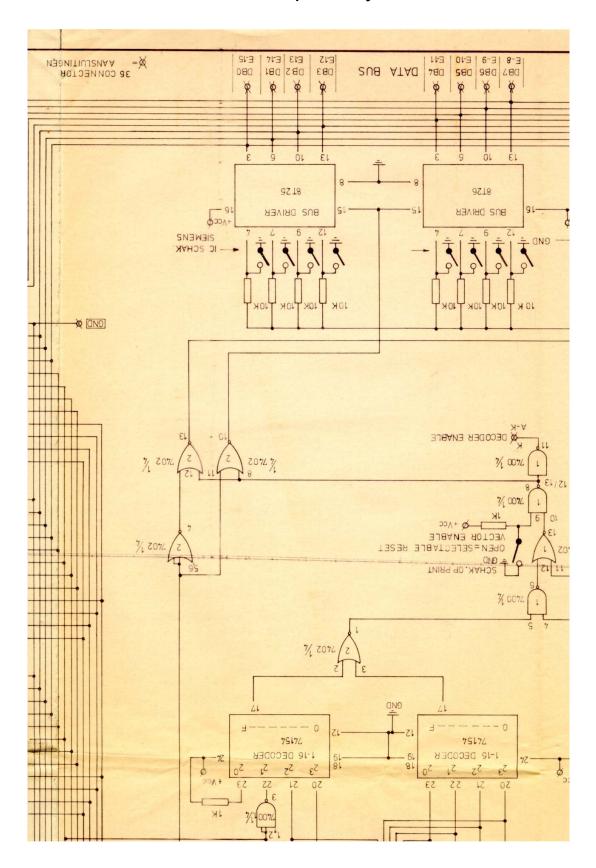
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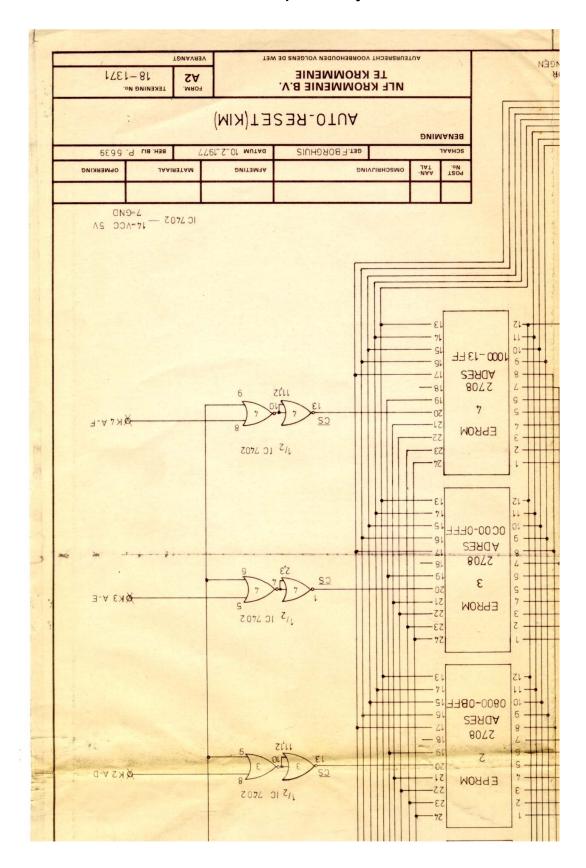
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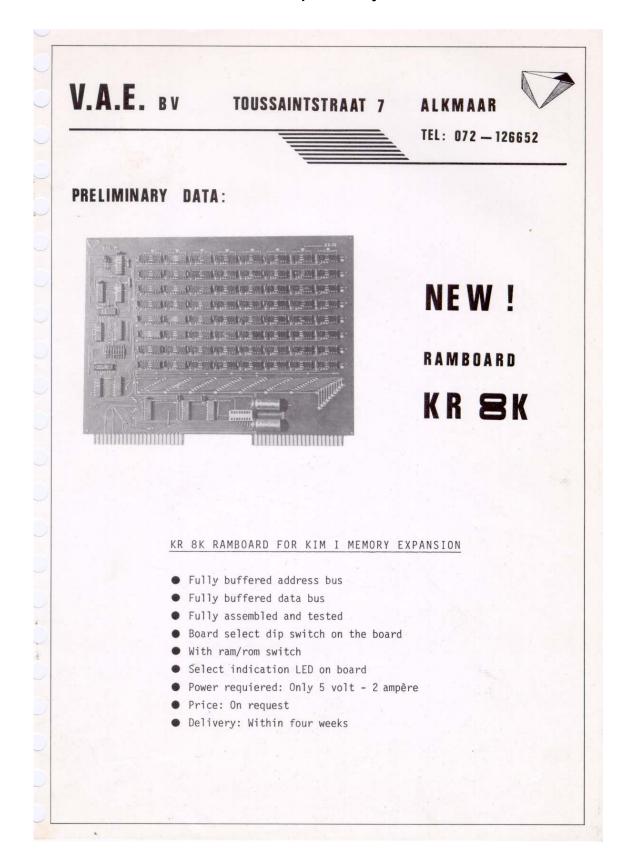


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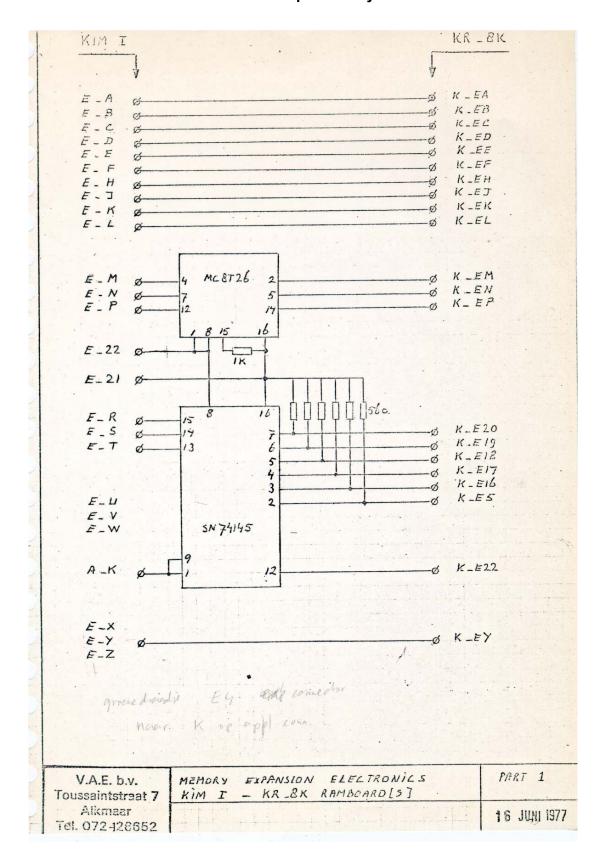


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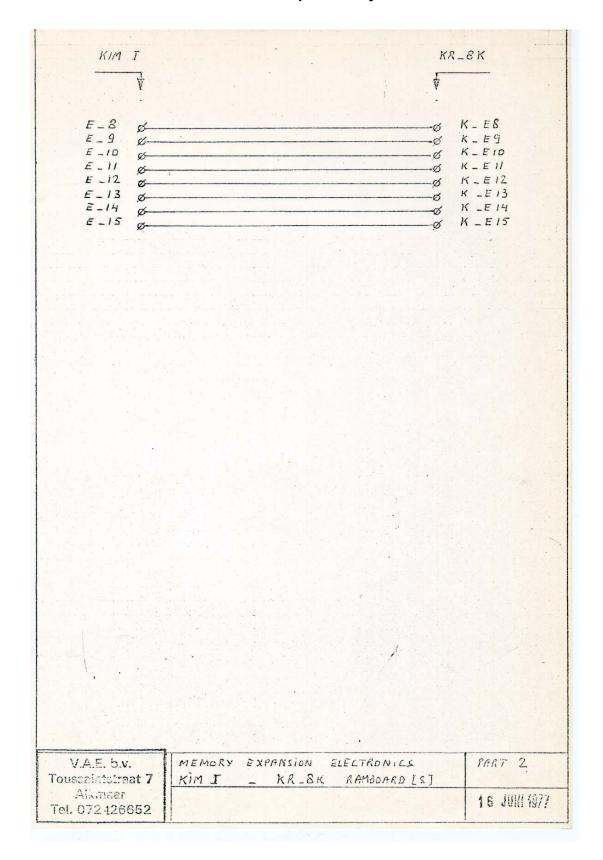




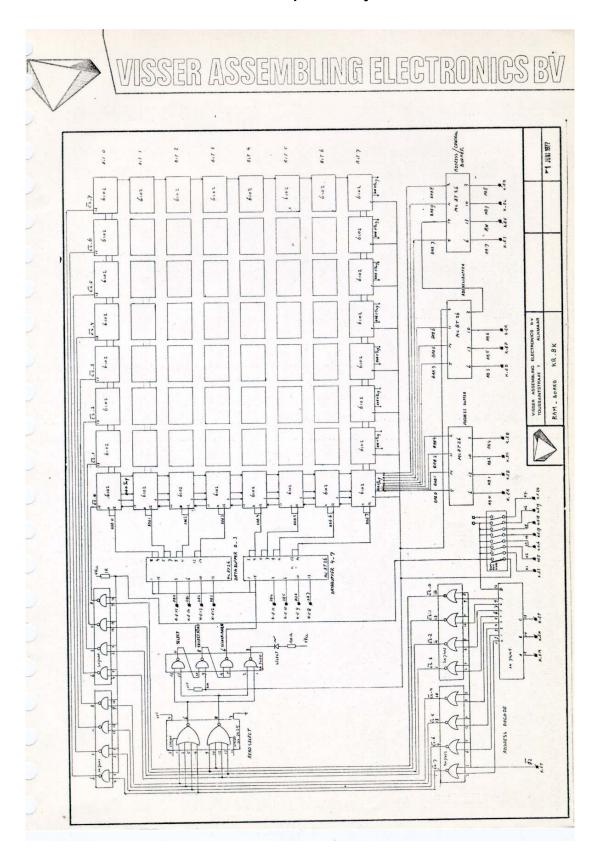
T4 KIM-1 expansion system



T4 KIM-1 expansion system



T4 KIM-1 expansion system



T4 KIM-1 expansion system

