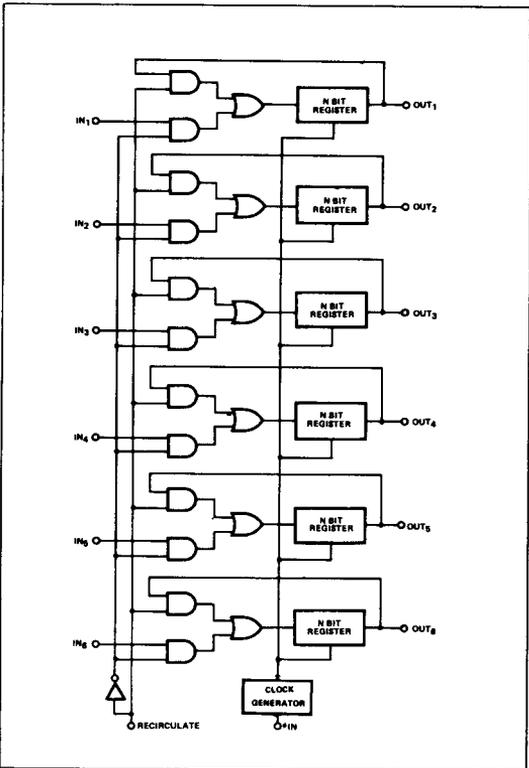# signetics

DESCRIPTION

These Signetics 2500 Series hex 32-bit and hex 40-bit recirculating static shift registers consist of enhancement mode P-channel silicon gate MOS devices integrated on a single monolithic chip. Internal recirculation logic plus TTL/DTL level clock signals are provided for maximum interfacing ease.
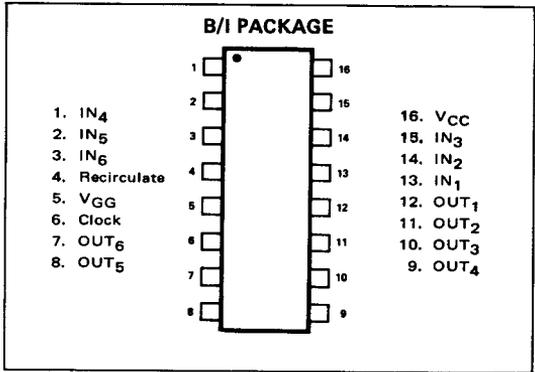
FEATURES

- TYPICAL CLOCK AND DATA RATE = 3MHz
- SINGLE TTL/DTL COMPATIBLE CLOCK
- LOW CLOCK CAPACITANCE
- RECIRCULATION PATH ON CHIP
- TWO BIT LENGTHS AVAILABLE
- SINGLE—ENDED (BARE DRAIN) BUFFERS
- TTL, DTL COMPATIBLE SIGNALS
- STANDARD PACKAGE — 16 PIN DIP
- P-MOS SILICON GATE TECHNOLOGY

BLOCK DIAGRAM

PIN CONFIGURATIONS (Top View)

B/I PACKAGE

1. IN_4
2. IN_5
3. IN_6
4. Recirculate
5. V_{GG}
6. Clock
7. OUT_6
8. OUT_5

16. V_{CC}
15. IN_3
14. IN_2
13. IN_1
12. OUT_1
11. OUT_2
10. OUT_3
9. OUT_4

APPLICATIONS

LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST STATIC BUFFER MEMORIES
CRT REFRESH MEMORIES — LINE STORAGE
LINE PRINTERS
CARD EQUIPMENT BUFFERS

TRUTH TABLE

RECIRCULATE	INPUT	FUNCTION
1	0	Recirculate
1	1	Recirculate
0	0	"0" is Written
0	1	"1" is Written

PART IDENTIFICATION TABLE

PART NUMBER	BIT LENGTH	PACKAGE
2518B	HEX 32	16-Pin Silicone DIP
2518I	HEX 32	16-Pin Ceramic DIP
2519B	HEX 40	16-Pin Silicone DIP
2519I	HEX 40	16-Pin Ceramic DIP

MAXIMUM GUARANTEED RATINGS (1)

|	
Operating Temperature (2)	$0^{\circ}C$ to $+70^{\circ}C$
Storage Temperature	$-65^{\circ}C$ to $+150^{\circ}C$
Package Power Dissipation at $T_A = 70^{\circ}C$	640 mW
Data and Clock Input Voltages and Supply Voltages with Respect to V_{CC}	$+0.3V$ to $-20V$

NOTES

1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a $150^{\circ}C$ maximum junction temperature and a thermal resistance of $125^{\circ}C$ C/W, junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at $+25^{\circ}C$ and nominal supply voltages.
8. Guaranteed input levels are stated for worst case conditions including a $\pm5\%$ variation in V_{CC} and a temperature variation of $0^{\circ}C$ to $+70^{\circ}C$. Actual input requirements with respect to V_{CC} are $V_{IH} = V_{CC} - 1.85V$ and $V_{IL} = V_{CC} - 4.15V$.
9. V_{OL} is dependent on R_L and input characteristics of driven gate.

DC CHARACTERISTICS

$T_A = 0^{\circ}C$ to $+70^{\circ}C$; $V_{CC} = +5V$ $+5V$ $\pm5\%$; $V_{GG} = -12V$ $\pm5\%$ unless otherwise noted. (Notes: 3,4,5,6,7)

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	INPUT LOAD CURRENT		10	500	nA	$V_{in} = -5.5V$, $T_A = 25^{\circ}C$
I_{LO}	OUTPUT LEAKAGE CURRENT		10	1000	nA	$T_A = 25^{\circ}C$
I_{LC}	CLOCK LEAKAGE CURRENT		10	500	nA	$V_{ILC} = GND$, $T_A = 25^{\circ}C$
I_{GG}	POWER SUPPLY CURRENT		16	25	mA	CONTINUOUS OPERATION $T_A = 25^{\circ}C$ $F = 1.5$ MHz
V_{IL}	INPUT "LOW" VOLTAGE			+0.6	V	Note 8
V_{IH}	INPUT "HIGH" VOLTAGE	+3.4		5.3	V	Note 8
V_{ILC}	CLOCK INPUT "LOW" VOLTAGE			+0.6	V	Note 8
V_{IHC}	CLOCK INPUT "HIGH" VOLTAGE	+3.4		5.3	V	Note 8

TIMING DIAGRAM
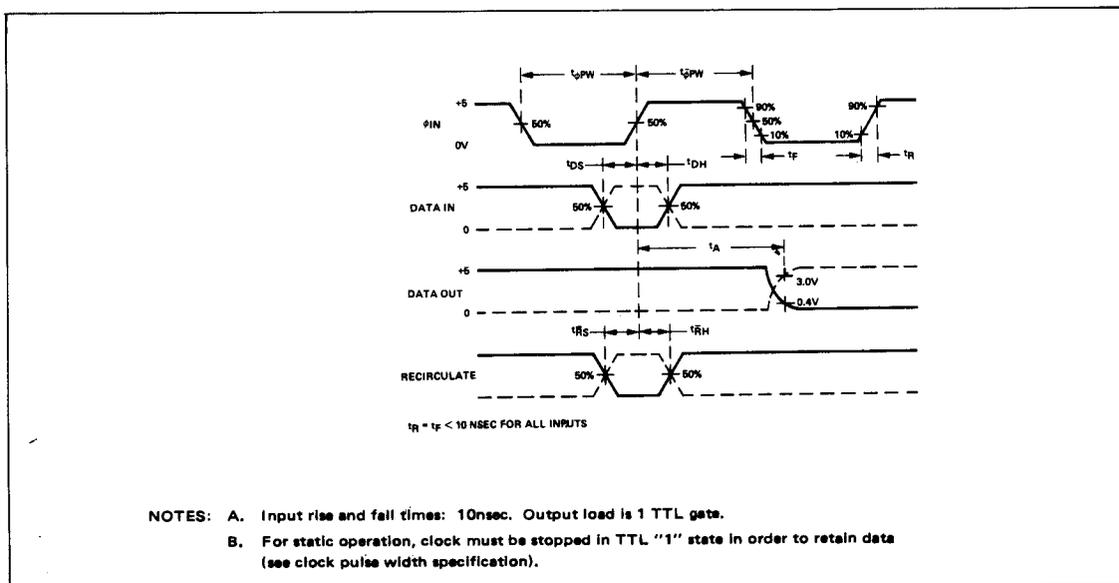
NOTES: A. Input rise and fall times: 10nsec. Output load is 1 TTL gate.

B. For static operation, clock must be stopped in TTL "1" state in order to retain data (see clock pulse width specification).

TIMING DIAGRAM

WRITE CYCLE
THE POSITIVE-GOING EDGE OF THE RECIR-CULATE CONTROL IS COINCIDENT WITH THE NEGATIVE-GOING CLOCK EDGE. THE OUTPUT ENABLE CONTROL MAY BE EITHER "1" OR "0". IF IT IS "1", PREVIOUS DATA WILL BE READ, AND THE 1st BIT WILL BE READ AFTER THE FOURTH RISING CLOCK EDGE.

RECIRCULATE CYCLE
DATA RECIRCULATES WHILE THE RECIR-CULATE CONTROL IS "0". NEW INPUT DATA IS IGNORED. OUTPUT DATA IS READ OUT DURING THIS TIME.

AC CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = +5V +5V ±5%; V_{GG} = −12V ±5%, V_{ILC} = 0.4V to 4.0V

| SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
FREQUENCY	CLOCK REP RATE	DC	3	2	MHz	See Max Frequency Curve
$t_{\phi PW}$	CLOCK PULSE WIDTH	.300		100	μsec	See Note B
$t_{\bar\phi PW}$	CLOCK PULSE WIDTH	.200		DC	μsec	
t_R, t_F	CLOCK PULSE TRANSITION			5	μsec	
t_{DS}	DATA WRITE (SET-UP) TIME	100			nsec	
t_{DH}	DATA TO CLOCK HOLD TIME	50			nsec	
t_A	CLOCK TO DATA OUT DELAY		300	350	nsec	
t_{RS}	RECIRCULATE SET-UP TIME	150			ns	
t_{RH}	RECIRCULATE HOLD TIME	50			ns	
C_{in}	INPUT CAPACITANCE		5	7	pF	@ 1MHz; V_{in} = V_{CC}; V_{AC} = 25mV p-p
$C\phi$	CLOCK CAPACITANCE		6	7	pF	@ 1MHz; V_ϕ = V_{CC}; V_{AC} = 25mV p-p
V_{OL}	OUTPUT "LOW" VOLTAGE		+0.5		V	I_{OL} = 1.6mA
V_{OH}	OUTPUT "HIGH" VOLTAGE	+3.8			V	I_{OH} = 100μA

APPLICATIONS DATA
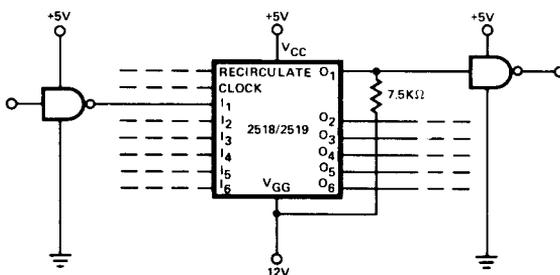
TTL INTERFACE

APPLICATIONS (Cont'd)
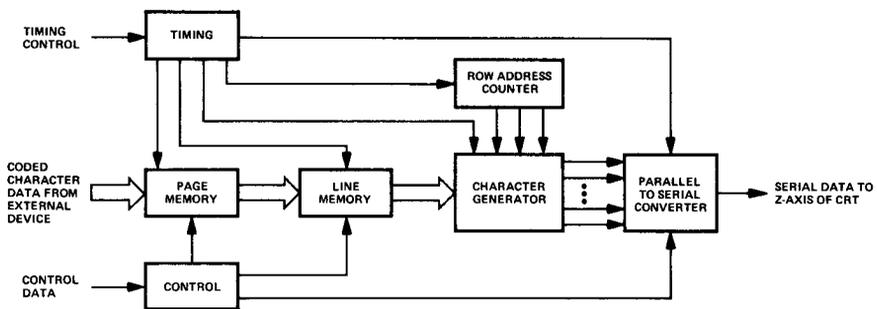
PAGE MEMORY: THIS MEMORY CONTAINS CHARACTER CODES. TYPICALLY, IT CONTAINS THE SAME NUMBER OF CHARACTER CODES AS THE NUMBER OF CHARACTER ON A FULL SCREEN.

LINE MEMORY: THIS MEMORY CONTAINS THE CHARACTER CODES FOR ONE LINE OF THE CRT DISPLAY. THE 2518 AND 2519 WORK WELL AS LINE MEMORIES.

CHARACTER GENERATOR: THE CHARACTER GENERATOR IS TYPICALLY A ROM WHICH CONVERTS CHARACTER CODE INPUTS TO DOT MATRIX BITS AT THE OUTPUT.
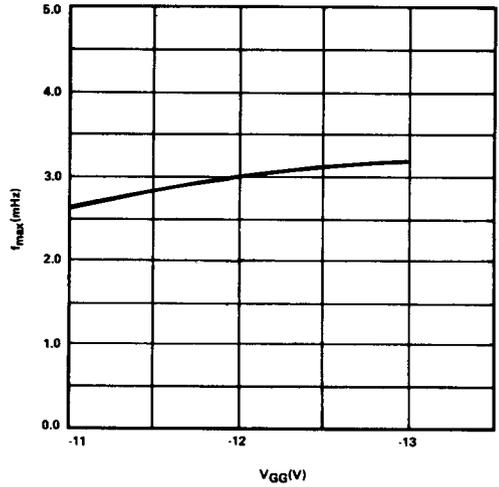
CIRCUIT SCHEMATIC
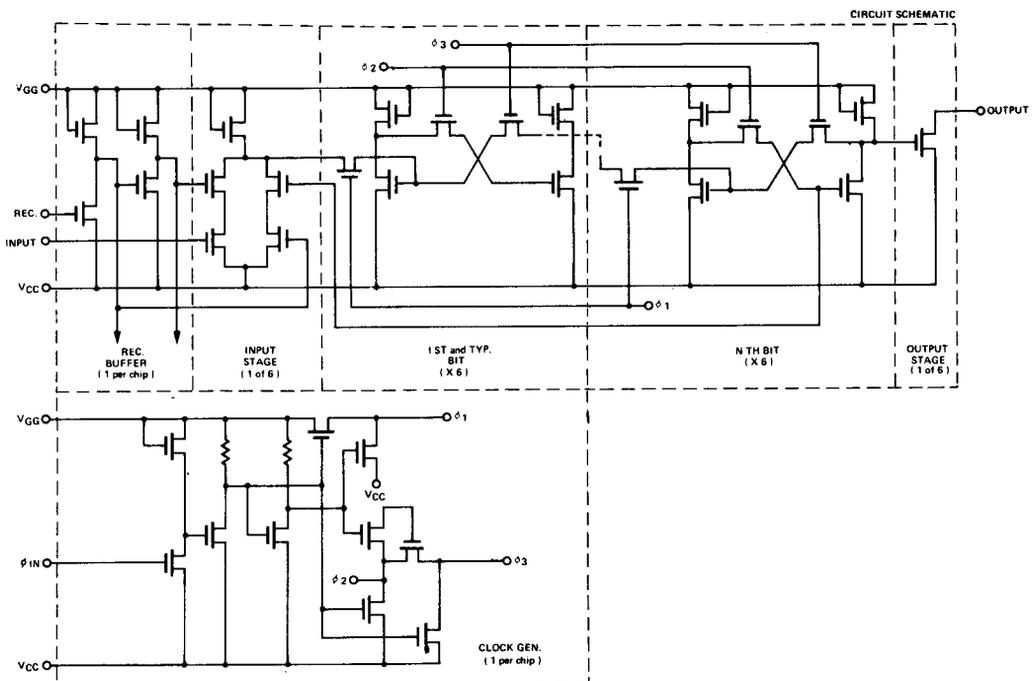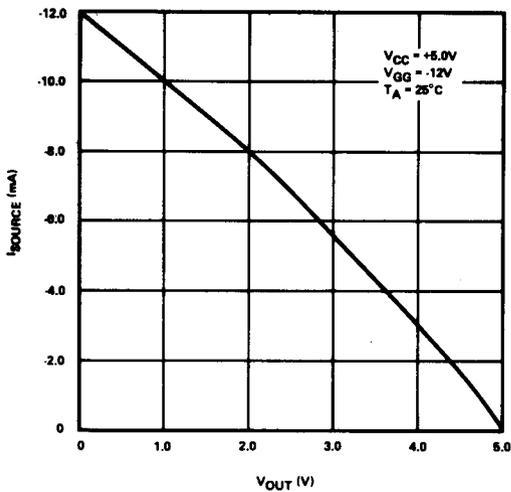
TYPICAL CHARACTERISTIC CURVES

I_{GG} VERSUS TEMPERATURE
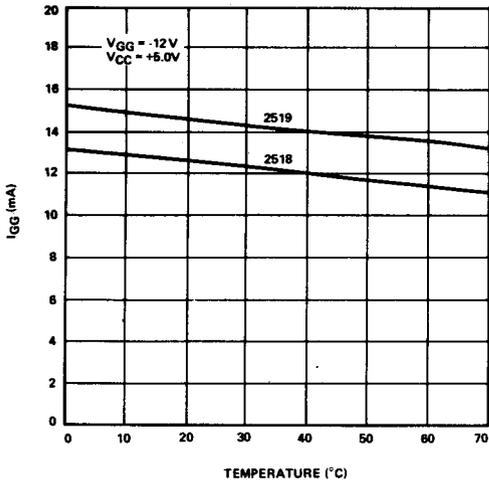
MAXIMUM SHIFT FREQUENCY VERSUS V_{GG}

I_{SOURCE} VERSUS V_{OUT}

I_{GG} VERSUS V_{GG}